iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** V **Month of publication:** May 2017

DOI:

www.ijraset.com

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Volume 5 Issue V, May 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

A Review on Multiplier Circuits based on Various Performance Parameters

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Abstract: ***A processor consumes most of its hardware resource and time in carrying out multiplication operation than all other arithmetic operations like addition and subtraction. The central processing unit in a computer devotes a substantial quantity of time interval in implementing arithmetic operations, specifically multiplication operation. In this paper, comparative study of different multipliers is done namely Array multiplier, Booth multiplier, Modified booth multiplier, Wallace tree multiplier, Modified Booth Wallace Multiplier and Dadda Tree Multiplier based on various parameters like speed, area, circuit complexity and power consumed. So, inorder to enhance the system performance it is necessary to design a fast multiplier.***
Keywords: Carry Save Adder(CSA);Carry Look-ahead adder; Partial Product Generator(PPG);Partial Product Reduction Tree(PPRT); Final Carry-Propagate Adder(CPA).

I. INTRODUCTION

Multiplication is an important fundamental function in every digital signal processor. Computer arithmetic operations are widely used in many digital signal processing applications. Multiplication operations are more complicated than adder and subtractor operation, so the operating speed of a DSP system is typically determined by the speed of multiplier operation. Therefore high speed multiplier is much desired. The main factor in determining the instruction cycle time of a DSP processor is still the multiplication operation. With an ever increasing search for high computing power on battery powered mobile devices, design accentuation has shifted from optimizing conventional delay time and size of area to minimizing power dissipation whereas still maintaining the high performance. Hence designing of multiplier circuit with high speed, low power consumption, lesser area or even combination of them is of great interest.

The architecture of multiplier circuit can be broadly categorized into three main stages namely, partial product generation stage, partial product reduction stage and addition of the reduced partial product stage. Normally shift and add algorithm has been used but from delay point of view this is not appropriate, since lot of adders will be used. The speed of multiplication operation can be geared up either by reducing the amount of partial products or by increasing the speed of accumulation of partial products. By using multibit processors the number of addition stages of partial products can be reduced.

Multiplier circuits are available in different forms and each of them are having different algorithms and structures. Different multipliers have different performance parameters and each of them can be optimized to get better performance parameters.

Different researchers have developed and optimized different kinds of multipliers. In the following section the six multipliers namely Array multiplier, Booth multiplier, Modified booth multiplier, Wallace tree multiplier, Modified Booth Wallace Multiplier and Dadda Tree Multiplier are compared based on different performance parameters.

II. ARRAY MULTIPLIER

Array multiplier is an well-known multiplier due to its regular structure shown in Fig 1. The array multiplier uses add and shift algorithms for its multiplication operation. By multiplying the multiplicand with each bit of the multiplier the partial products are generated, the partial products generated as a result are shifted according to their bit orders and then added together. The addition can be performed with normal carry propagate adder. N-1 adders are required to designing a array multiplier, where the multiplier length is denoted by N. The power consumption is more, since array multiplier uses more components when compared with other multipliers [2]. When an array multiplier is designed with CSA the speed of the multiplier is improved by 78.3%, area reduced by 4.2% and power consumption decreased by 1.4% [1].

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				A3	A2	A1	A0
			x	B3	B2	B1	B0
		+	C	B0A3	B0A2	B0A1	B0A0
	+	C	B1A3	B1A2	B1A1	B1A0	
+	C	B2B3	B2A2	B2A1	B2A0		
C	B3A3	B3A2	B3A1	B3A0			
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Fig 1: Array Multiplication Structure

III. BOOTH MULTIPLIER

The performance of multiplier can be improved by reducing the number of partial products generated. The Booth multiplier is one such multiplier. To reduce the number of partial products the booth multiplier scans the three bits that is two bit from the present pair and a third bit from the high order bit at a time [3]. To speed up the multiplication operation Booth multiplier performs several steps of multiplication at once. The addition/subtraction operation can be skipped, if the successive bits in the multiplicand are same this can be proved from the basics of Booth algorithm. Thus the delay associated with Booth Multiplication is smaller when compared with Array multiplier. However the performance of Booth Multiplier based on delay is input data dependant. The method of Booth multiplier reduces the numbers of adders and hence the delay required to produce the partial sums by examining three bits at a time. The main drawback of booth multiplier is the power consumption due to the usage of large number of adder cells[3]. An 8 bit Booth multiplier takes 5266.78 μm^2 area, 378.33µW power and 3.98ns delay[7].

IV. MODIFIED BOOTH MULTIPLIER

To reduce the number of partial products the Modified Booth multiplier scans three bits at a time [4]. In the design of Modified Booth multiplier modified booth encoder and selector techniques are used to reduce and rearrange the partial products. This reduces the number of gate count and on the other hand improves the performance of the multiplier. The Booth encoder encodes the multiplier bits using Radix eight or Radix four algorithm. A n-bit binary number can be interpreted as a n/2- digit Radix four number, a n/3-digit Radix eight number and so on, that deals with more than one multiplier bits in each cycle for using high radix multiplication [4]. When the operands are equal to or greater than 16 bits modified Radix four Booth algorithm is used. In this algorithm, in order to reduce the number of partial products the two's complement of the multiplier is encoded The block diagram of modified booth multiplier is shown in Fig 2.

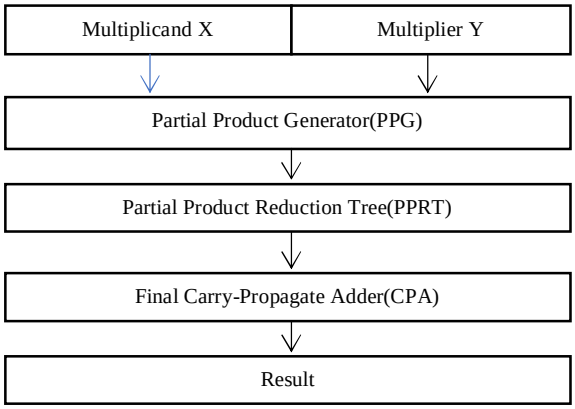

Fig 2 Block Diagram of Modified Booth Multiplier

In order to improve the performance of modified booth multiplier pipelining concept is introduced. The Booth multiplier with pipelining concept consist of three modules: 1) the modified Booth encoder and decoder module to generate N/2 partial products; 2) the Wallace tree module to add the partial products in parallel; 3) the carry look-ahead adder module for the final addition[5]. Since the speed improvement ratio is much greater than the area increase ratio, they can be used in the application systems which require very high performance while the area is tolerable[5].

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V. WALLACE TREE MULTIPLIER

Wallace introduced a new process for the fast multiplication of two numbers. The multiplication of two numbers is carried out by using three important steps, in the first step the bit products are formed, in the second step the bit product matrix is reduced to a two row matrix where sum of two row equals the sum of bit products and in the third step the two resulting rows are summed with a fast adder to produce a final product.

In this method, a three bit signal is passed to a one bit full adder which is called a three input Wallace tree circuit and the output signal is given as an input to the next stage full adder of the same bit and the carry output signal is passed to the next stage full adder of the same bit. By using compressors, such as 4:2 compressor, 5:2 compressor, 6:2 compressor and 7:2 compressors the performance of the Wallace tree multiplier can be improved. The usage of compressors in Wallace tree multiplier will reduce the number of half adders used in the design of multiplier circuit that in turn reduced the complexity of the circuit as well as time delay[6]. An 8 bit Wallace tree multiplier occupies 1315.15μm^2 area, 678.43µW power and 1.73ns time delay[7]. The structure of Wallace tree multiplier with 3:2 compressor is shown in Fig 3

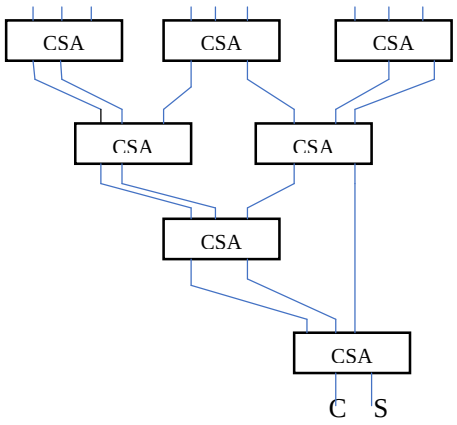

Fig 3. Wallace tree multiplier with 3:2 compressor

VI. MODIFIED BOOTH - WALLACE MULTIPLIER

The modified Booth-Wallace multiplier overcomes the disadvantages of the previously discussed multipliers. The four major modules used in modified Booth Wallace multiplier are, booth encoder, partial product generator, Wallace tree and carry look ahead adder[9]. The radix four or radix eight of the multiplier bit is done by booth encoder. Partial products are generated by the generator based on the multiplicand and the encoded multiplier. The performance of the modified booth algorithm is limited for large multipliers of thirty two bits. So Booth multiplier along with Wallace tree multiplier is used to make the multiplication operation faster[8]. The block diagram of modified booth Wallace tree multiplier is shown in Fig 4

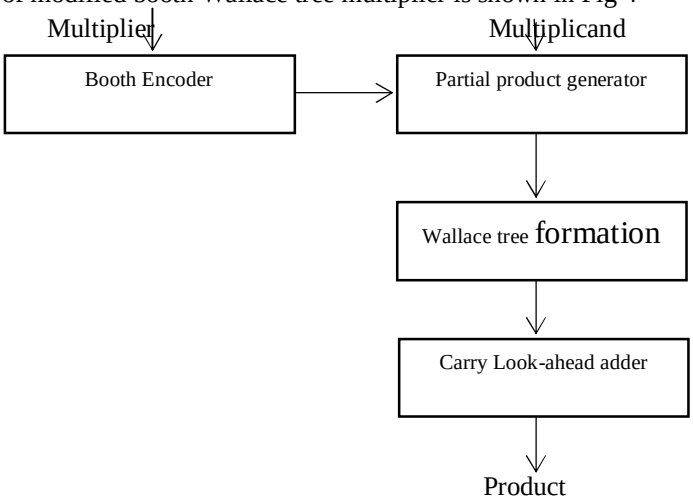

Fig 4 Block Diagram Of Modified Booth Wallace Tree Multiplier

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If Radix 4 algorithm is used the modified Booth algorithm reduces the number of partial products to half the number of multiplier bits, if Radix-8 booth algorithm is used it reduces the number of partial products to one third of the number of multiplier bits. The modified booth Wallace multiplier will reduce both chip area and delay because it make use of carry save adder for fast accumulation of partial products[4].

VII. DADDA TREE MULTIPLIER

Dadda multiplier perform the reduction of partial products at each level. The three steps in dada multiplier are

Step 1: Multiply each bit of one of the arguments, by each bit of the other.

Step 2: Reduce the number of partial products to two layers of full and half adders.

Step 3: Group the wires in two numbers, and add them with a conventional adder.

Dadda tree multiplier occupies less area when compared with Wallace tree multiplier. For an 8 bit multiplier dada multiplier uses seven half adders and thirty five full adders. Due to the usage of CPA the delay in dada multiplier is reduced. An 8 bit dada multiplier takes 1395.79 μm^2 area, 645.60µW power and1.72ns delay[7].

VIII. CONCLUSION

In this section, six multipliers are compared based on speed, area, circuit complexity and power consumed. In terms of its circuit complexity, the array multiplier is the simplest of all the multipliers, but the speed of multiplication is low since it uses the old add and shift algorithm. Based on the above study it can be concluded that of all the multipliers used Dadda tree multiplier is the fastest of all the multiplier since it is having a very small delay. In terms of power consumption booth multiplier consumes less power when compared with all the other multipliers discussed. Wallace tree multiplier occupies lesser area when compared with other multipliers. From the various studies, we came to realize that often there is a trade-off between performance parameters of the multipliers. If, we could design a new multiplier by combining various optimizing techniques with low delay, low power consumption and lower area, then the design will certainly give a boost to the trending technologies.

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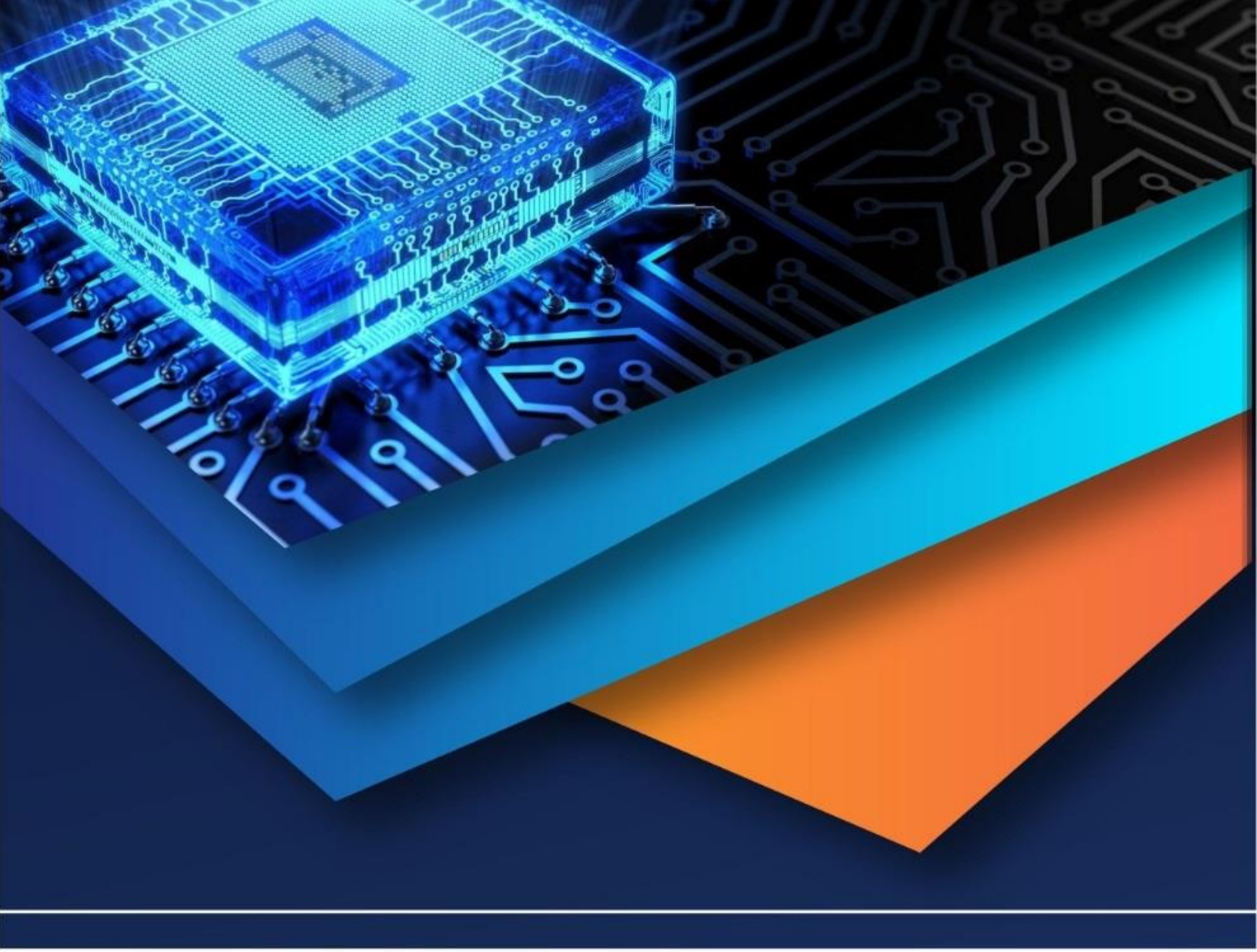

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