Implementation of Full Adder using CMOS Logic

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Abstract: this paper gives an insight into the use of Complementary Metal Oxide Semiconductor (CMOS) logic which can be made use of to implement various circuits, both combinational and sequential. In this paper, full adder, having three inputs is simulated with the help of P Spice software, and the output waveforms are recorded. CMOS ICs have gained recognition all over the world, due to its power handling capacity, small size and increased speed.

Keywords: CMOS, Full Adder, MOSFET, Net-list, P Spice

I. INTRODUCTION

Very Large Scale Integration (VLSI) Technology has significantly reduced the size of the circuits and now, billions of transistors can be fabricated onto a single chip or an IC. This has in turn, been very advantageous to the industry in terms of increased speed and greater reliability. Logic circuits, both combinational and sequential can be simulated with the help of Personal Simulation Program with Integrated Circuit Emphasis, more commonly abbreviated as P Spice. The waveforms are obtained with the help of probes as per the three inputs given to the circuit in the form of AC voltages.

CMOS logic basically encompass of p-MOS and n-MOS logic, which are complementary to each other. A basic CMOS inverter, which consists of two MOSFETs, is shown in Fig 1. N-MOS is build with n-type source and drain and p-type substrate and p-MOS is build with p-type source and drain and n-type substrate. The majority charge carriers in n-MOS in electrons and that in p-MOS is holes. Due to this, the n-type MOSFETs are usually faster than p-type MOSFETs, since electrons are twice as fast as holes. This also makes n-MOS IC’s smaller in size and less immune to noise than p-MOS IC’s. While simulating any circuit design, MbreakP and MbreakN models are used for n-MOS and p-MOS respectively.

Drain to Source current equation in n-MOS is given by:

\[ I_{DS} = \beta V_{DS} (V_{GS} - V_T - V_{DS}/2) \]

II. WORKING AND FUNCTIONALITY

The p-MOS circuit is also known as ‘pull-up’ network and the n-MOS circuit is called ‘pull-down’ network. When the input is high, i.e. when \( V_{in} = 1 \), p-MOS acts as an open circuit and when \( V_{in} = 0 \), n-MOS acts as an open circuit. This is the reason why p-MOS is efficient to transfer strong logic-1 and n-MOS is efficient to transfer strong logic-0. Also, since no static current flows and there is no such static power dissipation, CMOS can be efficiently used for higher density packages.
III. P SPICE SOFTWARE

Cadence P Spice simulation technology offers its users a single, unified design environment for both, simulation and PCB Design. It offers a vast variety of models that are available for simulation purpose. It is quiet efficient software as it is easy to debug and identify the errors in the model. The components can be dragged and dropped to the design or can be added via the Net-list or the library. This property of rectifying the errors is useful to the designers as it saves a lot of their precious time as well as is cost effective.

A. Pseudo n-MOS Logic

In high density circuits, complex CMOS gates may face a problem due to the large area requirements. To reduce the number of transistors, a single p-MOS transistor with its gate terminal connected to the ground, is used as the load device. The gate terminal of the p-MOS is grounded in order to keep it permanently in ON state. Hence, with a simple pull up arrangement, the complex circuit can be implemented with much fewer transistors. Therefore, in comparison with the CMOS Logic, which consisted of 2N transistors, only N+1 transistor are required in Pseudo n-MOS Logic.

Although it reduces the number of transistors, the primary disadvantage of using pseudo n-MOS is the non zero static power dissipation, due to the always ON p-MOS load device conducts a steady state current when the output voltage is less than $V_{DD}$.

B. Full Adder

Full adder is a combination circuit that adds three 1-bit binary numbers, and outputs two 1-bit binary numbers, representing sum and carry respectively. All the desired components are selected from the library and three AC inputs (0-5V) are provided in terms of AC voltages, all components are wired and the simulation results are compared to the truth table of Full Adder to verify.

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<tr>
<th>INPUTS</th>
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<td>A</td>
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The Boolean equation for full adder is given as:

$\text{Sum} = \overline{A}BC + \overline{A}BC + ABC + ABC$

$= A(B \oplus C) + C(\overline{A}B + AB)$

$= A(B \text{xor} C) + (A \text{xnor} B)$

$= A \text{xor} B \text{xor} C$

$\text{Carry} = AB + BC + CA$
Fig. 3 Design of Full Adder on P Spice (SUM)

Fig. 3 Design of Full Adder on P Spice (CARRY)
Fig. 4 Output waveform (SUM)

Fig. 4 Output waveform (CARRY)
IV. CONCLUSIONS

Full adder circuit was implemented with the help of P Spice, by using the pseudo n-MOS logic design. Output waveforms, were recorded and the Netlist was obtained which depicts the connection between any two nodes in the circuit. Further it was observed that the circuit worked more efficiently as less number of transistors needed was less as compared to the CMOS logic design. In order to further improve the performance of the circuit, domino and dynamic logic can be used.

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REFERENCES
