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A Systematic Perspective for 4Ghz Frequency Synthesizer Integration on to Single Systems

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Abstract: ***In wireless medium, necessity of higher frequency is expanding day by day. For higher frequency deploy system data rates should be higher. In unguided medium, as signal passes a longer distance and due to intervention of noise, there is fallacy. In phases and frequencies and we get a drifted output. In view of this, we are prompted to make a low power frequency synthesizer which would provide a lower locking time, low settling time, average value of damping factor to give a regulated frequency response at the output. The suggested design aspect is for higher frequency which is executed in IEEE 802.11 WLAN standard and OFDM technology, Bluetooth technology, high frequency processor. We have used Microwind 3.1 55nm technology and ADS as outline tool to execute design.***

Keywords: Frequency synthesizer, phase frequency detector, voltage-controlled oscillators, Microwind 3.1, ADS, wireless communication

I. INTRODUCTION

The stipulation for high data rate wireless local area network, Higher frequencies processors with lower power utilization is speedly expanding. The unlicensed national information infrastructure (UNII) band provides 700MHz of spectrum at 3.4 to 3.8 GHz for wireless communication. The lower 200MHz of this band overlie the higher execution radio LANs frequency band. This frequency band is divided into 8 channels. In this paper we scrutinize the blueprint of a thoroughly integrate frequency synthesizers as a local oscillator (LO). We also signify the upper hand of a voltages controlles differentiate injection lock frequency divider as a lower power frequency divide in this higher frequency synthesizers[1]. The Frequency synthesizers discovered in the before time years for decrement of the noise in the received signal was examine that the signal forthcoming from the distance transmitters is guve tise to some noise if it is not duly tuned and later it examined that the noise is developed due to inconsistency of phase and frequency at the receiver input and a circuit was blueprinted to reduce the phase and frequency errors at the receivers site. With the time goes the frequency of functionality increases and the necessity of frequent loop locking is essential. This feature prompted us to make a frequency synthesizer for higher frequency applications. In this research, new methods and blueprint are introduce and develop to discourse those disputes. 1st a low phase noise ring oscillators and a capacitor multiplier-type with a high multiplication factors systematically shortens the silicon area of sub components, and a compact programmable delay-locked loop based frequency multipliers is designed to overlap the PLL based frequency synthesizer. 2nd, the charges spreading mechanism for repressing reference spurs is theoretical analyze [2], and edge interpolation method for implement the mechanism is designed.

II. SYSTEM ARCHITECTURE

A. *Block Diagram*

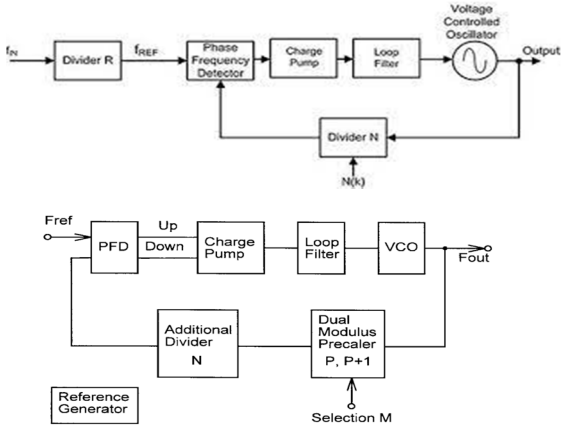


Figure 1: Block diagram of frequency synthesizer

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B. Illustrations

Frequency synthesizers is circuits which synthesize and generate a clock for the determined frequency. It make use of a negative feedbacks to match phase and frequency of signal so that any signal get retrive should be exactly matched. Frequency multipliers which accumulate by a factor to lower frequency input F_{ref} to transfigure it into higher frequency output $F_{out.}$
The main purpose of this frequency synthesizer block is to recover the signal without phase and frequency error.

Main block of frequency synthesizer is

1) Phase frequency detector
2) Low pass filter
3) Charging pump
4) Multi module divider
5) Voltage controlled oscillator

C. Phase Frequency Detector

The 1st block of PLL is PFD , which is used for detection of frequencyiwith reference frequency. The basic function of a PD or a PFD is to detect the difference in the phase and frequency.A simple design of PFD consists of two D flip flops and AND gate. As the figure shows the D input of the flip-flops is connected to VDD and the input signals (CLKREF,
CLKVCO) are applied to the clock input. When one of the clocks change to high, this flip-flop will charged and change its output to high. The AND gate is for preventing both flip-flop to be high at the same time. As we can see the inputs of the AND gate are the both Up and DOWN signal from both flip-flops, and the output of the AND gate is connected to the reset input of the flip-flops. As soon as both outputs (UP, DOWN) are high the AND gate will generate a high signal that will reset both flip-flops avoiding the situation of both high at the same time. The signal transaction in figure 2 gives an example of CLKREF leading CLKVCO The UP and the DN, to convey the information. By rising edges of the reference clock, *fref*, and the divided VCO clock, *fdiv*, the UP and the DN become 1 simultaneously.

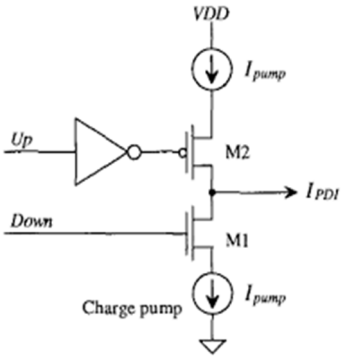


Figure 2: Block diagram of phase frequency detector

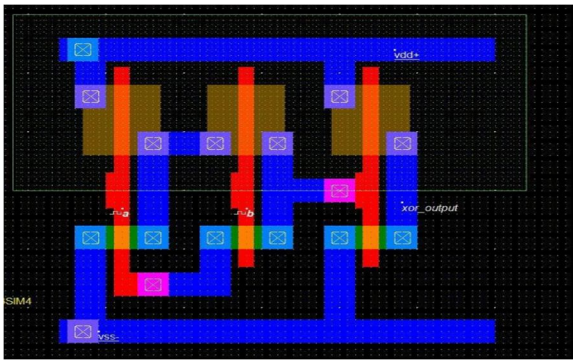


Figure 3: CMOS layout of phase detector

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D. Charging Pump

Charge Pump in a phase locked loop (PLL) generates non-ideal effects such as current mismatches at the output node and switching errors at the pull up and pull down networks. This work presents a novel transmission gate cascode current mirror charge pump circuit. The switches incorporated in this work are Transmission Gates which help to reduce various switching errors, and only one supply independent reference current source is used to have a minimum current mismatch First, the charge pump converts the pulse-modulated phase/frequency difference information into corresponding charges, and then these charges are translated to DC voltage by the loop filter.

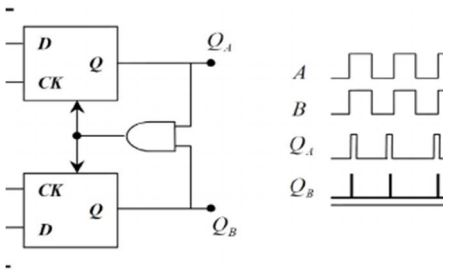


Figure 4: Block diagram of charge pump and second order loop filter

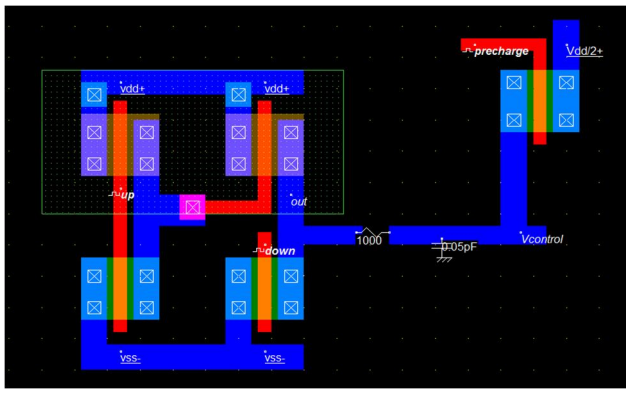


Figure 5: CMOS Layout of charge pump and loop filter

E. Loop filter

The design of the PLL, loop filter is crucial to the operation of the whole phase locked loop. The actual circuit of the PLL loop filter is generally remarkably simple, but it has a major impact on the performance of the loop. In the design of the loop filter the choice of values is normally a very careful balance between a number of often conflicting requirements. Therfore high order loop filter is derive over best noise abolition a loop filter of order 2 or more is used in most of the crucial application PLL circuits. If the PFD output is Q_a high for time Δt in that case the total phase error at the output of the PFD is

$$\Delta\varphi=\Delta t/T_{clock}*2\Pi(\text{radian}) \qquad (1)$$

Where is the phase error of the two input at PFD and the value of phase error are given in radians and the value of output voltage of charge pump is

$$V_{charge\ pump} = \{(V_{DD}-0)/4\Pi\}*\Delta\varphi= K_{cp}*\Delta\varphi \quad (2)$$

F. Voltage-Controlled Oscillator

To enhance the phase noise performance of a ring VCO, the proposed ring VCO adopts the saturated type delay cell of with a cross-coupled latch. Thus, the delay cell eliminates the tail current source and has pseudo-differential configuration using a PMOS cross-coupled latch. As a saturated-type VCO, the delay cell allows a rail-to-rail output signal swing. In addition, the cross-coupled latch accelerates the signal and provides fast-switching edges. When the signal is injected, the latch operates in the direction of opposing the signal transition in the PMOSs. However, after a while, the function of the latch change into a positive feedback and accelerates the signal transition. With the rail-to-rail swing signal with fast-switching transition, the proposed oscillator can enhance phase noise performance compared to conventional ones.

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A typical example of an unturned oscillator is a ring oscillator. The ring VCOs without inductors can be implemented in a small die area. Thus, in this work, a ring type oscillator has been considered in order to integrate a VCO generating quadrature output signals for the SSB mixer in compact chip area for improving the poor phase noise performance the proposed oscillator adopted a saturated-type delay cell with a latch configuration. The schematics of the proposed delay cell and the 3-stage ring oscillator are shown in Figure,

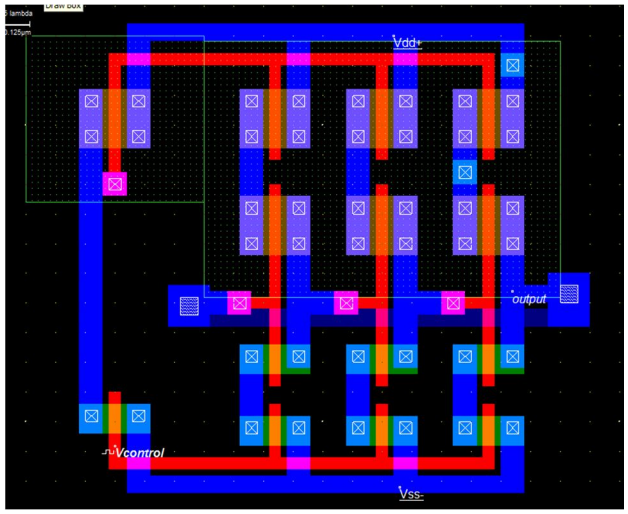


Figure 6: Diagram of three stage ring oscillator.

G. Multi-Modulus Divider

A high-frequency programmable divider is presented with the improved timing of the multi-modulus divider structure and the high-speed embedded flip-flops. The D flip-flop and logic flip-flop are proposed by using a fast pipeline technique, which contains single-phase, edge-triggered, ratioed, and high-speed technologies. The circuits achieve high-speed by reducing the capacitive load and sharing the delay between the combination logic blocks and the storage elements. By the way, it is suitable for realizing high-speed synchronous counters. The programmable divider using proposed flip-flops is measured in 0.25-μm CMOS technology with the operating clock frequency reaching as high as 4.7 GHz under the supply voltage of 3V.

The multi-modulus divider is a programmable architecture of generic chain of N/N+1 divider in which one divider is connected to other in the cascaded manner so that every divider divides the output of the previous divider in a controlled way of division. The N/N+1 divider represent here as the 2/3 divider in which the same divider circuit divide the input either by 2 or by 3 depending upon the programmable input of the divider. The 2/3 divider circuit is the combination of four D-latch which are arranged by the combination of AND gate and NOT gate with them in which the input frequency is given to the clock point in each latch

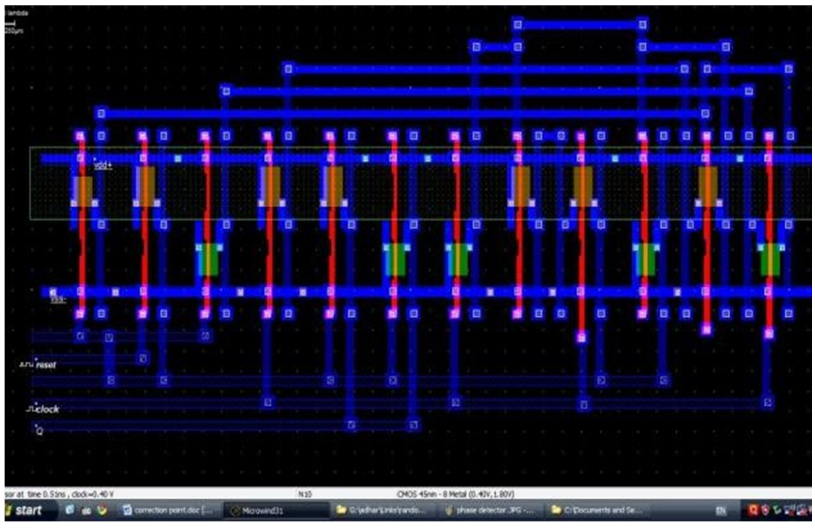


Figure 7: Block diagram of Multi module divider

H. Frequency Synthesizer in ADS

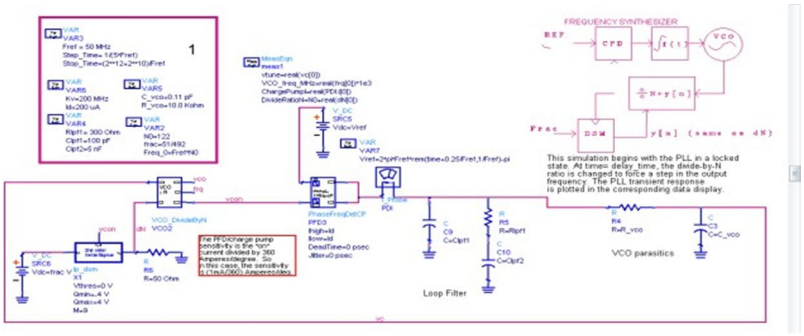


Figure 8: Complete architecture of frequency synthesizer in ADS tool

III. NOISE IN FREQUENCY SYNTHESIZER

The outputs of the practical systems deviate from the required response. This is because of deformity and noise in the system. The supplied noise also acts on the output noises of the frequency synthesizer system. There are mainly two types of noise. They are describe below.

A. Phase Noise and Jitter

This paper presents the design, the phase noise analysis and measurement results of a fourth-order phase-locked loop (PLL) circuit. The PLL is composed of a four-stage inductorless ring oscillator, a 1/16-divider, phase-frequency detector (PFD), charge pump and loop filter, which all are fully differential circuits. A tuning range of 6 to 11 GHz is achieved using delay interpolation elements in the ring oscillator. In fact, these simple expressions predict jitter and phase noise much more accurately than oscillation frequency; this is similar to what is seen in amplifier design, where input-referred noise is predicted much more accurately than gain.

Jitter is the deviation from true periodicity of a presumably periodic signal, often in relation to a reference clock signal. In clock recovery applications it is called timing jitter. Jitter is a significant, and usually undesired, factor in the design of almost all communications links. Jitter can be quantified in the same terms as all time-varying signals, e.g., root mean square (RMS), or peak-to-peak displacement. Also, like other time-varying signals, jitter can be expressed in terms of spectral density. Jitter also provides the bit error rate(BER) of the incoming signal.

IV. PARAMETER IN FREQUENCY SYNTHESIZER

A. Rise Time

In electronics, when describing a voltage or current step function, rise time is the time taken by a signal to change from a specified low value to a specified high value. These values may be expressed as ratios or, equivalently, as percentages with respect to a given reference value. In analog electronics and digital electronics[citation needed], these percentages are commonly the 10% and 90% (or equivalently 0.1 and 0.9) of the output step height however, other values are commonly used.

B. Peak Overshoot

The overshoot is the maximum amount by which the response overshoots the steady-state value and is thus the amplitude of the first peak. The overshoot is often written as a percentage of the steady-state value. The peak overshoots must be within Note that the overshoot does not depend on the natural frequency of the system but only on the damping factor. As the damping factor approaches 1 so the percentage overshoot approaches zero.

C. Lock time

The range of frequencies over which PLL will track the input frequency signal and remains locked is referred as PLL Lock range. The lock range is usually band of frequencies above and below the PLL free running frequency as described earlier.

D. Pull-in time

This is the time required to pull-in the signal in the fast locking state when the signal are locking or acquisition time is very slow once the signal comes in the fast locking state then it will lock very fast. Generally pull-in process is very slow.

V. RESULT SCANNING OF SYNTHESIZER

A. Phase Frequency Detector

Phase frequency detector is one of the important parts in PLL circuits. PFD (Phase Frequency Detector) is a circuit that measures the phase and frequency difference between two signals, i.e. the signal that comes from the VCO and the reference signal.

PFD has two outputs UP and DOWN which are signaled according to the phase and frequency difference of the input signal. And the output of pfd is given to charge pump.

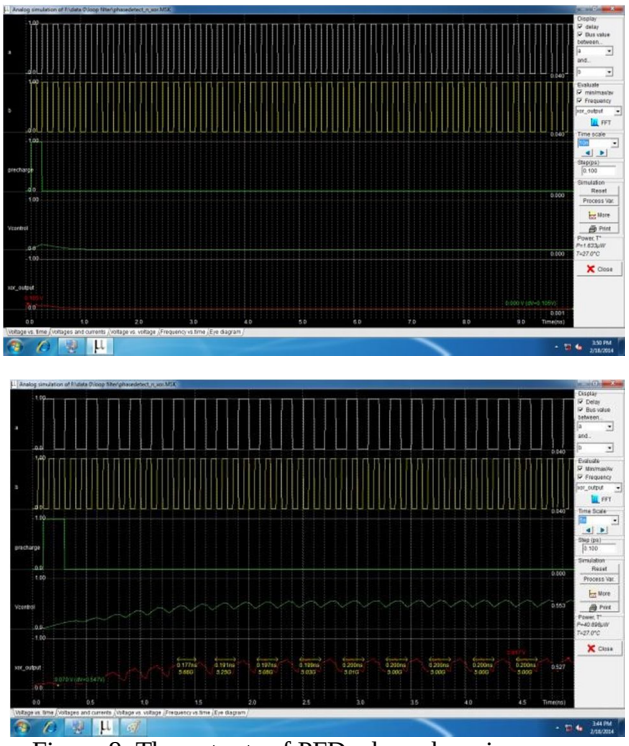


Figure 9: The outputs of PFD when phase is same

B. Charge Pump and Loop Filter

A charge pump is a switch type mode power supply, which creates discrete multiples of the input voltage using a capacitor. In low power electronics at certain conditions, where we have a low voltage say 3.3V, but we require 5V. In order to overcome this situation, we use a boost converter. These converters are inefficient at low powers because they consume lots of power while operating, they are noisy device and does not work in reverse operation. Calculation of various parameters in the circuit is done between the dynamic output of the controlled voltage which is ineffect an output of the second orders closed-loop systems so that the computation is done with this output. From below figure we can observe that the circuit is give rise to an overshoot at few point of time so that from that figure take the value of maximum over-shoot and also sompute the peak time at which the maxima overshoots is landing. By taking this two value calculate the value of damping ratio and natural frequency of oscillation

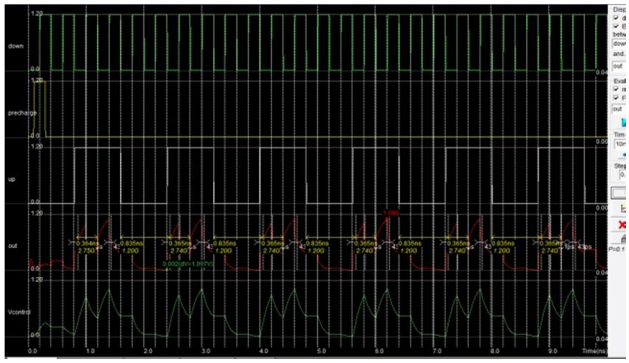


Figure 11: The outputs of Loop filter

C. Voltage Controlled Oscillator

A voltage-controlled Capacitor is one method of making an LC oscillator vary its frequency in response to a control voltage. Any reverse-biased semiconductor diode displays a measure of voltage-dependent capacitance and can be used to change the frequency of an oscillator by varying a control voltage applied to the diode[18]. The centre frequency in this VCO is obtained at the controlled voltage of $V_{DD}/2$.The V_{DD} in this circuit 1.2 volt so the centre frequency is obtained at the controlled voltage.[20]

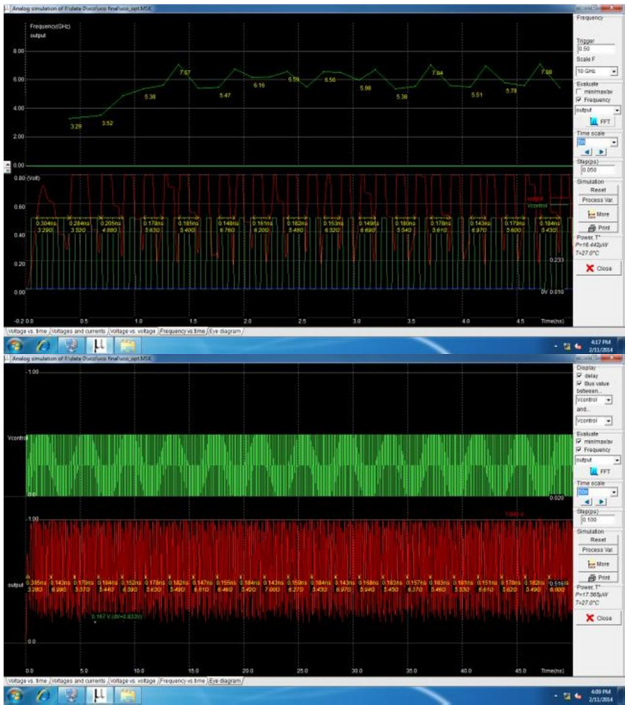


Figure 12: The ouput frequency of Ring Oscillator

D. Multi Modulo Divider

In the propose architectonics we have make the MMD which can divide the clock by 2 with failing edge

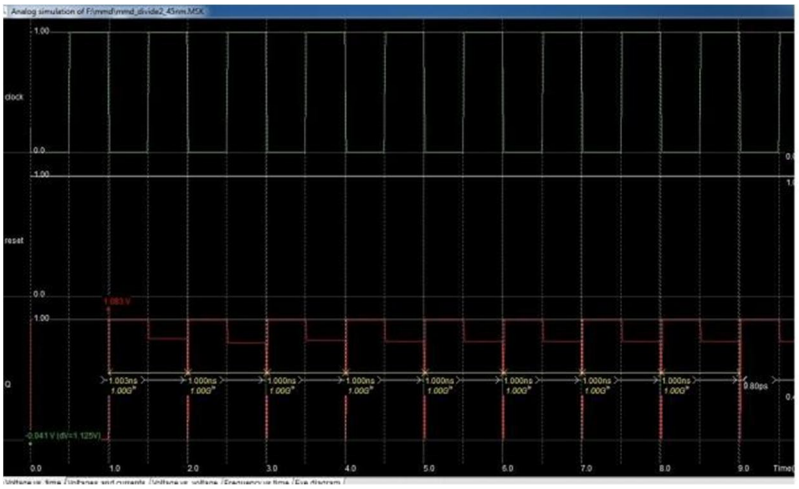


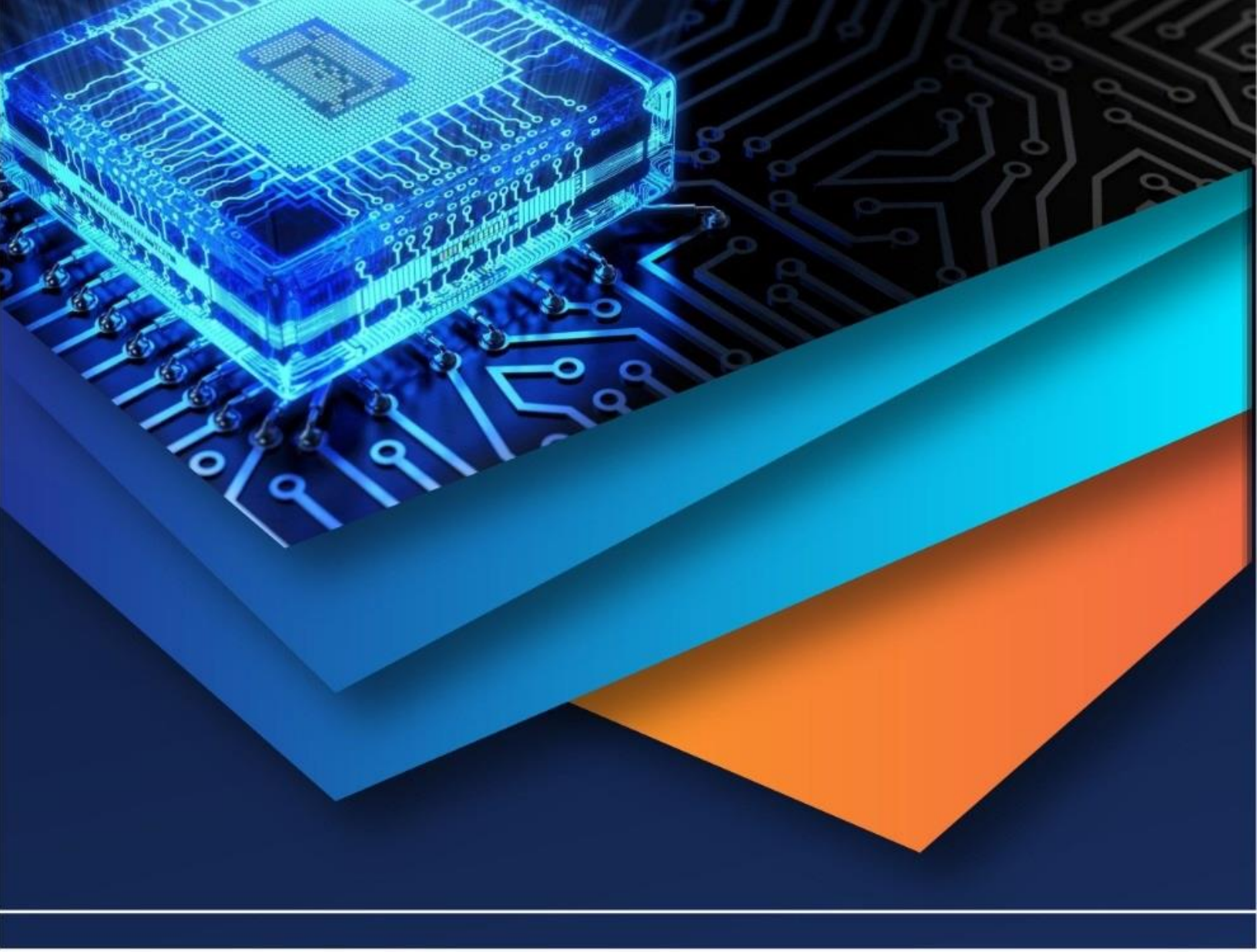
Figure 13: Ouput of MMD

VI.CONCLUSION

A 4 GHz fully integrated frequency synthesizer is introduced . The phase frequency detector determine the linear and the pull-in range of the frequency synthesizer hence the selection of PFDs is crucial in the designing. For fractionally frequency divide the designs of divider circuit is most prime and it additionally determines the range of frequency which can be applied to the frequency synthesizer.

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