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Design and Simulation of Vedic Multiplier Using Verilog HDL

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Abstract: ***This Paper is created for the simulation of a high speed Vedic multiplier. In the proposed paper, the multiplier circuit is designed by using algorithms that involve Vedic Mathematics. Calculations that involve Vedic mathematics are derived from the old contexts known as Vedas. The VHDL programs are synthesized and simulated using Xilinx ISE simulator. The study of Vedic multipliers is done in comparison with the conventional multipliers to find the fact that which multiplier is fast and efficient and the research and analysis has shown that the Vedic multiplier is more efficient than conventional multipliers because of its fast response in digital signal processing and it gives less delay in system logic design. Vedic mathematics used in the Vedic multiplier increases the speed of multiplier as it reduces the number of partial products. Hence, the speed of the overall digital design can be increased by implementing a Vedic multiplier.***

Keywords: Multiplier, Adder; Testbench; RTL, Power Reduction

I. INTRODUCTION

Multipliers are a major part of DSP algorithms that are used in various fields including computer applications and digital system designing. Multiplication is the most fundamental function in an arithmetic operation. Operations that ~~in~~volve multiplications are slower than addition and subtraction hence it is advised to implement a multiplier that performs fast multiplications to increase the speed of the calculation as fast multiplications result in fast calculations. A high-speed multiplier is needed in system and logical design because it decreases the processors time in DSP algorithms and algorithms involving FET. The need for fast multipliers has become significantly important because the computing applications of the computer is expanding day by day. Vedic multiplier is a fast, convenient and logical way of performing calculations that uses Vedic mathematics derived from the ancient contexts known as 'Vedas'. It minimizes the processors time by reducing the number of delays and partial products. Vedic multiplier is preferred over conventional multipliers as it produces minimum number of partial products while performing multiplication operation.

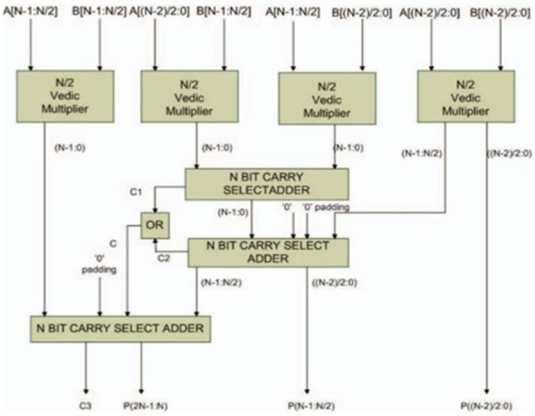
II. METHODOLOGY

The project is implemented using the following tools and software:

1) XILINX ISE SIMULATOR
2) VERILOG HDL
3) URDHVA- TIRYAKBHYAM SUTRA

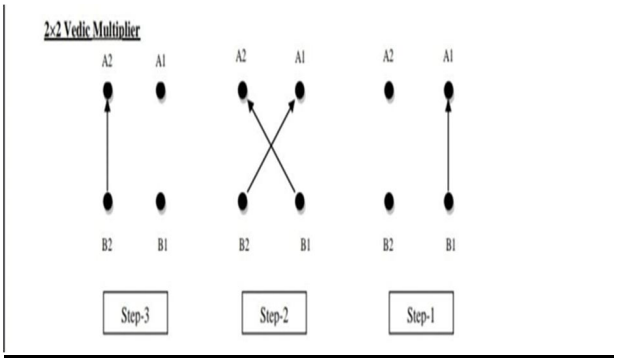
Algorithm-

- Flowchart of NxN Vedic Multiplier Multiplier :



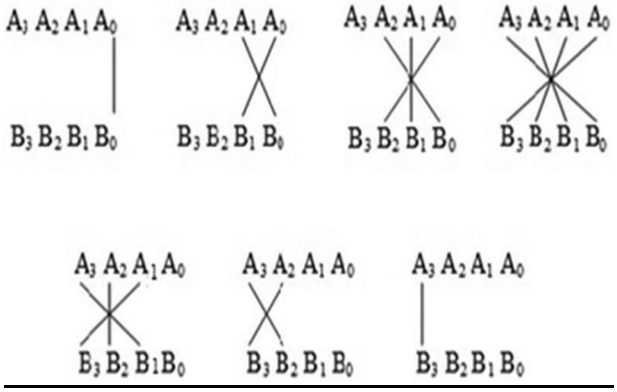
- Block Diagram of 8x8 Multiplier :

- 2x2 Multiplier :



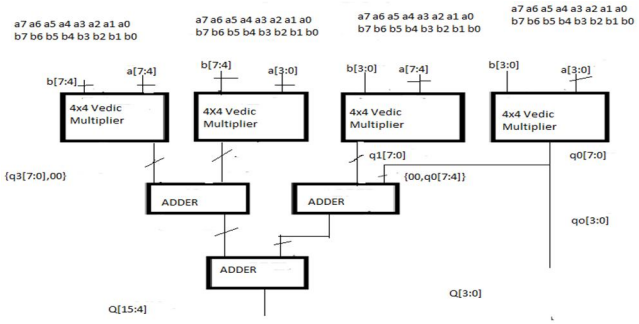
Step 1: A1 x B1 = (multiplying the left side)
Step 3: A2 x B2 = (multiplying the right side)
Step 2: (B2 x A1) + (B1 x A2) = (cross-multiplying both sides)

- 4x4 Multiplier :



4x4 Multiplier is implemented by using 2x2 Vedic Multiplier blocks.

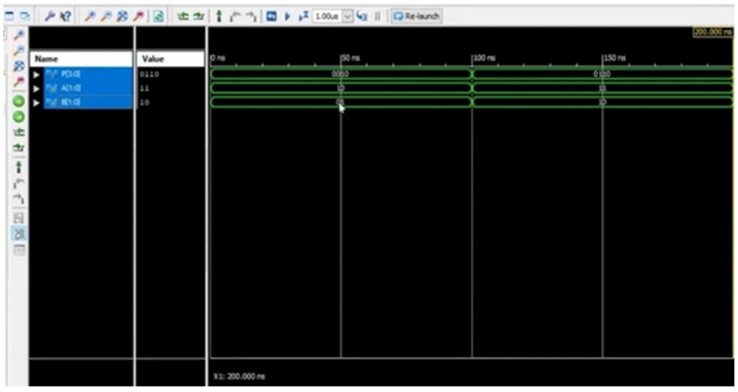
- 8x8 Multiplier :



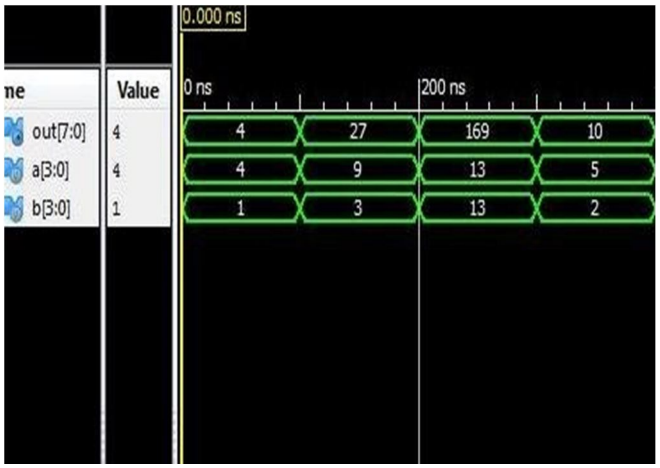
This diagram illustrates the basic structure of the 8x8 Vedic multiplier using four 4x4 multipliers and 12-bit adders. Each 4x4 multiplier performs the multiplication of two 4-bit numbers, and the adders accumulate the partial products to produce the final result.

III. SIMULATION RESULT

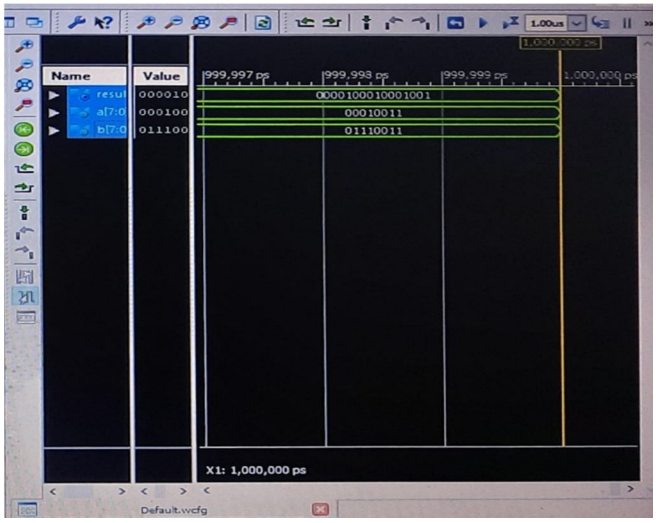
Simulation Result of 2x2 Multiplier on Xilinx ISE Tool:



Simulation Result of 4x4 Multiplier on Xilinx ISE Tool:



Simulation Result of 8x8 Multiplier on Xilinx ISE Tool:



IV. RESULT AND CONCLUSION

1) This implementation is carried out on Spartan-6 board, and the results are displayed on the LCD of the Spartan-6 The Xilinx software has been an effective tool in the modelling of 2x2, 4x4 and 8x8 multipliers based on the principles of Vedic Mathematics, specifically the Urdhvatiryakbhyam sutra. . The multiplier designs are implemented using digital circuits consisting of half adder and full adder circuits.

2) The implementation of vedic multiplier circuits has resulted in fast calculations by decreasing the processors time and delay. The given review paper is an outline of 2x2 and 4x4 vedic multiplier implementation which further lays down the outline of other NxN multipliers.

3) The proposed model of 2-bit and 4-bit and Vedic multiplier uses logic gates and carry adders, resulting in fast response , memory usage, and logic levels when compared to other conventional multipliers. The design is implemented using a carry select adder for performing the calculation of partial products .This vedic multiplier simulation is used for fast multiplications in computer, DSP and FFT applications.

4) The 8-bit Vedic multiplier architecture uses logic gates and carry adders. Together latency, memory usage and logic levels are reduced when compared to the drag coefficient designs.

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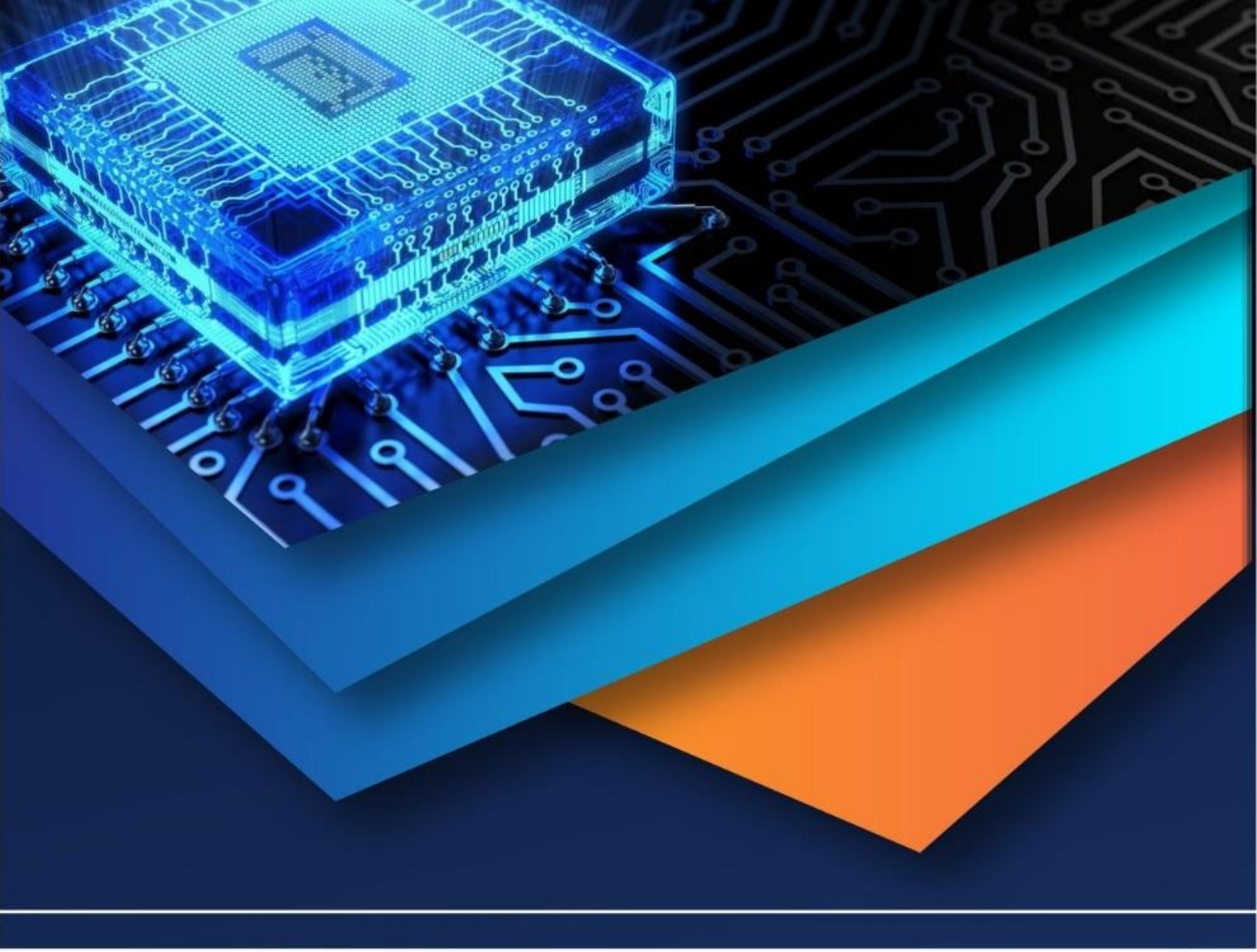

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