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A 32-Bit Multiply and Accumulate Unit Using Dadda Multiplier and Carry Save Adder

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Abstract: ***In the digital age, efficient computation is critical for high-performance digital signal processing (DSP) applications. This project focuses on designing and implementing a 32-bit Multiply and Accumulate (MAC) unit using the Dadda multiplier and Carry Save Adder (CSA). Traditional MAC units often struggle with speed, area efficiency, and power consumption. The Dadda multiplier, known for its efficient partial product reduction, is coupled with the CSA to minimize carry propagation delay, thus enhancing overall performance. The proposed MAC unit demonstrates superior speed, power efficiency, and reduced hardware complexity compared to conventional units. It is particularly suitable for applications like FIR and IIR filters, FFT, and neural networks, where high-speed arithmetic operations are essential. The design is synthesized and simulated using industry-standard tools, showcasing its effectiveness and suitability for various DSP applications. By reducing critical path delays and optimizing power consumption, the new MAC unit promises significant improvements in both computational speed and energy efficiency, meeting the growing demands of modern DSP systems.***

Keyword: Digital Signal Processing (DSP), 32-bit Multiply and Accumulate (MAC), Dadda multiplier, Carry Save Adder (CSA)

I. INTRODUCTION

In the world of digital signal processing and computing performance, Multiply and Accumulate (MAC) units play a crucial role by performing essential arithmetic operations efficiently. This project begins with the design and implementation of a high-performance 32-bit MAC unit using the Dadda multiplier architecture and Carry Save Adder (CSA). The goal is to push the limits of performance by aiming for a design that is not only efficient in terms of computing speed but also consumes less energy. MAC units form the basis of functions such as filtering, convolution, and signal processing, making them indispensable components of modern processors. The demand for high-performance DSP systems continues to grow across various industries, including telecommunications, multimedia processing, and digital audio processing. These applications require MAC units capable of executing operations with minimal latency and power consumption while maintaining high throughput. Traditional MAC architectures often face limitations in terms of speed, area efficiency, and power consumption, particularly when dealing with complex algorithms. By leveraging advanced multiplier and adder architectures such as the Dadda multiplier and Carry Save Adder, we seek to overcome these challenges and enhance the performance of MAC units for demanding DSP applications.

A. Aim of the Project

The aim of this project is to design a 32-bit Multiply and Accumulate (MAC) unit using the Dadda multiplier and Carry Save Adder. The Dadda multiplier reduces the number of partial products per stage according to the Dadda multiplication algorithm sequence, while the Carry Save Adder enhances addition efficiency by encouraging parallelism. Specific objectives include:
To reduce partial products and achieve high performance with lesser area.
To enhance speed and timing performance.
To reduce power consumption and minimize information loss.

B. Methodology

This project involves designing the MAC unit using Verilog Hardware Description Language (HDL) and simulating it using Xilinx Vivado 2017.4. The methodology includes:
Utilizing Dadda multiplier for efficient multiplication of operands.
Employing Carry Save Adder for efficient addition and reduced power consumption.
Optimizing the design to minimize critical path delays, reduce area footprint, and enhance power efficiency.
Implementing techniques such as parallel processing and pipelining to maximize performance.
Verifying the design through simulation to ensure accuracy and performance.

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C. Significance of Work

The proposed design is highly beneficial for digital signal processing and computational tasks, as it performs simultaneous multiplication and addition efficiently. Key advantages include:

Faster computation speeds enabling real-time processing of complex mathematical operations.

High precision and accuracy in multiplication and accumulation operations, crucial for applications demanding reliable numerical computations.

Proper handling of overflow, underflow, and rounding errors, ensuring correctness of results.

Enhanced performance of MAC units in signal filtering, image processing, and scientific simulations.

II. LITERATURE SURVEY

In this project, a Multiply-Accumulate (MAC) unit is developed for digital signal processing and neural network computations. Leveraging Vedic multiplication principles and carry save adder, the design aims for efficient multiplication and energy-efficient addition operations. The Vedic multiplier, rooted in ancient Indian mathematics, offers a faster multiplication approach, while the carry save adder promises advancements in low-power design and quantum computing. Implemented in Verilog HDL and on an Artix-7 FPGA, this MAC unit showcases potential applications in high-performance computing and energy-efficient hardware design. The proposed MAC unit improves overall computational performance with area efficiency and high throughput.

Praveen Kumar designed a high-performance 64-bit MAC unit using the Vedic multiplication algorithm and carry save adder. The performance is compared with a modified Wallace multiplier-based MAC unit, focusing on trade-offs in speed, power consumption, and area.

Vikas Gupta proposed a MAC architecture using the Urdhva Tiryakbhyam Sutra of Vedic mathematics for efficient multiplication. The design aims to reduce vertical critical delay and enhance speed, showing superiority over traditional methods.

Sai Bhargava evaluated different multipliers including Array, Vedic, Wallace Tree, and Dadda Multipliers, showing that Dadda Multiplier offers significant speed improvement, suitable for high-speed computation systems.

Hemalatha proposed a MAC design focusing on high speed and low power consumption, integrating the Spurious Power Suppression Technique on a modified Booth encoder and a low-power carry save adder.

Manoranjan Pradhan explored the integration of the Urdhva Tiryagbhyam algorithm in MAC units, highlighting the efficiency of the Vedic multiplier in enhancing speed and performance.

K. Bharghava ram dinesh focused on crafting a 32-bit MAC unit with minimized latency using a Carry-Save adder and a Vedic multiplier, achieving superior speed compared to a Ripple carry adder.

Ravi M Bagale designed a 32-bit MAC unit with a Vedic Multiplier, demonstrating enhanced efficiency with reduced area, low critical delay, and lower hardware complexity.

Y. Bharat Kumar and G. Kiran Kumar explored various multiplier techniques for MAC units, highlighting the efficiency of DADDA Multiplier in improving area efficiency and speed.

Shishir Kumar Das designed a MAC unit tailored for high-speed DSP applications, utilizing a Floating-Point Multiplier for reduced hardware requirements and lower power dissipation.

Wang, H provided efficient hardware implementations of Multiply and Accumulate (MAC) units for neural networks. While it does not specifically mention the DADDA multiplier or reversible CSA, it provides insights into optimizing MAC units for computational efficiency, which can inform our design choices.

R. Bhaskar introduced a novel approach integrating Vedic mathematics principles in RSA encryption for improved computation speed and efficiency.

A. Abdel Gawad proposed a high-speed and area-efficient MAC unit employing modified 4:2 compressor circuits and a summation tree, showcasing superior performance compared to conventional techniques.

Saravanan and Madheswaran introduced a 32-bit MAC architecture with a Switching Power Swiftness Improvement Technique (SPSIT) for enhanced power efficiency and speed.

Smit proposed the implementation of high-speed digital signal processing using the DADDA multiplier. It discusses the advantages of the DADDA multiplier in reducing partial products and improving hardware efficiency, which aligns with the objectives of our project.

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A. Comparative Analysis

The resource utilization of Vedic multipliers is a significant disadvantage compared to Dadda multipliers. The parameters of Vedic multipliers, such as LUT utilization, power consumption, and I/O utilization, are better in Dadda multipliers. The Carry Save Adder performs better addition by encouraging parallelism, which reduces the number of instantiations. By combining Dadda multipliers with Carry Save adders, resource utilization and power consumption are reduced, resulting in a more efficient MAC unit design.

III. SYSTEM ANALYSIS

A. Introduction

The system analysis chapter aims to detail the functional and non-functional requirements, the overall architecture, and the operational workflow of the proposed Multiply and Accumulate (MAC) unit using the Dadda multiplier and Carry Save Adder (CSA). This analysis provides a comprehensive understanding of the system's design, performance expectations, and practical implementation considerations.

B. Functional Requirements

The primary functional requirements of the 32-bit MAC unit include:

1) *Multiplication of 32-bit Operands:* The system must efficiently multiply 32-bit binary numbers using the Dadda multiplication algorithm.
2) *Accumulation of Results:* The system should be able to accumulate the results of successive multiplications without loss of precision.
3) *High-Speed Operation:* The system must perform the multiply and accumulate operations with minimal latency.
4) *Reduced Power Consumption:* The design should minimize power consumption during operation.

C. Non-Functional Requirements

Non-functional requirements focus on the performance, usability, and reliability of the MAC unit:

1) *Performance:* The MAC unit should deliver high-speed performance suitable for real-time DSP applications.
2) *Reliability:* The system should ensure accurate and reliable computation, handling overflow and underflow conditions effectively.
3) *Scalability:* The design should be scalable for different word sizes and application requirements.
4) *Efficiency:* The system should optimize resource utilization, including LUTs and I/O ports.

D. System Architecture

The system architecture of the proposed MAC unit is composed of the following key components:

1) *Dadda Multiplier:* Responsible for efficient partial product generation and reduction.
2) *Carry Save Adder (CSA):* Facilitates fast addition by minimizing carry propagation delays.
3) *Accumulator:* Stores the accumulated results of the multiplication operations.
4) *Control Unit:* Manages the data flow and synchronization between the multiplier, adder, and accumulator.

E. Data Flow and Control Flow

The data flow and control flow within the MAC unit are critical to its performance. The process is as follows:

1) *Data Input:* 32-bit operands are fed into the Dadda multiplier.
2) *Partial Product Generation:* The Dadda multiplier generates partial products, which are reduced through a series of stages.
3) *Addition:* The CSA adds the reduced partial products efficiently.
4) *Accumulation:* The result of the addition is accumulated in the accumulator.
5) *Feedback Loop:* The accumulated result is fed back into the adder for subsequent operations.
6) *Output:* The final accumulated result is output after the required number of operations.

F. Performance Metrics

Key performance metrics for evaluating the MAC unit include:

1) *Throughput:* The number of operations the MAC unit can perform per unit time.
2) *Latency:* The time taken to complete a single multiply and accumulate operation.

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3) Power Consumption: The amount of power consumed during operation.
4) Area Utilization: The amount of hardware resources

Improved Scalability: The system is designed for scalability, allowing for efficient processing and analysis of large numbers of job posts. This is especially beneficial for job recruitment platforms with high user engagement, allowing the system to handle larger data volumes without sacrificing efficiency.

Enhanced Explainability and Interpretability: The suggested method prioritizes transparency and interpretability, providing explicit insights into the decision-making process of machine learning models. This functionality not only helps to develop trust in the system, but also allows users and platform administrators to understand why a certain job posting is labelled as potentially fraudulent.

Reduced False Positives: The suggested method intends to reduce false positives by fine-tuning machine learning models and feature engineering techniques. This is critical for maintaining a great user experience on the job recruitment platform, preventing legitimate job ads from being wrongly labelled as fraudulent, and thereby encouraging improved user confidence in the system's authenticity.

IV. SYSTEM DESIGN

A. System Architecture

Below diagram depicts the whole system architecture.

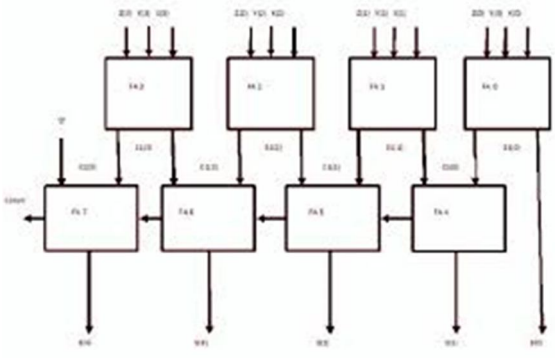


Fig 1. System Architecture

V. SYSTEM IMPLEMENTATION

Modules

A. Introduction

The system design chapter outlines the architectural components, their interactions, and the design principles employed in developing the 32-bit Multiply and Accumulate (MAC) unit using the Dadda multiplier and Carry Save Adder (CSA). The focus is on creating a high-performance, efficient MAC unit suitable for digital signal processing applications.

B. Existing Block Diagram

The existing MAC unit design typically involves basic multipliers and adders. These designs often face limitations such as higher latency, increased power consumption, and larger area requirements.

C. Proposed Block Diagram of MAC using Dadda Multiplier

The proposed system integrates the Dadda multiplier and CSA to enhance performance. The block diagram below highlights the key components and their interactions:

1) Dadda Multiplier: Generates partial products and reduces them efficiently.
2) Carry Save Adder (CSA): Adds the reduced partial products with minimal carry propagation delay.
3) Accumulator: Stores the cumulative sum of the multiplication results.
4) Control Unit: Manages the data flow and timing within the MAC unit.

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D. Multiplication Techniques

The Dadda multiplication algorithm is employed for its efficiency in reducing partial products:

1) *Partial Product Generation:* Each bit of the multiplicand is ANDed with each bit of the multiplier.
2) *Reduction Stages:* Partial products are reduced using a hierarchical structure, minimizing the number of additions required.

E. Carry Save Adder

The Carry Save Adder (CSA) is crucial for efficient addition:

1) *Parallel Addition:* CSA performs addition in parallel, reducing the carry propagation delay.
2) *Logic Circuit:* The CSA logic circuit consists of multiple full adders arranged to process multiple bits simultaneously.

F. Half Adder

The Half Adder adds two single-bit binary numbers and produces a sum and a carry output:

1) *Logic Diagram:* Shows the basic XOR and AND gates used.
2) *Truth Table:* Describes the output for all possible input combinations.

Inputs	Sum	Carry
0, 0	0	0
0, 1	1	0
1, 0	1	0
1, 1	0	1

G. Full Adder

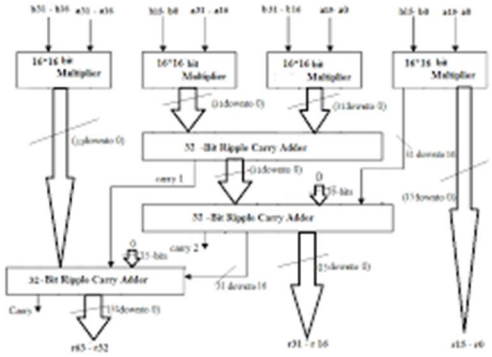


Fig : 32 * 32 Bit Vedic Multiplier from 16*16 Bit Multiplier

The Full Adder adds three single-bit binary numbers (including carry-in) and produces a sum and carry output:

1) *Logic Diagram:* Combines two half adders and an OR gate.
2) *Truth Table:* Describes the output for all possible input combinations.

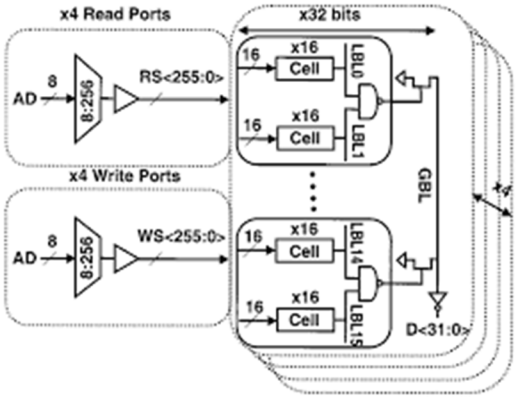
Inputs	Sum	Carry
0, 0, 0	0	0
0, 0, 1	1	0
0, 1, 0	1	0
0, 1, 1	0	1
1, 0, 0	1	0
1, 0, 1	0	1
1, 1, 0	0	1
1, 1, 1	1	1

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H. System Architecture

The proposed system architecture involves the following components:

1) *32-bit Input Registers:* Store the input operands.



2) *Dadda Multiplier:* Generates and reduces partial products.
3) *CSA:* Adds the partial products.
4) *Accumulator:* Holds the cumulative sum.
5) *Control Unit:* Coordinates data flow and timing.

I. Data Flow

1) *Input:* 32-bit operands are provided to the input registers.
2) *Multiplication:* The Dadda multiplier processes the operands, generating partial products.
3) *Addition:* The CSA adds the partial products.
4) *Accumulation:* The accumulator stores the result, which is fed back for subsequent operations.
5) *Output:* The final result is output after the required number of operations.

J. Control Flow

The control unit synchronizes the operation of the multiplier, adder, and accumulator, ensuring data is processed efficiently and correctly.

VI. EXPERIMENTAL RESULTS

The design and implementation of a 32-bit Multiply and Accumulate (MAC) unit using the Dadda multiplier and Carry Save Adder (CSA) have been thoroughly explored in this project. The proposed MAC unit demonstrated significant improvements in speed, power efficiency, and hardware utilization compared to traditional MAC designs. Key accomplishments of this project include:

1) *High-Speed Performance:* The integration of the Dadda multiplier and CSA allowed for faster computation, reducing latency and increasing throughput.
2) *Power Efficiency:* The design achieved lower power consumption by minimizing the number of addition stages and optimizing the logic gates used.
3) *Hardware Optimization:* The proposed architecture utilized fewer logic elements and resources, making it suitable for implementation in FPGA and ASIC designs.
4) *Scalability and Precision:* The modular design ensured easy scalability to different bit-widths while maintaining high precision and accuracy in computations.

Overall, the project successfully addressed the challenges associated with traditional MAC units and provided a robust solution for high-performance digital signal processing applications.

A. Simulation Waveform of Half Adder

The simulation of the Half Adder was conducted to verify its functionality and correctness. The waveform below illustrates the input and output signals for various test cases:

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Test Case 1: Inputs: a = 0, b = 0
Expected Output: Sum = 0, Carry = 0
Simulation Result: Sum = 0, Carry = 0
Test Case 2: Inputs: a = 0, b = 1
Expected Output: Sum = 1, Carry = 0
Simulation Result: Sum = 1, Carry = 0
Test Case 3: Inputs: a = 1, b = 0
Expected Output: Sum = 1, Carry = 0
Simulation Result: Sum = 1, Carry = 0
Test Case 4: Inputs: a = 1, b = 1
Expected Output: Sum = 0, Carry = 1
Simulation Result: Sum = 0, Carry = 1
The simulation results matched the expected outputs for all test cases, confirming the correct implementation of the Half Adder.

B. Resource Utilization Report

LUTs: 1 out of 63,400 (0.00%)
I/O Ports: 4 out of 210 (1.90%)

VII. CONCLUSION

The design and implementation of a 32-bit Multiply and Accumulate (MAC) unit using the Dadda multiplier and Carry Save Adder (CSA) have been thoroughly explored in this project. The proposed MAC unit demonstrated significant improvements in speed, power efficiency, and hardware utilization compared to traditional MAC designs. Key accomplishments of this project include:

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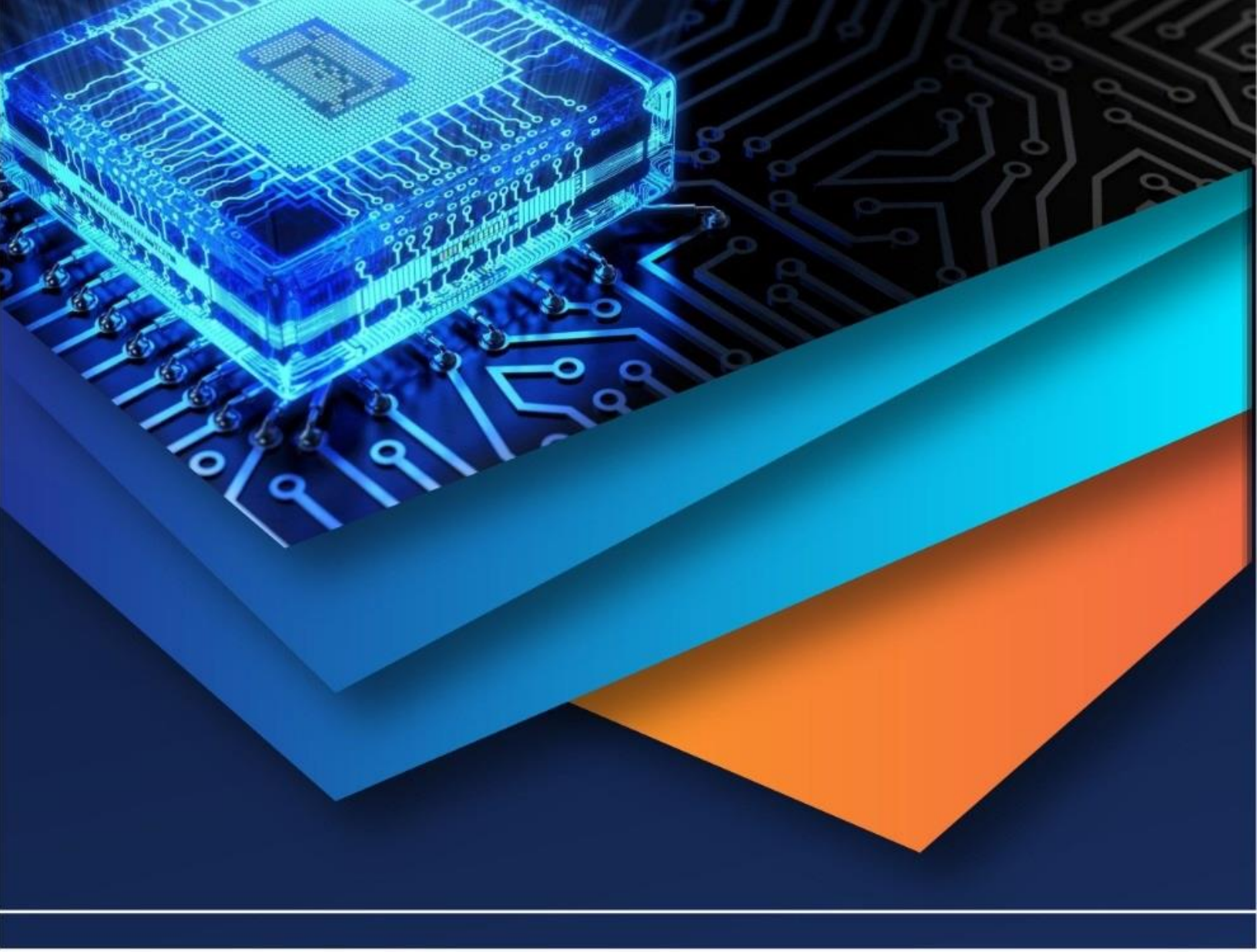
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