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A Comprehensive Analysis on Level Shifters: Challenges, Opportunities, and Future Directions

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Abstract: ***Level shifter has an important role in low power circuits useful in electronic gadgets such as smartphones, tablets, laptops and many other. Basically, level shifters are used to convert voltage levels from lower to higher or higher to lower. Low power dissipation is a major challenge in level shifter circuits. Along with power dissipation this paper includes comparison on delay and voltage range of various level shifter configurations. There is need for level shifter with minimum delay and higher speed which the existing level shifters are lacking from. Modified conventional level shifter shows better performance, consuming less power and has a less delay, making it suitable for applications such as IoT, battery powered devices, wireless networks etc.***

Keywords: Level Shifters, Power dissipation, delay and Conventional Level Shifters.

I. INTRODUCTION

Level shifters act as bridges to signals. They basically convert signals for the devices so that it can communicate with all the parts. When designing a level shifter, it is important to see the 3 major things, that is power delay and voltage variations [1] a per our survey discussion. Dynamic voltage level shifter is a circuit that will adjust the output voltage according to the given input voltage. This will change dynamically to save the power. It will consider the input conditions to avoid any power loss in the circuit. The LS shifts up when input is low voltage and LS shifts down when in need. This LS shows the power efficient circuits [2].

As the CMOS Technology is getting better LS circuits are also improving This makes the new designs to focus more on reducing the unwanted power loss and delay in the circuit. [3]. Level Shifters are differentiated based on how they work, how they are designed using the CMOS Technology. [4]. The circuit is designed to reduce the damage in the circuit so the voltages are within certain limits [5]. Some of LS uses Multi Threshold Voltage. This has transistors with different voltage thresholds. Topological modifications are also done in the circuit so that it can operate for wide range of voltages [6]. In present there is use of dynamic voltage scaling while dealing with two power supplies. This saves the power and also maintains the performance depending on the need [8]. There can be seen new LS with current mirrors that reduces the power loss and also works very effectively [9].

Modifies SSLS converts low input voltage to high output voltage. There is less requirement of any extra pins, therefore reducing the routing congestion. This design has 2 extra NMOS transistors which reduces the leakage current and power absorption [11]. Bootstrapping NVLS is designed for both voltage shifts that is positive and negative. Bootstrapping switch is used to increase and improve the input impedance along with switching. Leakage current is reduced as there is not shortest path considered [20].

II. PROPOSED METHODOLOGIES

A. Level Shifter Designs

1) Modified Conventional Level Shifters (CLS)

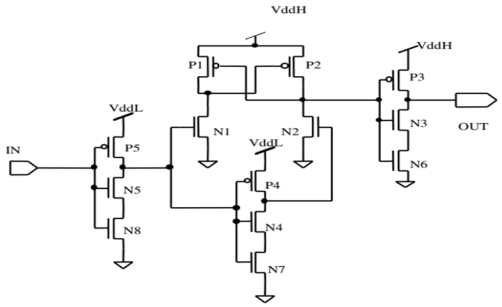

Figure 1 Modified Conventional LS

Fig.1 shows Conventional LS with three additional NMOS transistors [N6, N7, N8]. NMOS transistors works the circuit for low voltage and can handle wide range of voltage. This basically lets the logic signals to switch fast and reduce the delay. Even the power loss is also reduced. When the circuits works with low input then PMOS transistor is turned ON and VOUT is made high. In the other case the NMOS is turned ON and VOUT is made LOW. Stacking NMOS will basically reduce sub - threshold leakage [11].

2) Dynamic Voltage Level Shifters (DVLS)

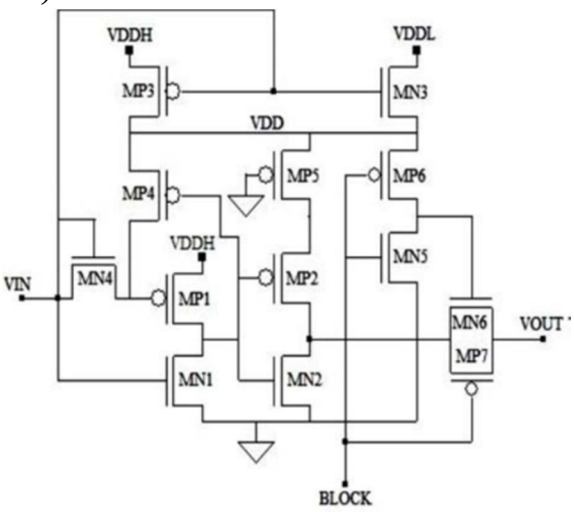

Figure 2 Dynamic voltage LS

Fig.2 shows Dynamic voltage LS having provision to block the data, it is capable of performing both level up shift and level down shift with input voltage. During level up shifting transistor MP3 turns ON. VOUT is charged to high VDDH through transmission gate. During level down shifting MN3 turns ON and VOUT is discharged to 0.4V. In Blocking mode MP3 turns ON and VDDH is takes as the supply and VOUT is discharged to 0V [2].

3) Modified Single Supply Level Shifter (MSSLS)

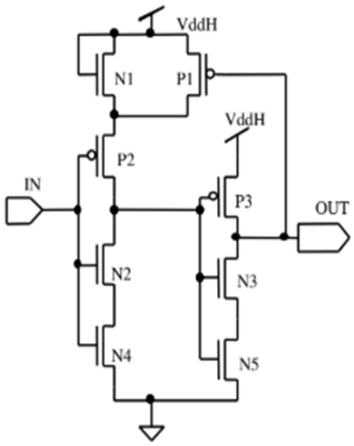

Figure 3 Modified Single supply LS

Fig.3 shows Modified single supply LS that has two NMOS transistors which is additional [N4, N5]. These additional transistors are stacked so that voltage is distributed across multiple devices, it also helps in leakage current reduction and enhanced voltage swing. When the input is low pull up PMOS transistor turns ON pulling VOUT high. During low input pull down NMOS turns ON and VOUT is low. Stacking technique reduces the sub threshold leakage and keeps the output voltage level consuming less power [11].

4) Bypass Enabled Level Shifter (BELS)

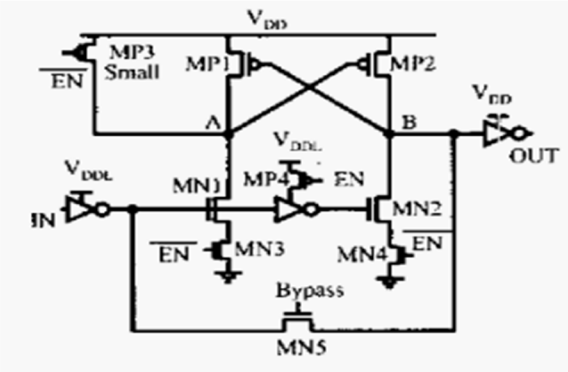

Figure 4 Bypass Enabled LS

Fig.4 shows Bypass Enables LS having additional two PMOS and three NMOS transistors compared to conventional LS. It has two modes 'BYPASS' and 'SHIFT' that helps in voltage conversion. When VDD is at high voltage BELS works in SHIFT mode. It reduces contention at node B, enabling quick logic switching When VDD is low BELS works in BYPASS mode. EN signal is set to VDDH which turns off unused transistors [13].

5) Bootstrapping Negative Voltage Level Shifter (BNVLS)

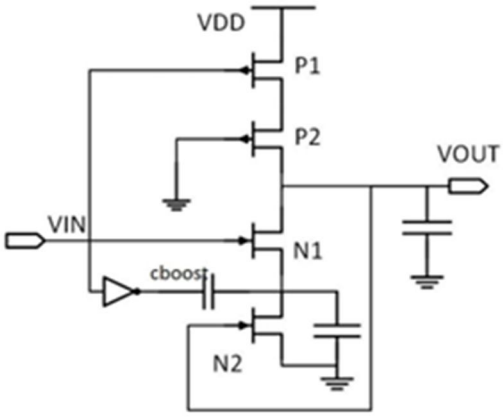

Figure 5 Bootstrapping Negative Voltage LS

Fig.3 shows Bootstrapping negative voltage level shifter, in this technique Cboost capacitors increases impedance of the particular circuit so that voltage LS driving capability increases. Along with cboost capacitors, parasitic and load capacitors are also used. In the case of low to high transition N1 is turned OFF and P1 is turned ON. This basically forces the output voltage to charge up to VDD. When there is high to low transition input is high and N1 is turned ON and output node will be discharged to zero. N2 is turned OFF. The Cboost value is set in the range of 1pf to 100pf for a supply voltage of 1V [20].

B. Comparative Analysis

Table 1

Design	Power	Delay	Voltage
MCLS	402.2264pW	2.3376ns	3.3V & 2.2V [11]
BNVLS	1.16nW	12.82ns	0.7 V – 1.2V [20]
BELS	398uW	350ps	0.7 – 3.3V [13]
MSSLS	108.641pW	2.564ns	3.3V – 1.6V [11]
DVLS	20.9nW	5.6ns	0.4V –1V [2]

III. RESULTS AND DISCUSSION

Bootstrapping technique has higher efficiency which increases the driving capability and also reduces power dissipation. Compared to Convention LS this ha low Propagation delay. Instead of using two circuit, a single circuit can be used for the working [20].
There is a power reduction in BYPASS mode up to 50% that eliminates the contention problems. This also eliminates voltage shifting when not required [13]. Voltage selection is done automatically in DVLS which reduces additional control circuits. This LS is faster than the conventional LS. The output is displayed when needed [2]. Stacking technique reduces power leakage but keep the same voltage range operation. This is observed in Modified single supply level shifter and modified conventional level shifter [11].

IV. RESEARCH GAPS & FUTURE SCOPE

The requirement for sub-threshold voltage level shifters is ever-increasing for IoT and biomedical applications [1]. More study needs to be carried out for LS architectures that are efficient under ultra-low voltage operation, such as 100mV, for biomedical and Internet of things applications [12]. Some study is needed to optimize both power and speed, particularly for high-speed communication applications [5]. The requirement is to bring in newer designs that stress upon very minimum delay, while the power consumption remains efficient [3]. Large LS designs still have a lot of power and delay concerns, and these problems can be sorted out using scaling of transistors and improving design techniques for reduction and efficiency [1]. Most of the existing designs have been suffering with the problem of high sensitivity to process-voltage-temperature (PVT) variations. Future researches would, therefore, need focus on self-adaptive LS circuits [15]. The overhead area in complex LS designs remains a source of concern. Optimizing transistor sizing and layout techniques can improve area efficiency [1]. Seeking hybrid LS techniques that can combine differential and bootstrapping mechanisms would further take the power efficiency and speed to greater heights [6].

V. CONCLUSION

DVLS provides the best dynamic voltage which can be used in multi – voltage systems [2]. Modified Single supply LS has the low power consumption which is used in IOT devices and battery – powered systems [11].
Modified Convention level shifter has the lowest delay which is used in low power digital IC and portable devices [13]. BELS has the fastest delay which makes it applicable for high-speed application. But the power consumption is high that is not suitable for ultra-low power designs. This also has broader voltage range [13]. Slowest performance can be seen in BNVLS due to the highest delay which is less useful for Low- voltage energy efficient circuits [20].

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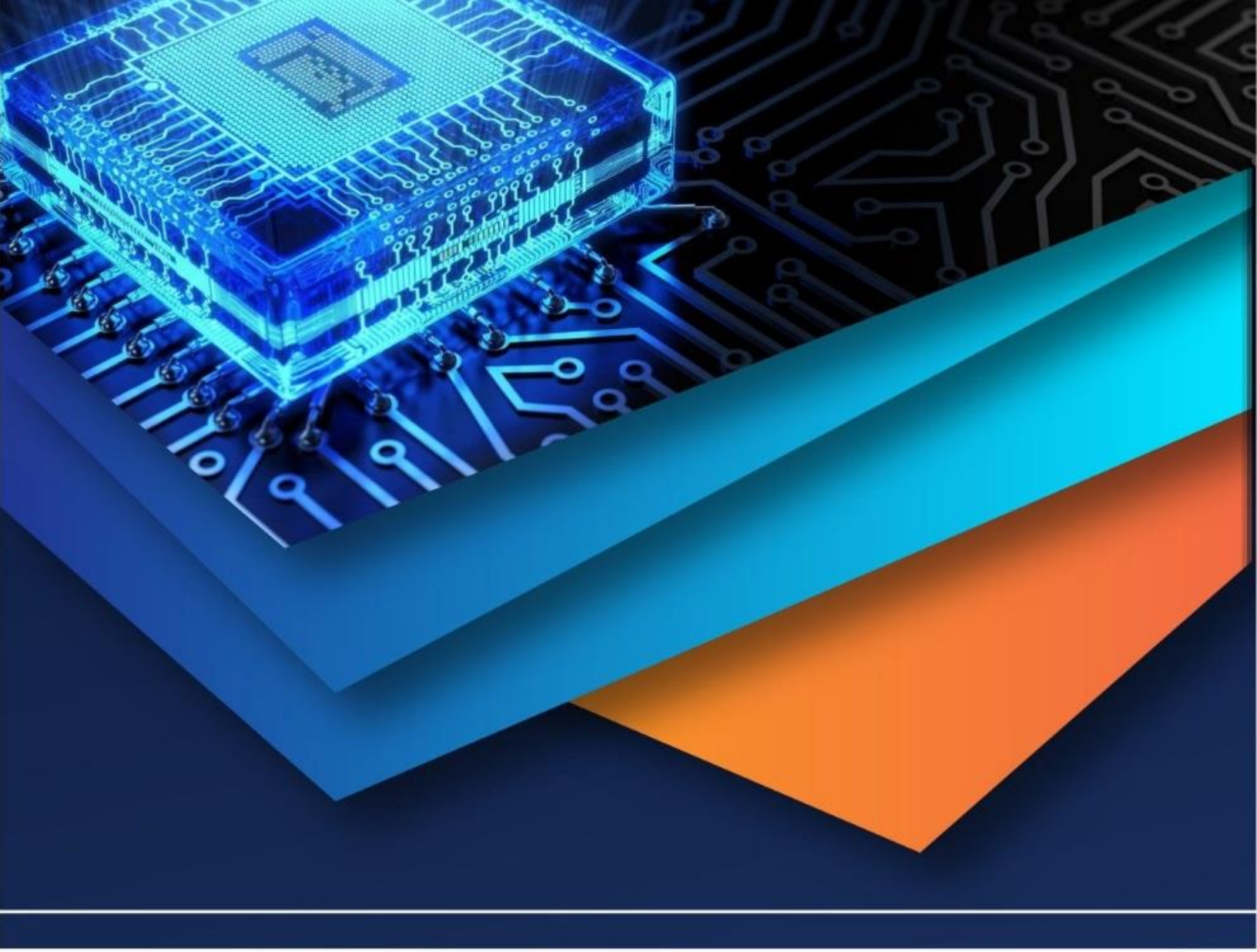

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