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A Hybrid PTL-TGL 4:1 Multiplexer with MTCMOS Power Gating for Energy-Efficient VLSI Systems

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Abstract: ***The increasing impact of power dissipation and leakage current in deep-submicron CMOS technologies has become a major challenge in the design of portable and battery-powered VLSI systems. This paper presents the design and optimization of a 4:1 multiplexer based on a hybrid Pass Transistor Logic (PTL) and Transmission Gate Logic (TGL) architecture integrated with the Multi-Threshold CMOS (MTCMOS) power-gating technique to improve energy efficiency. In the proposed design, PTL is employed to reduce the transistor count and propagation delay, while TGL is incorporated to ensure full voltage swing and maintain reliable signal transmission. To further reduce standby power consumption, a high-threshold sleep transistor is introduced through the MTCMOS technique, enabling effective isolation of the logic circuit from the power supply during inactive operation. The proposed architecture is designed and simulated using Tanner EDA tools with 90 nm CMOS technology. Simulation results demonstrate a significant reduction in leakage power while introducing only a minimal delay overhead compared with conventional 4:1 multiplexer designs. The combined advantages of hybrid PTL–TGL logic and MTCMOS power gating provide an effective balance between power efficiency and circuit performance, making the proposed architecture a suitable solution for modern low-power and high-speed VLSI applications.***

Keywords: Low-power VLSI, 4:1 Multiplexer, Pass Transistor Logic (PTL), Transmission Gate Logic (TGL), Multi-Threshold CMOS (MTCMOS), Leakage Power Reduction, Power Gating, 90 nm CMOS.

I. INTRODUCTION

The growing demand for energy-efficient Very Large Scale Integration (VLSI) systems has made low-power circuit design a significant area of research in modern semiconductor technology. Power optimization can be achieved at multiple levels of VLSI design, including architectural design, circuit implementation, physical layout, and fabrication process technology. Among these approaches, circuit-level optimization plays a crucial role, as the selection of an appropriate logic style for designing combinational circuits directly affects key performance parameters such as power consumption, switching activity, load capacitance, propagation delay, and short-circuit current.

Different logic design techniques exhibit different advantages depending on the application requirements, circuit complexity, and performance constraints.

Therefore, selecting a universally optimal logic style is challenging, as the trade-off between power, speed, and area varies for different design conditions. The continuous scaling of CMOS technology has further intensified the need for efficient logic architectures capable of minimizing energy consumption while maintaining reliable operation.

Energy dissipation has become one of the major concerns in advanced electronic systems. The fundamental relationship between information loss and energy consumption was introduced by R. Landauer in 1960 through Landauer's principle. According to this principle, the irreversible loss of one bit of information results in a minimum energy dissipation of $kT\ ln(2)$ joules, where k represents Boltzmann's constant and T represents the absolute temperature in Kelvin. Conventional irreversible logic circuits dissipate energy during computation due to the loss of information, which is consistent with the second law of thermodynamics stating that lost information cannot be recovered without additional energy expenditure.

This work focuses on the analysis and comparison of a 4:1 multiplexer implemented using different logic styles. The performance evaluation is carried out using Tanner EDA Tool v16.1, considering important design parameters to identify an efficient logic approach for low-power VLSI application.

II. LITERATURE SURVEY

Multiplexers (MUXes) are fundamental components in digital datapaths, used to select one input from multiple signals and route it to a single output. They are widely employed in arithmetic logic units, register files, data buses, and control circuits. In modern system-on-chip (SoC) designs, particularly for mobile and embedded applications, power efficiency has become a major design objective. Since multiplexers are replicated across wide datapaths, they contribute significantly to dynamic power consumption, short-circuit current, leakage power, and propagation delay. Therefore, optimizing MUX structures for low power, reduced area, and high speed can considerably improve overall system performance and energy efficiency.

The Gate Diffusion Input (GDI) technique was introduced as a power-efficient alternative to conventional CMOS logic. A basic GDI cell uses a common gate input for both PMOS and NMOS transistors, while their source terminals receive separate inputs. This structure enables the implementation of several logic functions using only two transistors, thereby reducing transistor count, switching activity, silicon area, and dynamic power consumption. However, practical implementation of GDI requires careful body-biasing and is generally more suitable for twin-well or triple-well CMOS technologies. Despite these challenges, reported studies indicate that GDI-based multiplexers can achieve substantial reductions in power consumption and area compared with standard CMOS implementations.

Pass Transistor Logic (PTL) is another low-power design style in which MOS transistors act as switches to transfer logic signals directly between circuit nodes. By avoiding complementary pull-up and pull-down networks, PTL reduces transistor count, capacitance, and switching power. However, PTL suffers from threshold voltage degradation, particularly when an NMOS transistor passes a logic high level, which can reduce noise margins and slow signal transitions. To overcome this limitation, level-restoring circuits, weak pull-up transistors, or hybrid transmission-gate structures are often employed. Although these additions slightly increase hardware complexity, PTL remains an attractive option for compact and energy-efficient multiplexer designs.

Transmission Gate (TG) multiplexers use parallel NMOS and PMOS transistors controlled by complementary signals, allowing full rail-to-rail signal transmission without threshold voltage loss. As a result, TG MUXes provide excellent signal integrity, balanced rise and fall times, and reliable operation in critical datapath applications. However, they require a higher number of transistors and additional inverter circuitry for complementary control signals, leading to increased area and dynamic power consumption. Despite these drawbacks, their robustness and compatibility with standard CMOS processes make them widely used in commercial digital designs. Comparative studies of GDI, PTL, and TG multiplexer implementations have evaluated their performance in terms of power, delay, area, and signal integrity. GDI and PTL designs generally offer lower dynamic power and reduced transistor count, while TG multiplexers provide superior output voltage swing and reliability. However, several reported works are limited to schematic-level simulations and do not fully consider post-layout parasitics, process variations, or operating condition changes. Recent research emphasizes the importance of post-layout extraction and variability-aware analysis to obtain realistic performance estimates.As CMOS technology scales to deep submicron nodes such as 180 nm and 90 nm, process variations, voltage fluctuations, temperature changes, and device mismatches significantly affect circuit performance. These variations can alter delay, leakage power, switching characteristics, and functional reliability. Consequently, Process-Voltage-Temperature (PVT) corner analysis and Monte Carlo simulations are widely used to evaluate circuit robustness and yield. Such analyses are especially important for low-power multiplexer designs, where reduced voltage margins can increase sensitivity to manufacturing and environmental variations.

Although previous research has demonstrated the advantages of GDI and PTL-based multiplexer designs, comprehensive evaluations that include post-layout parasitics, PVT corner analysis, and statistical variability assessment remain limited. Many existing studies also do not fully address the practical implementation challenges of GDI logic in standard CMOS fabrication flows or quantify the impact of level-restoration circuitry. Therefore, the present work focuses on designing and comparing 2:1 and hierarchical 4:1 multiplexers using GDI, PTL, and TG logic styles at 180 nm and 90 nm technology nodes. The evaluation will include schematic-level and post-layout simulations, along with detailed PVT and Monte Carlo analysis, to compare power consumption, propagation delay, area, and overall design robustness for low-power VLSI applications.

III. PROPOSED SYSTEM

The proposed work presents a Hybrid Pass Transistor Logic–Transmission Gate Logic (PTL–TGL) based 4:1 multiplexer integrated with the Multi-Threshold CMOS (MTCMOS) power-gating technique to achieve low-power and high-speed performance for VLSI applications. The proposed architecture combines the advantages of PTL and TGL while minimizing their individual limitations. PTL is employed to reduce the transistor count and switching capacitance, whereas TGL is incorporated to provide full voltage swing and improve signal reliability. By integrating these two logic styles, the multiplexer achieves an efficient balance between power consumption, propagation delay, and circuit complexity.

The proposed 4:1 multiplexer consists of four input lines (D0, D1, D2, and D3), two select lines (S0 and S1), and a single output terminal. Depending on the combination of the select signals, one of the four input signals is transferred to the output. PTL is mainly used in the data selection path to reduce the number of switching transistors, while transmission gates are employed at critical stages to eliminate threshold voltage loss and ensure accurate logic-level transmission. This hybrid arrangement improves the overall switching performance and maintains stable output characteristics under different operating conditions.

To further improve power efficiency, the proposed design incorporates the MTCMOS power-gating technique. In this approach, a high-threshold voltage sleep transistor is inserted between the logic circuit and the power supply. During active operation, the sleep transistor remains ON, allowing the circuit to function normally with minimal performance degradation. During standby mode, the sleep transistor is turned OFF, disconnecting the logic block from the supply voltage and significantly reducing leakage current. This effectively minimizes static power dissipation without affecting the normal functionality of the circuit.

The proposed architecture is developed using 90 nm CMOS technology and implemented with Tanner EDA design tools. The circuit is designed in S-Edit, while functional verification and performance analysis are carried out using T-Spice simulations. The design is evaluated based on important performance parameters such as average power consumption, leakage power, propagation delay, and Power-Delay Product (PDP). The obtained results are compared with conventional CMOS, PTL, and Transmission Gate multiplexer implementations to demonstrate the effectiveness of the proposed hybrid approach.

The proposed system is designed to overcome the limitations of conventional multiplexer architectures by reducing transistor count, minimizing leakage current, and improving signal integrity. The combination of hybrid logic and MTCMOS power gating provides an efficient solution for designing energy-efficient digital circuits suitable for portable electronics, embedded systems, and other low-power VLSI applications.

IV. METHODOLOGY AND IMPLEMENTATION

The proposed Hybrid PTL–TGL 4:1 multiplexer with MTCMOS power gating is implemented using Tanner EDA in 90 nm CMOS technology to achieve low power consumption, reduced leakage current, and improved switching performance. The implementation process includes circuit design, schematic development, simulation, and performance evaluation. The proposed methodology focuses on reducing both dynamic and static power while maintaining reliable operation and high-speed performance.

Initially, the logic function of the 4:1 multiplexer is analyzed using its truth table and Boolean expressions. Based on the required functionality, a hybrid logic structure is developed by combining Pass Transistor Logic (PTL) and Transmission Gate Logic (TGL). PTL is employed in the data selection path to minimize transistor count and reduce switching capacitance, whereas TGL is incorporated at critical nodes to eliminate threshold voltage degradation and provide full voltage swing at the output. The combination of these logic styles results in an optimized circuit with improved speed and reduced hardware complexity.

To minimize standby leakage power, the MTCMOS power-gating technique is integrated into the proposed architecture. A high-threshold PMOS sleep transistor is inserted between the power supply and the logic circuit. During active operation, the sleep transistor remains ON, allowing the multiplexer to operate normally. During standby mode, the sleep transistor is turned OFF, isolating the logic block from the power supply and significantly reducing leakage current. This approach effectively lowers static power consumption without affecting the normal operation of the circuit.

The complete schematic of the proposed multiplexer is developed using the S-Edit environment of Tanner EDA. Standard 90 nm CMOS transistor models are used to implement the design. After completing the schematic, functional verification is performed using T-Spice simulations. Different combinations of input data and select signals are applied to verify the correct operation of the multiplexer. The simulated output waveforms confirm that the selected input is accurately transferred to the output for all possible input combinations.

The performance of the proposed design is evaluated using parameters such as average power consumption, leakage power, propagation delay, and Power-Delay Product (PDP). These performance metrics are compared with conventional CMOS, PTL, and Transmission Gate multiplexer implementations under identical simulation conditions. The comparison demonstrates the effectiveness of the proposed hybrid architecture in reducing power consumption while maintaining high-speed operation and reliable performance.

The implementation procedure consists of the following steps:

1) Design the logic of the 4:1 multiplexer.
2) Develop the hybrid PTL–TGL circuit architecture.
3) Integrate the MTCMOS power-gating technique.
4) Implement the schematic using Tanner S-Edit.

5) Perform functional verification using T-Spice simulation.
6) Measure power consumption, leakage power, propagation delay, and Power-Delay Product.
7) Compare the obtained results with existing multiplexer designs.

The adopted methodology provides an efficient approach for designing low-power multiplexers suitable for modern VLSI systems. The integration of hybrid logic and MTCMOS power gating improves energy efficiency, reduces leakage current, and enhances the overall performance of the multiplexer

V. CIRCUIT DESIGN

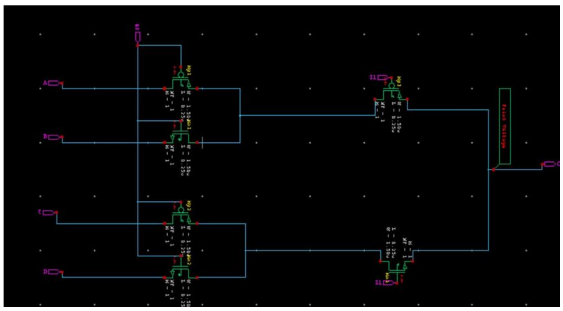

Figure 1. Hybrid 4X1 Mux

VI. RESULTS AND DISCUSSION

The proposed Hybrid PTL–TGL 4:1 multiplexer with MTCMOS power gating was designed and simulated using Tanner EDA in 90 nm CMOS technology. Functional verification was performed by applying different combinations of input signals and select lines to ensure correct multiplexer operation. The simulated output waveforms confirmed that the selected input was accurately transferred to the output for all possible input combinations, demonstrating the correctness of the proposed design.

The performance of the proposed multiplexer was evaluated using key design parameters such as average power consumption, leakage power, propagation delay, and Power-Delay Product (PDP). These parameters were measured under identical operating conditions and compared with conventional CMOS, Pass Transistor Logic (PTL), and Transmission Gate Logic (TGL) multiplexer implementations. The comparison indicates that the proposed hybrid architecture achieves improved energy efficiency while maintaining reliable circuit performance. The integration of PTL significantly reduces the transistor count and switching capacitance, resulting in lower dynamic power consumption. The incorporation of Transmission Gate Logic eliminates threshold voltage degradation and provides full output voltage swing, thereby improving signal integrity and reducing propagation delay. Furthermore, the MTCMOS power-gating technique effectively suppresses standby leakage current by disconnecting the logic circuit from the power supply during idle conditions. As a result, the proposed architecture demonstrates lower static power dissipation compared to conventional multiplexer designs. The simulation results also indicate that the proposed hybrid design provides an improved balance between power consumption, speed, and circuit complexity. Although the inclusion of a sleep transistor introduces a negligible delay overhead, the significant reduction in leakage power makes the proposed architecture highly suitable for low-power VLSI applications. The overall improvement in Power-Delay Product (PDP) confirms that the proposed design offers better energy efficiency than the existing multiplexer implementations.

The performance comparison between the proposed design and existing multiplexer architectures is summarized in the following tables and figure

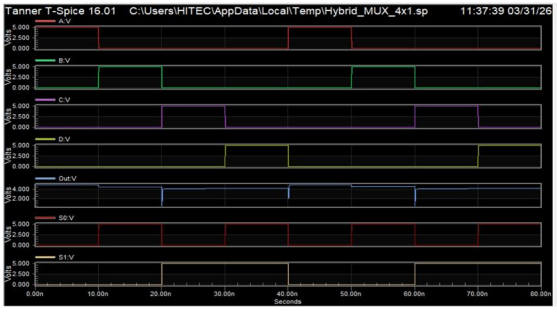

Figure 2. 4X1 Mux Output Waveform

The obtained simulation results demonstrate that the proposed Hybrid PTL–TGL multiplexer integrated with MTCMOS power gating successfully achieves the primary objectives of reducing leakage power, minimizing power consumption, and improving switching performance. The combination of hybrid logic techniques and power-gating methodology provides an efficient solution for designing energy-efficient multiplexers suitable for high-speed and portable VLSI applications.

VII. CONCLUSION

The proposed Hybrid 4:1 multiplexer provides a balanced improvement in power, delay, and area compared to Conventional CMOS and GDI designs. While CMOS ensures reliable operation, it has higher power consumption, and GDI may experience signal degradation. Although hybrid logic can introduce voltage loss and reduced noise margins, careful design minimizes these effects, making it an efficient solution for low-power VLSI applications.

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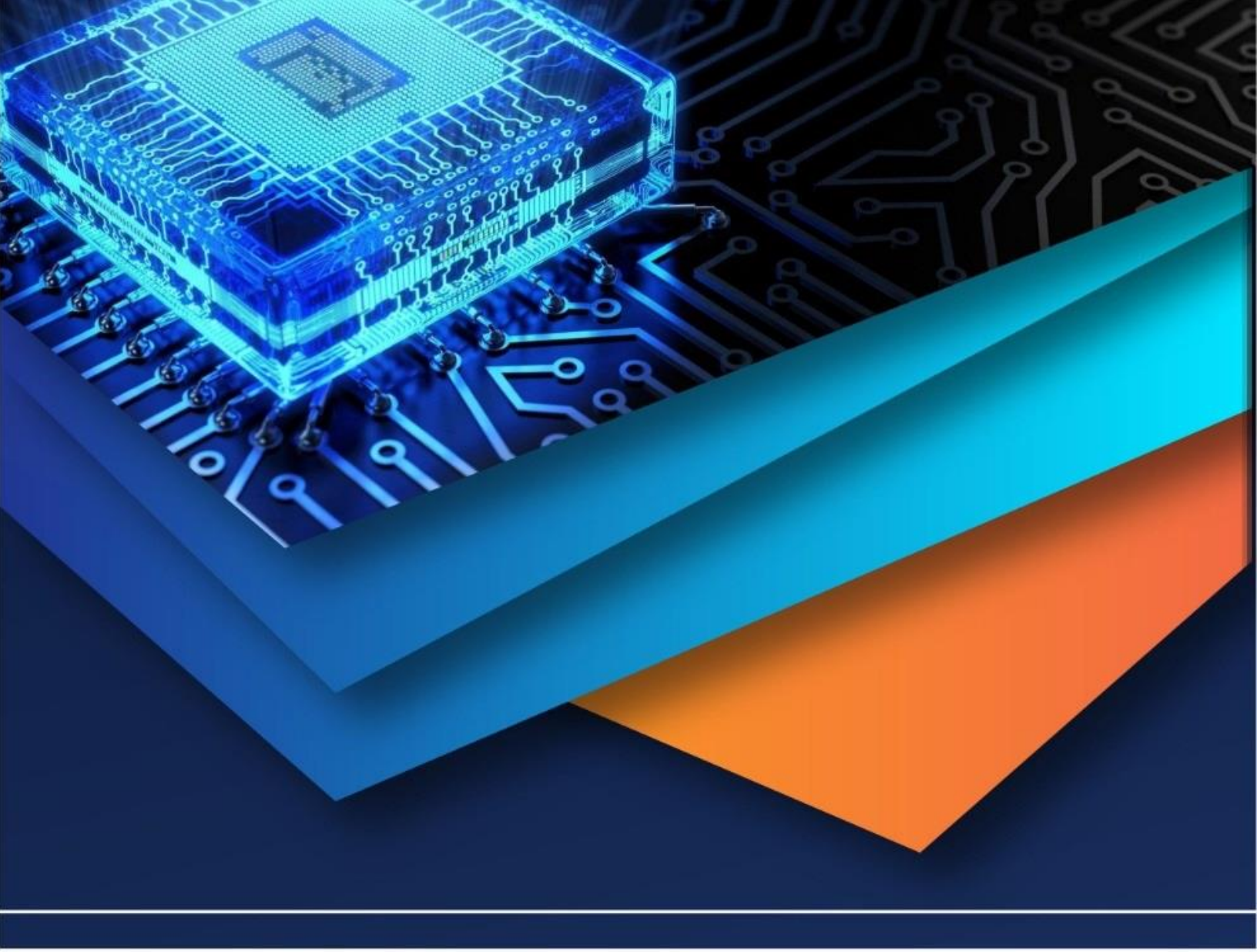

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