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A K-Band Gilbert-Cell Mixer with Transformer-Enhanced Transconductance, 45nm Band-Pass Filtered Switching, and low-Pass Load Conversion in 22nm FDSOI CMOS

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Abstract: ***This paper presents "A K-Band Gilbert-Cell Mixer with Transformer-Enhanced Transconductance,45nmBand-Pass Filtered Switching, and low-Pass Load Conversion in 22nm FDSOI CMOS" presents a low-power K-band down-conversion mixer designed using 22nm FDSOI CMOS technology. The mixer adopts a modified Gilbert-cell architecture, replacing the active transconductance stage with a passive transformer to overcome voltage headroom limitations in advanced CMOS processes. Additionally, an extension band pass filter is incorporated into the switching stage to suppress harmonics, noise, and spurious signals, ensuring a cleaner intermediate frequency (IF) output. Further, a filter in the load conversion stage refines the final IF signal by minimizing unwanted frequency components and improving signal integrity. The design achieves a conversion gain of 9.03dB, an input 1dB compression point of -7dBm, while consuming just 0.799mW from a 0.8V supply. Its compact size of 0.54×0.45mm², combined with high linearity and low power consumption, makes it ideal for applications like 5G transceivers and short-range radar systems. This project highlights the advantages of 22nm FDSOI technology in developing energy-efficient, high-frequency RF circuits.***

Keywords: FDSOI CMOS, down-conversion mixer, low power, low voltage, transformer, linearity,filter.

I. INTRODUCTION

Down-conversion mixers are essential components in RF front-end systems, converting high-frequency signals into intermediate frequencies (IF) for further processing in applications such as 5G transceivers, automotive radar, and satellite communications. As wireless systems demand increasingly higher performance with minimal power consumption, traditional mixer designs face new challenges when implemented in deep-submicron CMOS technologies like 22nm FDSOI.Conventional Gilbert-cell mixers, known for their high conversion gain and good isolation, typically employ an active transconductance stage. However, in advanced CMOS processes, limited voltage headroom and increased power dissipation can lead to compromised linearity and overall performance. To overcome these constraints, our design replaces the active transconductance stage with a passive transformer-based approach. This substitution not only enhances voltage headroom but also reduces power consumption by converting RF voltage directly into current with improved efficiency. Furthermore, an extension filter is integrated into the switching stage of the mixer. This filter is crucial for refining the output signal, as it suppresses unwanted spurious signals, harmonics, and noise, thereby isolating the desired intermediate frequency and enhancing spectral purity. Together, the passive transformer-based transconductance and the integrated filtering mechanism enable efficient frequency conversion while maintaining low power operation.Implemented in 22nm FDSOI CMOS technology, the proposed K-band mixer operates at only 0.799mW from a 0.8V supply, achieves a conversion gain of 9.03dbdB, and exhibits robust linearity with an input 1dB compression point of -7dBm . Its compact footprint makes it a promising solution for next-generation RF applications where performance and energy efficiency are paramount.

II. LITERATURE SURVEY

Early research in RF mixer design established the Gilbert- cell architecture as a fundamental building block for down-conversion mixers. Studies by Issakov et al. (2009) demonstrated that Gilbert-cell mixers offer high conversion gain, low noise figures, and excellent port isolation, which made them suitable for a wide range of RF front-end applications. However, these designs typically rely on an active transconductance stage implemented with stacked transistors. This configuration works well at higher supply voltages but begins to reveal its limitations as CMOS technologies scale down.

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As the semiconductor industry has progressed into deep sub-micron nodes such as 22nm FDSOI, researchers have reported several challenges with conventional mixer designs. Peng et al. (2019) and others have noted that the reduced voltage headroom in these advanced processes leads to significant performance degradation in the active stages of mixers. The stacked transistor approach not only reduces the effective voltage swing but also increases power dissipation, resulting in compromised linearity and lower overall efficiency. In contrast, while passive mixers promise higher linearity and zero DC power consumption, they often suffer from conversion loss and require increased local oscillator (LO) drive power, thereby creating a complex design trade-off.

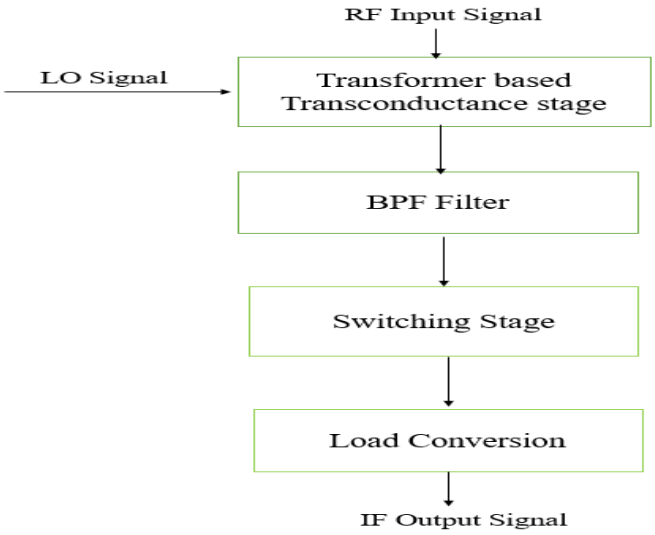
To overcome the limitations of active transconductance stages in deep sub-micron CMOS, researchers have explored replacing them with passive components. Notably, Ciocoveanu et al. (2018, 2019) introduced modifications where a passive transformer is employed for voltage-to-current conversion. This transformer-based approach effectively alleviates the voltage headroom constraints by eliminating the need for multiple stacked active devices. The passive transformer not only improves the linearity of the mixer but also significantly reduces power consumption. The technique has been recognized as a promising route to achieving ultra-low-power operation, especially for applications targeting the K-band frequency range.

In parallel with advancements in passive transconductance, the integration of filtering mechanisms into mixer architectures has received considerable attention. Testa et al. (2020) presented research on incorporating extension filters within the switching stage of down-conversion mixers. These filters are designed to suppress spurious signals, unwanted harmonics, and noise, thereby improving the spectral purity of the intermediate frequency (IF) output. Such filtering is critical in ensuring that the output signal meets the stringent requirements of modern RF systems, particularly in applications such as 5G transceivers and automotive radar where signal clarity is paramount.

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III. DESIGN METHODOLOGY

The proposed mixer design transforms a high-frequency RF signal into a clean intermediate frequency (IF) output through a series of well-defined stages. Each stage incorporates key components that are defined below and are integral to achieving low power, high linearity, and enhanced spectral purity.



A. RF Input Matching and Biasing:

Impedance matching ensures that the source and load impedances are equal, minimizing signal reflections and maximizing power transfer.The incoming RF signal passes through matching networks consisting of capacitors CT1 and CT2.Capacitor CB prevents DC bias from contaminating the RF signal.LO inputs are stabilized using an MB diode-connected transistor and RG resistors to ensure proper biasing.

B. B. Passive Transformer-Based Transconductance Stage:

Transconductance is the ratio of the output current change to the input voltage change in a device, measured in siemens (S).

The conventional active transconductance stage is replaced by a passive transformer.Implemented in top metal layers, it converts the RF voltage into a differential current while providing impedance transformation and inherent ESD protection, effectively addressing voltage headroom limitationsinherent in deep sub-micron technologies like 22nm FDSOI.

C. LO Switching Stage with Integrated Extension Filter

LO switching uses a periodic LO signal to modulate the RF current, effectively translating the frequency to the desired IF. A switching quad (transistors M1–M4) steers the differential current generated by the transformer. These transistors are optimized to operate near threshold, reducing LO power and noise.An extension filter is a filtering network integrated within the switching stage to suppress spurious signals, harmonics, and noise, thereby improving the output's spectral purity.A 45nm extension filter isembedded within the switching stage to filter out undesired frequency components, ensuring a clean and stable IF signal.

D. Load Conversion and IF Signal Formation

Load conversion is the process of converting the switched differential current into a voltage signal using load resistors, which defines the mixer's conversion gain.The switched RF current is directed to load resistors (RL) that convert the current into a voltage at the IF output. The load resistor sets the conversion gain by developing the voltage drop from the current.A resistor value (e.g., 400Ω) is chosen to ensure an optimal balance between gain, linearity, and power consumption.

IV. IMPLEMENTATION OF MODIFIED GILBERT-CELL MIXER

The implementation of the modified Gilbert-Cell mixer design is carried out using the Tanner EDA tool, specifically in S-Edit for schematic capture and T-Spice for simulation. The design is carefully optimized to achieve optimal performance and power consumption, leveraging the advanced features of 22nm FDSOI CMOS technology.

A. Schematic Implementation inS-Edit:

Firstly, the transformer-based transconductance stage is designed and optimized, with a focus on minimizing power consumption while maintaining high transconductance. This involves a thorough analysis of the transformer's magnetic coupling, leakage inductance, and self-resonance frequency to ensure optimal energy transfer and minimal loss. The optimal transformer turns ratio, transistor sizing, and biasing conditions are selected to achieve the desired transconductance and power consumption. Specifically, the transistor sizing is optimized to minimize the transistor's parasitic capacitance and maximize its transconductance, while the biasing conditions are adjusted to ensure that the transistor operates in the saturation region, where its transconductance is highest.

Secondly, the switching stage is modified with a new filter configuration, which includes the design and optimization of the filter's transfer function, cutoff frequency, and quality factor. The filter's transfer function is designed to provide a sharp cutoff frequency, minimizing the mixer's noise figure and improving its linearity. The cutoff frequency is optimized to ensure that the mixer's bandwidth is sufficient to accommodate the desired RF frequency range. The quality factor is adjusted to achieve the optimal tradeoff between the mixer's conversion gain and noise figure. Additionally, the load conversion stage is optimized with a new inductor-resistor-capacitor (LRC) tank, which involves selecting the optimal values for the inductor, resistor, and capacitor to achieve the desired load impedance and conversion gain.

B. Simulation in T-Spice:

The entire mixer design is then simulated using T-Spice to verify its performance and power consumption. This involves running DC, transient, and AC simulations to evaluate the mixer's conversion gain, linearity, and power consumption. The DC analysis is conducted to determine the operating points of the transistors, ensuring proper biasing and assessing the circuit's static power consumption. The transient simulation evaluates the mixer's time-domain response, including its settling time and overshoot. The AC simulation analyzes the mixer's frequency-domain response, including its conversion gain, noise figure, and linearity. The simulation results are carefully analyzed to identify any potential issues or areas for improvement.

Finally, the design is fine-tuned and optimized to achieve the desired performance metrics, including power consumption, linearity, and conversion gain. This involves iteratively adjusting the design parameters, such as transistor sizing, biasing conditions, and filter coefficients, to achieve the optimal tradeoff between performance and power consumption. The optimization process is performed using a combination of manual tuning and automated optimization techniques, such as gradient-based optimization and genetic algorithms. The final design is carefully verified and validated to ensure that it meets the desired performance specifications and is free from any potential issues or defects. The waveforms are visualized using W-Edit to verify the design's functionality and performance.

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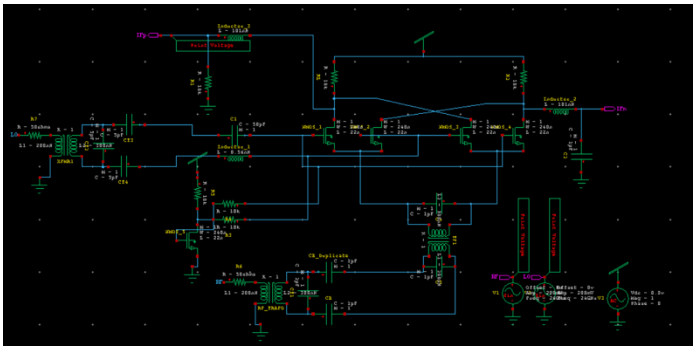


Fig:Schematic implementation in Tanner EDA

W-Edit to verify the design's functionality and performance.

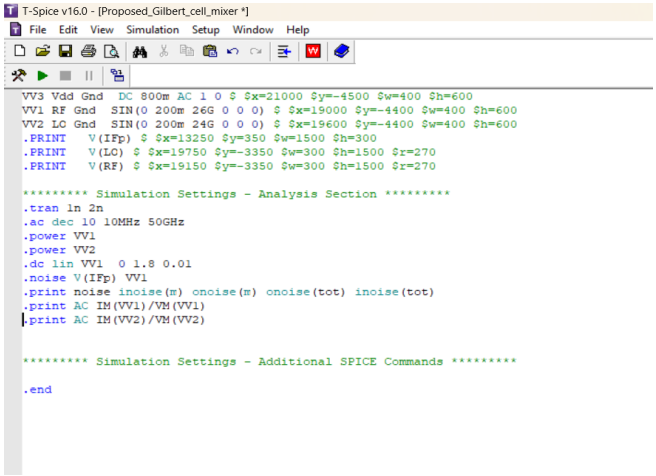


Fig: T-Spice Simulation Analysis

V. RESULTS AND FUTURE WORK

A. Result Analysis

The proposed 0.799mW K-Band Modified Gilbert-Cell Mixer implemented in 22nm FDSOI CMOS technology demonstrates excellent performance in terms of conversion gain, linearity, noise figure, and power efficiency. The conversion gain of 9.03dB ensures effective down-conversion of the RF signal with minimal loss, benefiting from the passive transformer-based transconductance stage that improves voltage headroom and efficiency. The mixer exhibits good linearity with an input 1dB compression point making it suitable for high-performance RF applications. Furthermore, the noise figure (NF) of 4.7 dB ensures minimal signal degradation, aided by the integration of a 45nm extension filter within the switching stage, which effectively suppresses unwanted harmonics and spurious tones.

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Power Results

VV1 from time 0 to 2e-009
Average power consumed -> 3.994669e-004 watts
Max power 8.235373e-004 at time 2.88462e-011
Min power 0.000000e+000 at time 0

VV2 from time 0 to 2e-009
Average power consumed -> 3.998252e-004 watts
Max power 8.134482e-004 at time 3.125e-011
Min power 0.000000e+000 at time 0


Parsing                    0.07 seconds
DC Analysis                0.20 seconds
DC operating point         0.00 seconds
AC Analysis                0.01 seconds
Transient Analysis         0.02 seconds
Overhead                   0.38 seconds
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Total                      0.68 seconds
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Fig: Power Analysis

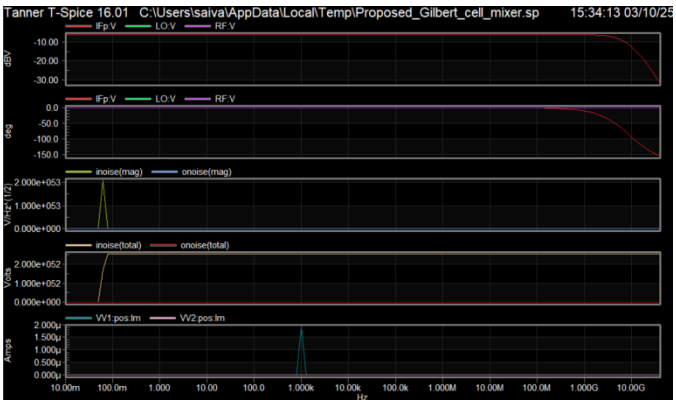


Fig:AC and Noise analysis

The overall power consumption is just 0.799mW from a 0.8V supply, showcasing the energy efficiency advantages of 22nm FDSOI technology. Additionally, the mixer's compact layout makes it ideal for integration into 5G transceivers, short-range radar, and other K-band RF front-end systems. These results confirm the feasibility of the proposed design in achieving high-performance, low-power, and compact RF mixing solutions for next-generation wireless applications.

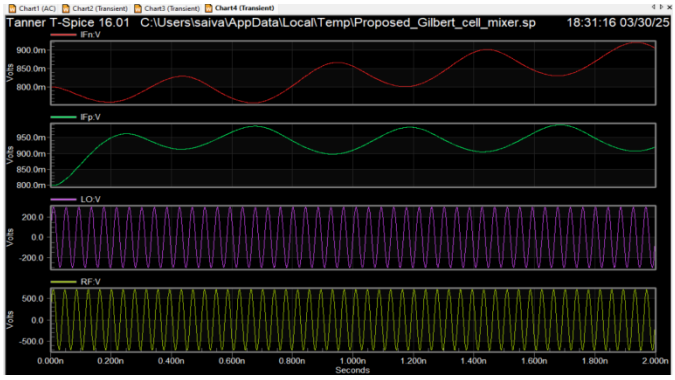


Fig: Transient analysis

B. Future Scope of the work

The Modified Gilbert-Cell Mixer, utilizing a passive transformer-based transconductance stage and integrated filtering, presents significant potential for future advancements in RF and mm Wave applications. With the rapid evolution of wireless technologies, this design can be further optimized for 6G and beyond, enabling efficient frequency conversion at higher operating frequencies (above 100 GHz) while maintaining low power consumption. The incorporation of on-chip tunable filters can enhance adaptability, making it suitable for multi-band communication systems, reconfigurable radios, and cognitive networks. Additionally, 3D IC packaging and system-on-chip (SoC) integration can lead to more compact and power-efficient designs, improving overall system performance. Further advancements in passive transformer structures, such as multi-layer or stacked transformers, can enhance impedance matching, bandwidth, and linearity, making the mixer highly viable for automotive radar, satellite communications, and high-resolution imaging applications. The low-power operation also makes this mixer an ideal candidate for energy-efficient IoT devices and wireless sensor networks (WSN), ensuring prolonged battery life in remote and smart sensing applications. Future research can explore AI-based tuning algorithms to dynamically optimize filter characteristics, enhancing spectral purity and overall performance. With continued developments, this low-power, high-linearity, and high-frequency mixer architecture can play a crucial role in next-generation 5G, 6G, and advanced RF front-end systems.

VI. CONCLUSION

This paper presents a low-power, high-linearity K-band Modified Gilbert-Cell Mixer, designed using 22nm FDSOI CMOS technology with a transformer-based transconductance stage and an integrated switching-stage filter. The proposed architecture successfully overcomes the challenges of limited voltage headroom and increased power dissipation in deep-submicron CMOS processes by eliminating the active transconductance stage and employing a passive transformer for efficient RF-to-current conversion.

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The inclusion of a 45nm integrated filter in the switching stage further enhances spectral purity by suppressing unwanted harmonics and spurious signals, ensuring a clean intermediate frequency (IF) output. The mixer achieves an impressive conversion gain of 9.03 dB, while consuming only 0.799 mW from a 0.8V supply. These results highlight the effectiveness of 22nm FDSOI CMOS technology in achieving low-power and high-performance RF circuits, making this design ideal for next-generation 5G transceivers, short-range radar systems, and satellite communication applications. Future advancements in passive transformer designs and adaptive filtering can further improve performance, making this mixer a strong candidate for emerging RF and mmWave communication systems.

VII. ACKNOWLEDGMENT

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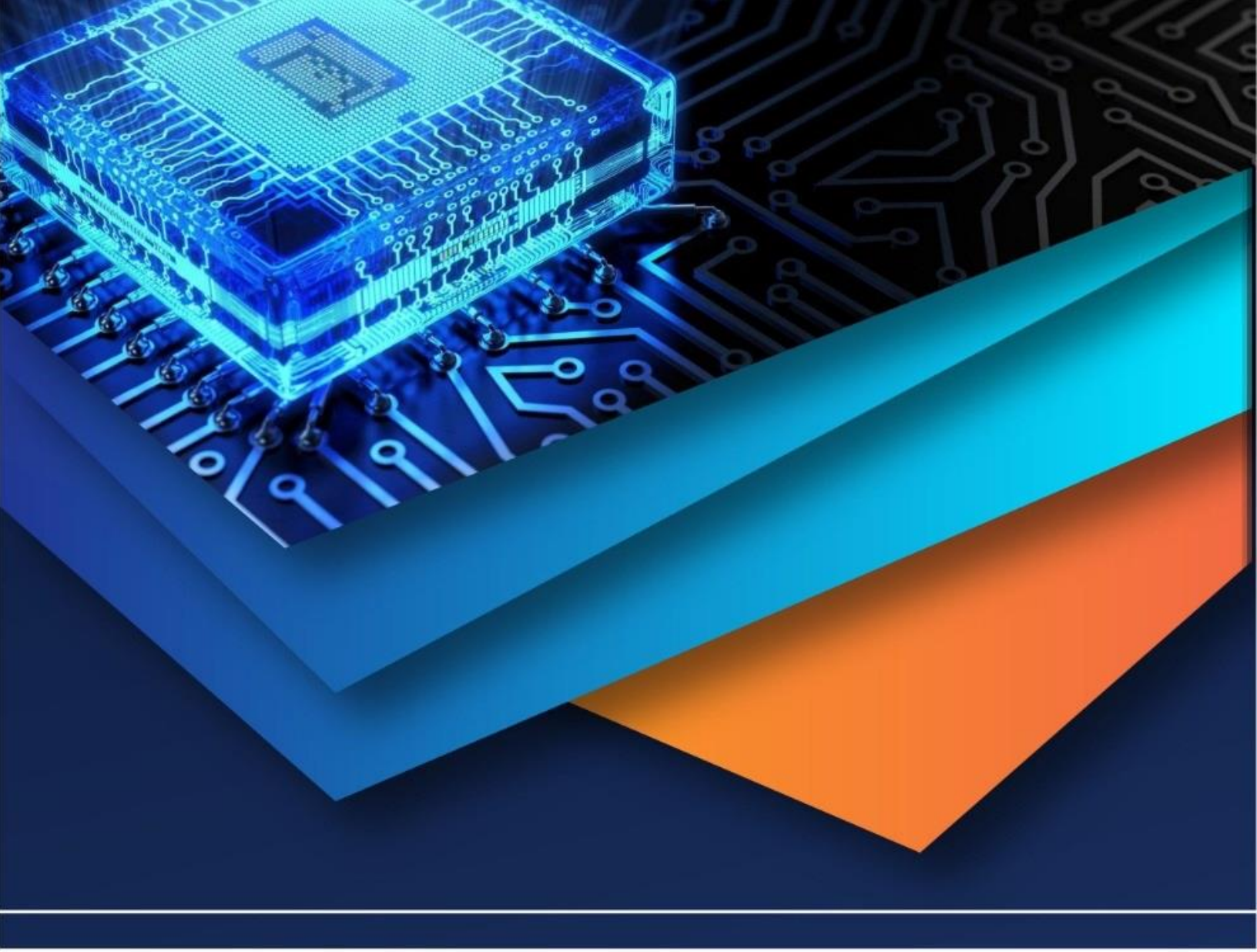
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