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A Review: O-ALU An Optimization-Enhanced Low Power ALU Design using Clock Gating and Power Gating

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Abstract: ***The rapid growth of portable, embedded, and IoT systems has made power efficiency a primary design constraint for Arithmetic Logic Units (ALUs), FPGA platforms, and RISC-V based processors. This review critically examines recent low-power design techniques reported between 2020 and 2025, covering clock gating, data gating, power gating, architectural optimization, and emerging device-level solutions. The surveyed literature shows that clock- and activity-aware gating methods, such as hybrid clock gating and signal-based gating, can achieve dynamic power reductions in the range of 45–66% while maintaining acceptable performance. FPGA-based implementations further demonstrate that clock gating, pipelining, and bio-inspired transition suppression can lower power consumption by up to 40%, though often at the cost of increased area and timing overhead. Technology-level innovations, including GDI logic, reversible logic, ternary logic, and sub-threshold operation, provide additional improvements in power-delay and energy-delay products, but their practical adoption is limited by design and verification complexity. At the system level, power-gated SRAM-FPGAs, FSM partitioning, and RISC-V based power management units enable substantial leakage and runtime power reduction, particularly for battery-constrained applications. Overall, the review indicates that hybrid strategies combining ALU-level gating, architectural power management, and system-level control offer the most balanced trade-off between power efficiency, performance, and scalability in modern digital systems.***
Keyword: Low-power ALU, Clock gating, Power gating, FPGA-based design, RISC-V processors, Energy-efficient architectures, Dynamic power reduction.

I. INTRODUCTION

Energy efficiency has emerged as a fundamental design objective in modern digital systems, particularly in embedded platforms, Internet of Things (IoT) devices, and high-performance computing environments. Core computational components such as Arithmetic Logic Units (ALUs), Field Programmable Gate Arrays (FPGAs), and processor architectures including RISC-V significantly contribute to overall power consumption. As technology scaling continues, controlling both dynamic and leakage power has become increasingly challenging.

A variety of low-power design techniques have been proposed at the architectural and circuit levels, including clock gating, power gating, Dynamic Voltage Threshold (DVT), and data gating. These approaches reduce unnecessary switching activity and minimize leakage during idle operation. Prior research has reported considerable power savings by employing hybrid clock gating, operand-aware clock control, distributed clock gating, and multi-Vdd techniques in ALU- and processor-based systems [1].

FPGAs offer a flexible platform for implementing low-power designs, enabling optimizations such as pipelining, logic restructuring, and parallel execution. Furthermore, advances in device-level technologies, such as Gate Diffusion Input (GDI), FinFET-based designs, and reversible logic using Quantum Dot Cellular Automata (QCA), have shown promising results in reducing energy consumption in nanoscale circuits [2].

However, these power-efficient techniques are often accompanied by increased design complexity, control overhead, and verification challenges. To evaluate their effectiveness, researchers have relied on industry-standard electronic design automation tools, including Xilinx Vivado, Cadence Virtuoso, and ModelSim, across various technology nodes. These evaluations confirm improvements in power-delay product and area efficiency for embedded and large-scale computing systems [3].

In parallel, RISC-V- and FPGA-based architectures have increasingly incorporated reliability and scalability considerations. Techniques such as Power Management Units (PMUs), Triple Modular Redundancy (TMR), hybrid encryption accelerators, and bio-inspired algorithms have been integrated to enable dynamic power management while enhancing fault tolerance and security [4]. Low-power ALU designs supporting 8-bit, 16-bit, and 32-bit operations have further facilitated scalable and real-time edge computing applications.

This review systematically analyzes low-power design strategies for ALUs, FPGAs, and RISC-V architectures, with particular emphasis on clock gating, power gating, DVT, and data gating techniques. By synthesizing existing research and identifying key trade-offs among power, performance, and area, the review highlights effective approaches for designing energy-efficient and reliable digital systems [1], [5].

II. LITERATURE REVIEW

A. *Clock Gating Power Gating DVT Low Power Design and Adder Techniques*

TABLE 1 Review of Clock Gating, Power Gating, and Low-Power ALU / DVT-Based Design Techniques

Ref.	Year	Authors	Target Architecture / Module	Key Technique(s)	Tools / Technology	Major Results	Limitations / Gaps
[6]	2025	Priyadarshini *et al.*	Arithmetic Logic Unit (ALU)	Hybrid Clock Gating (Instruction-aware + Operand-aware gating)	Xilinx Vivado 2022	• 52.22% reduction in dynamic power • Max delay: 6.8 ns • Area: 3687 µm²	• Increased control logic complexity • Limited focus on static power reduction • No adaptive or optimization-based gating
[7]	2021	Ghamkhari & Ghaznavi-Ghoushchi	Shift Register (DA-based FIR filter)	Gated Flip-Flop + Implicit Clock Gating + multi-Vdd	180 nm CMOS	• 62.2% dynamic power reduction • Additional 29–21% via Multi-Vdd • 15–40% power savings in shift registers	• Data-pattern dependent efficiency • Increased design overhead • Limited applicability beyond DA architectures

B. *FPGA, ALU, Low power design, Clock gating techniques*

Review of FPGA-Based ALU Low-Power Design and Clock Gating Techniques

Ref.	Year	Authors	Target System	Key Technique(s)	Platform / Tool	Power & Performance Gains	Limitations
[8]	2020	Kulkarni & Kulkarni	32-bit ALU	Distributed Clock Gating	45 nm CMOS, Cadence	• 45–50% power reduction • 250 MHz operation • Area ↑ 2–3%	Added control logic complexity
[9]	2022	Verma et al.	FPGA-based IoT ALU	Clock Gating, Operand Gating, Parallelism, Pipelining	Xilinx Vivado, XPower	• CGOH: 35.68% power ↓ • Pipeline: 31.92% power ↓	Trade-off between delay, area, and power

[10]	2022	Hameed et al.	ALU	Signal-Based Clock Gating (Glitch-Resilient)	130 nm CMOS, ModelSim	• Up to 24.90% total power reduction	Increased circuit complexity
[11]	2021	Arulkumar & Chandrasekaran	EDCI Scheme ALU	Power Gating + Signal-Based Clock Gating	130 nm CMOS, ModelSim	• Power ↑ 66.67% efficient • Delay ↓ 71–78%	Complex gating logic
[12]	2024	Hussein et al.	8-bit ALU	GDI + FET Technology	20 nm, Cadence Virtuoso	• Improved PDP & EDP • High energy efficiency	Layout complexity
[13]	2022	Vijay et al.	Synchronous Counters	Clock Gating	Spartan-3 FPGA, ISE 14.2	• Area ↑ 24% • Fmax ↑ 31% • Latency ↓ 36%	Additional control circuitry
[14]	2020	Singh et al.	CMOS Digital Systems	Logic Restructuring, Clock Gating	Quartus Prime, ModelSim	• Clock gating saved ~3.5% thermal power	Careful design required
[15]	2024	Yeapa et al.	Floating-Point Unit (FPU)	Pipelining + Ternary Logic + CEDS	Zybo Z7-10 FPGA	• Power/Delay/Area ↓ 45%	High design complexity
[16]	2024	Nagarathna & Aswatha	FPU	Ternary Logic + Clock-Efficient Distribution	Zybo Z7-10 FPGA	• 45% power & delay reduction	Ternary logic handling difficulty
[17]	2025	Mohanapriya et al.	FPU	Pipelining + Ternary Logic	Zybo Z7-10 FPGA	• 45% reduction in power & area	Increased circuit complexity
[18]	2021	Rattan & Walia	FPGA SoC	BRAM Cascading + HLS Optimization	Xilinx Vivado	• Reduced FPGA power via BRAM control	Hard to meet strict constraints
[19]	2025	Pasaya et al.	8-bit ALU	SSA & Swarm Intelligence Algorithms	Spartan-7 FPGA	• Power ↓ to 6 mW (SSA), 4 mW (SIA)	Resource–power trade-off
[20]	2023	Jahanirad	SRAM-based FPGA	Power Gating + Sleep Mode	FPGA-SPICE	• 95% leakage ↓ in sleep mode	Dynamic control complexity
[21]	2025	Sharma et al.	FSM-based Systems	FSM Partitioning + Clock Gating	Xilinx ISE 14.7	• Power ↓ up to 87.5%	Partitioning overhead
[22]	2024	Agarwal et al.	FPGA Systems	FPGA Design Optimization Survey	Xilinx & Others	• Highlights FPGA flexibility & power	Requires careful power management

C. 8-bit, 16-bit, 32-bit ALU, Clock gating, Low power techniques

Comparative Analysis of Low-Power ALU and Processor Design Approaches

Ref.	Year	Architecture / Bit-Width	Key Techniques Used	Design & Simulation Tools	Performance Metrics Evaluated	Major Advantages	Key Limitations
[23]	2024	32-bit ALU	Multiplexer-based	Cadence	Power	Reduced power	Increased design

			arithmetic unit (4×1, 2×1 MUX), logic unit with basic gates; low-power ALU architecture	Virtuoso, GPDK 180 nm	consumption, propagation delay	consumption; suitable for high-speed portable applications; integrated arithmetic and logic operations	complexity due to extensive MUX usage; scalability concerns for higher bit-width ALUs
[24]	2021	Processor ALU (8-bit/byte-oriented)	Modular VHDL/Verilog design; Harvard architecture; pipelining; top-down ALU integration	VHDL, Verilog HDL, simulation testbenches	Functional correctness, execution speed	Faster execution through pipelining; modular and reusable architecture; resource-aware optimization	High design and verification complexity; strong inter-module dependency increases validation effort
[25]	2021	N-bit ALU (Reconfigurable)	Reversible logic gates; Quantum Dot Cellular Automata (QCA); low quantum cost adders and multipliers	Xilinx ISE, QCA simulation	Area, power dissipation, delay	Significant reduction in power, area, and delay; high flexibility due to reconfigurability	

D. RISC-V, ALU, Data gating, Clock gating, Power saving techniques

Review of Power-Efficient RISC-V Architectures and ALU-Level Power Optimization Techniques

Ref.	Year	Target Architecture	Key Techniques	Platform / Tools	Power & Performance Outcomes	Major Strengths	Limitations
[26]	2024	RISC-V A-core	Power Management Unit (PMU), Clock & Voltage Scaling, Activity Monitoring	Simulation-based RISC-V core	Reduced runtime power consumption; improved performance efficiency	Dynamic power adaptation based on workload	High design complexity; scalability issues in multicore systems
[27]	2021	RISC-V Execution Unit (ALU & Multiplier)	TMR, Standby Sparing, Alpha Counting	RTL-based RISC-V core	Improved fault tolerance without performance loss	High reliability and resource reuse	Increased area and control overhead
[28]	2023	RISC-V IoT Processor	Hybrid Encryption Accelerator (SM3 + SM4), ALU coupling	FPGA & 90 nm CMOS	• FPGA resources ↓ 39.1–66.2% • Power efficiency ↑ 10–34.8%	Secure and power-efficient data processing	Increased design and integration complexity
[29]	2021	Edge / IoT Computing Systems	Sub-threshold Operation, Ultra-low Voltage Logic (DDSL)	CMOS-based circuits	Significant energy reduction at ultra-low voltages	Excellent energy efficiency for battery devices	Noise sensitivity and timing instability
[30]	2023	RISC-V Soft Processors (Rocket, NOEL-V)	Fault Tolerance (TMR, Scrubbing, Refresh)	SRAM-based FPGA	Reliability improved up to 85×	Aerospace-grade reliability	Increased area and power overhead

III. COMPARATIVE ANALYSIS

The reviewed studies indicate that clock gating and activity-aware control are the most effective and widely adopted techniques for reducing power in ALU and processor designs. Priyadarshini *et al.* [6], Kulkarni and Kulkarni [8], and Arulkumar and Chandrasekaran [11] achieved 45–66% dynamic power reduction by selectively disabling the clock based on instruction or signal activity. These approaches preserve performance but introduce additional control logic, increasing design complexity.

FPGA-based ALU optimizations, such as those by Verma *et al.* [9], Vijay *et al.* [13], and Pasaya *et al.* [19], demonstrate that clock gating, pipelining, and intelligent transition suppression can significantly reduce power (up to 35–40%), though often at the cost of higher resource utilization and timing overhead. At the technology level, GDI logic, FET-based designs [12], reversible logic [25], and ternary logic CEDS architectures [15–17] provide further improvements in power-delay product and energy efficiency, typically achieving about 45% reduction, but they suffer from increased implementation and verification complexity. System-level solutions in FPGA and RISC-V platforms, including power gating, FSM partitioning, and PMU-based control [20, 21, 26], enable leakage reduction up to 95% in sleep modes and improve run-time energy efficiency, although they require sophisticated control and monitoring hardware. Overall, the literature suggests that hybrid approaches combining clock gating, power gating, and dynamic power management offer the best trade-off between power savings, performance, and scalability for modern low-power ALU and processor designs.

IV. RESEARCH GAPS

The review of studies published between 2020 and 2025 indicates substantial progress in low-power ALU and FPGA-based design techniques, including clock gating, power gating, multi-Vdd, Dynamic Voltage Threshold (DVT), and hybrid optimization approaches. Numerous researchers have focused on reducing dynamic and leakage power through fine-grained clock control, operand-aware mechanisms, and architectural modifications. In particular, hybrid clock gating (HCG), signal-based gating, and distributed clock gating techniques have demonstrated notable power savings—reaching up to 66% in certain designs—while maintaining acceptable trade-offs in delay and area. Similarly, FPGA-based implementations and RISC-V cores have adopted optimization strategies such as pipelining, bio-inspired algorithms, and multi-mode operation to enhance energy efficiency in Internet of Things (IoT) and high-performance computing applications. These approaches have proven effective in reducing power consumption under specific workloads and operating conditions. However, despite these advancements, several critical challenges remain unresolved. A recurring limitation across the reviewed literature is the increased design complexity introduced by aggressive low-power techniques. Fine-grained clock gating and hybrid control mechanisms often lead to higher control overhead, timing closure difficulties, and dependency on data activity patterns. Moreover, many existing solutions exhibit limited scalability and insufficient fault tolerance, which restrict their applicability in nanoscale technologies and safety-critical domains such as aerospace and mission-critical embedded systems.Another significant research gap lies in the fragmented nature of power optimization strategies. Most existing works focus on optimizing either dynamic power or leakage power in isolation, while very few studies integrate multiple power-saving techniques within a unified and flexible architectural framework. In addition, clock gating approaches frequently introduce synchronization and timing issues, and FPGA-based designs lack a systematic mechanism for adapting power consumption dynamically across varying workloads and operational modes. Consequently, there exists a clear need for a reconfigurable and scalable ALU architecture that can effectively balance low power consumption with manageable design complexity, high performance, and enhanced fault tolerance. Such an architecture should be capable of integrating multiple low-power strategies, supporting different data widths and workloads, and maintaining energy-efficient operation across modern embedded systems, IoT devices, and RISC-V processor environments. The identified research gaps and the motivation for the proposed work are illustrated in Fig.1

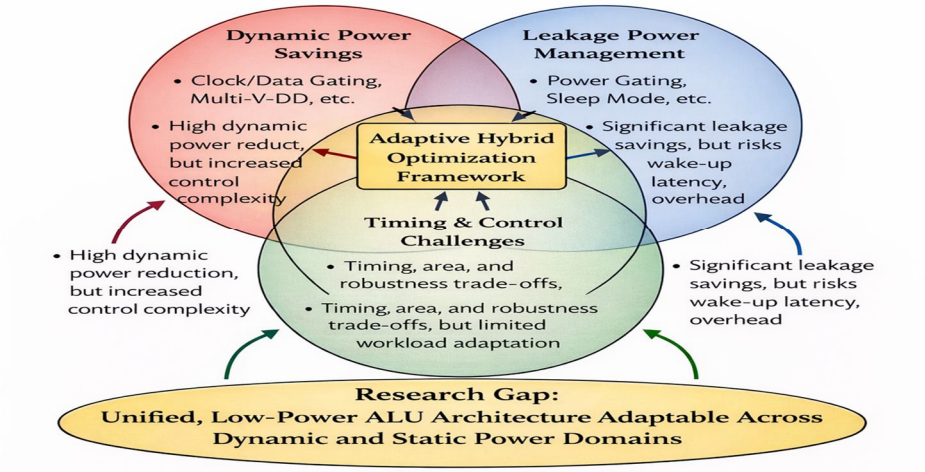

Fig. 1 an adaptive hybrid optimization framework in low-power ALU architecture

V. CONCLUSION

This review has presented a comprehensive analysis of low-power design methodologies applied to Arithmetic Logic Units (ALUs), FPGA-based systems, and RISC-V processor architectures. The surveyed research primarily focused on power-saving techniques such as data gating, clock gating, power gating, and Dynamic Threshold Voltage (DVT) scaling to reduce both dynamic and leakage power consumption. A wide range of strategies—including Hybrid Clock Gating (HCG), distributed and signal-based clock gating, and multi-Vdd schemes—have been explored to achieve energy-efficient operation while maintaining acceptable performance levels. These techniques have been validated across technology nodes ranging from 180 nm to 20 nm using industry-standard design tools such as Xilinx Vivado, Cadence Virtuoso, and ModelSim.

FPGA-based implementations have played a significant role in advancing low-power design through architectural optimizations such as parallelism, pipelining, and High-Level Synthesis (HLS). Experimental results reported in the literature demonstrate power reductions ranging from approximately 24% to more than 66%, confirming the effectiveness of gating and hybrid optimization methods. However, these benefits are often accompanied by increased design complexity, higher control overhead, synchronization challenges, and additional area requirements due to the inclusion of monitoring and control logic.

Despite these limitations, the reviewed architectures have proven highly suitable for embedded systems, Internet of Things (IoT) applications, and high-speed digital systems, where energy efficiency and performance are critical design requirements. In parallel, significant advancements have been achieved in low-power RISC-V processor designs, where energy optimization has been coupled with enhanced reliability and security. The integration of Power Management Units (PMUs), fault-tolerant techniques such as Triple Modular Redundancy (TMR), hybrid encryption accelerators, and intelligent data gating has enabled dynamic power control while maintaining robust system performance.

Furthermore, innovations at the device and logic levels—such as FinFET-based ALUs, reversible logic designs, Quantum Dot Cellular Automata (QCA), and ternary logic—have contributed to substantial improvements in power-delay product for nanoscale technologies. FPGA and CMOS implementations have also demonstrated notable gains in power efficiency, area utilization, and fault resilience, particularly in aerospace and IoT-oriented systems.

In summary, the reviewed studies clearly indicate that while existing low-power techniques are effective in significantly reducing energy consumption, achieving an optimal balance among power savings, scalability, performance, and design simplicity remains an open challenge. Future low-power computing architectures must therefore emphasize unified, reconfigurable, and fault-tolerant design approaches that can adapt to varying workloads and technology constraints while minimizing control complexity and verification overhead.

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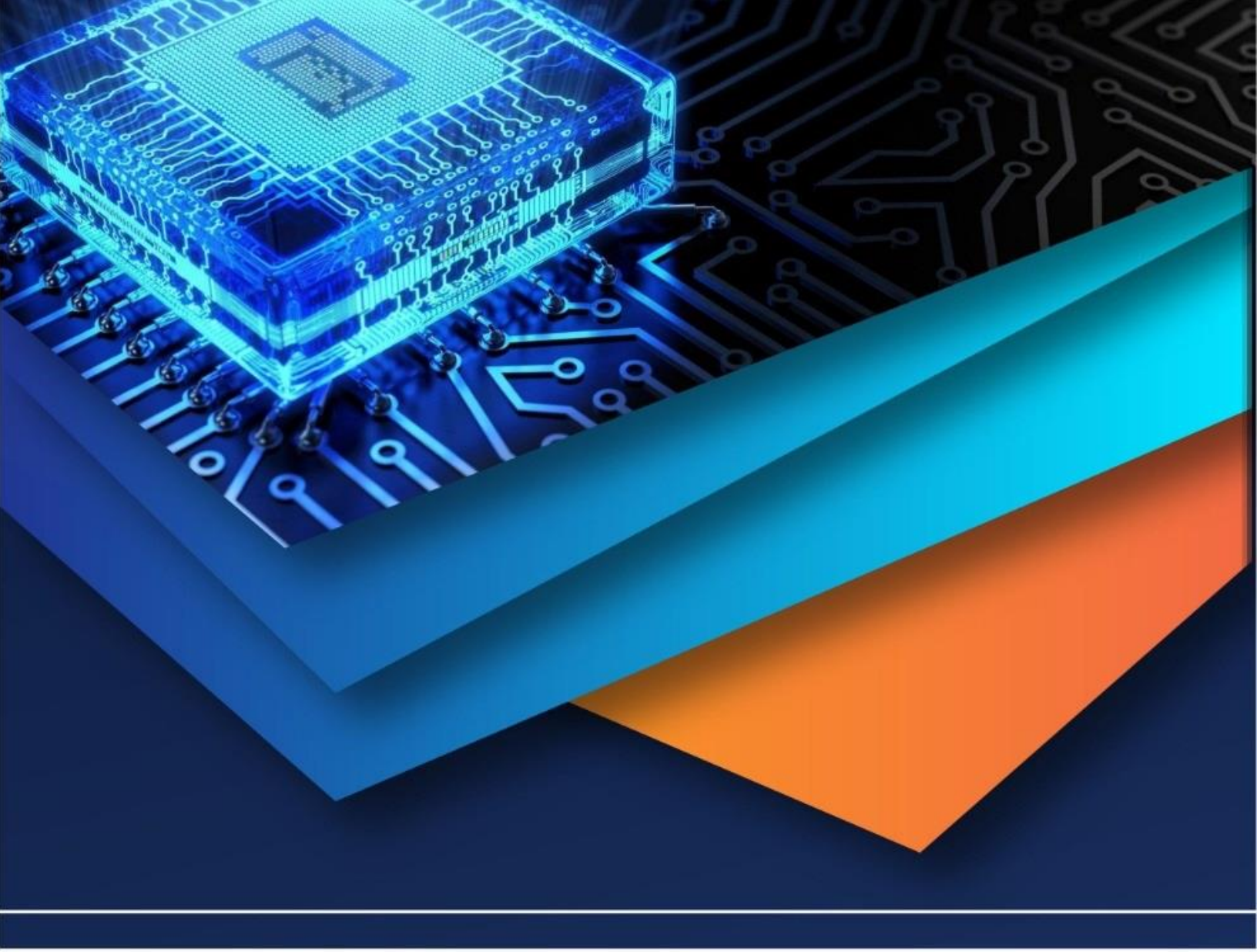

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