iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 13 **Issue:** VI **Month of publication:** June 2025

DOI: https://doi.org/10.22214/ijraset.2025.72860

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 13 Issue VI June 2025- Available at www.ijraset.com

A Second Order True VCO ADC Applying a Digital Pseudo DCO Apt for Sensor Arrays

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Abstract: ***This paper presents a power-efficient, second-order VCO-based analog-to-digital converter (ADC) implemented in 45 nm CMOS technology. The proposed architecture employs a power-gated, current-starved 7-stage ring VCO using MCML and a fully digital pseudo-DCO. By integrating sleep transistors and hardware-level gating, the design achieves a 66% reduction in total power consumption—from 1088.1 µW to 369.9 µW—while maintaining 4-bit resolution and a 1 MHz sampling rate. The scalable pseudo-DCO enables binary-weighted frequency generation, dynamic resolution control via Over-Running Ratio (ORR) tuning, and efficient multi-channel sharing. This digital-centric approach reduces reliance on complex analog blocks, enhances robustness in advanced nodes, and supports compact, low-power integration. This architecture is well-suited for battery-constrained applications such as wearable health monitors, implantable sensors and edge IoT devices.***

Keywords: True power gated current starved VCO-ADC, Digital pseudo-DCO, Frequency to digital converter, Sensor array application.

I. INTRODUCTION

The evolution of analog-to-digital converter (ADC) architectures has shifted decisively toward digitally dominated designs, driven by growing demands for low power, high integration, and robustness against process-voltage-temperature (PVT) variations. Applications such as implantable medical devices, wearable biosensors, and always-on IoT nodes require ADCs that are not only energy-efficient and compact but also capable of maintaining accuracy and resolution under constrained conditions. Voltage-Controlled Oscillator (VCO) based ADCs have emerged as promising alternatives to traditional analog-heavy designs, offering digital compatibility, reduced analog complexity, and technology scalability[1].

A second-order true VCO-based ADC,utilizing a digital pseudo-Digitally Controlled Oscillator (pseudo-DCO), presents a compelling solution for achieving precision with minimal power consumption[2]. The architecture leverages the inherent frequency modulation behaviour of VCOs and applies digital techniques such as pulse frequency modulation (PFM), noise shaping, and oversampling to enable high-resolution quantization without complex analog circuitry. This hybrid structure addresses common limitations in time-domain ADCs, including non-linearity, PVT sensitivity and limited dynamic range.

A key innovation is the use of a power-gated, current-starved ring VCO. Unlike conventional VCOs that consume static and dynamic power continuously, the proposed design employs sleep transistors, dual-threshold MOSFETs and gated-switch networks to selectively disable inactive circuit paths, significantly reducing leakage power during idle periods[3]. Additionally, the integration of MOS Current Mode Logic (MCML) enhances noise immunity and maintains signal integrity in mixed-signal environments[4]. Replacing traditional analog integrators and comparators, the design adopts a PFM-based second-order loop using the VCO and asynchronous digital accumulators[5].

This approach achieves infinite DC gain and effective noise shaping, while operating efficiently at low supply voltages and providing strong resilience against mismatch and variability across process corners. The fully digital pseudo-DCO further enhances the system's scalability and flexibility[6]. By generating orthogonal eigen rates through a sequence generator and combining them based on a digital input word, it outputs a binary-weighted frequency signal. With support for Over-Running Ratio (ORR) scaling, the pseudo-DCO enables dynamic adjustment of resolution and power, and supports multi-channel sharing, making it highly suitable for sensor arrays. In contrast to LC oscillators which offer precision but are area and cost intensive—the ring oscillator-based approach is inherently more compact, synthesizable, and suitable for dense CMOS integration.

The use of current-starved delay cells ensures fine-grained frequency control with minimal area and power overhead, ideal for high-channel-count systems.This work presents a digitally enhanced, power-optimized second-order VCO-based ADC that combines low-leakage circuit techniques with robust digital signal processing. The proposed architecture achieves high-resolution conversion, low power consumption and scalability, making it particularly well-suited for next-generation biomedical monitoring, wearable electronics, acoustic sensing and other ultra-low-power edge applications.

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ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 13 Issue VI June 2025- Available at www.ijraset.com

II. PROPOSED METHODOLOGY

A. Power Gated VCO

The Voltage-Controlled Oscillator (VCO) serves as the core of the ADC, converting the analog input voltage into a frequency-modulated signal. The given VCO design integrates multiple advanced techniques to optimize both power efficiency and performance, making it highly suitable for low-power applications such as biomedical signal processing and IoT systems. At its foundation, the VCO uses a 7-stage ring oscillator configuration composed of CMOS inverter-based delay cells. These stages generate a periodic output, and the oscillation frequency is directly modulated by the input voltage Vin, which controls the tail current through an NMOS transistor. This approach ensures a linear voltage-to-frequency conversion.

To achieve precise control over the oscillation frequency and reduce dynamic power consumption, the design adopts a current-starved architecture, which restricts current flow through each inverter stage, allowing finer tuning and lower energy dissipation. Additionally, power-gated MOSFETs are integrated between the delay stages and power rails, enabling the circuit to disconnect from the power supply during idle or sleep states Figure.1[4]. This significantly reduces leakage power, which is crucial for systems with long idle periods. Furthermore, the use of MOS Current Mode Logic (MCML) via a biasing transistor provides a stable reference current, helping to suppress switching noise and improve frequency stability.

The design also incorporates the Pull-Up Sleepy technique, using specially designed PMOS transistors that reduce leakage current when the circuit is inactive, without compromising performance during operation. Combined with power gating, this ensures both static and dynamic power reductions. Altogether, the VCO leverages current-starving, MCML biasing, pull-up sleepy logic, and power-gating to deliver a compact, low-power, and high-performance voltage-to-frequency conversion suitable for integration in hybrid VCO-based ADC architectures.

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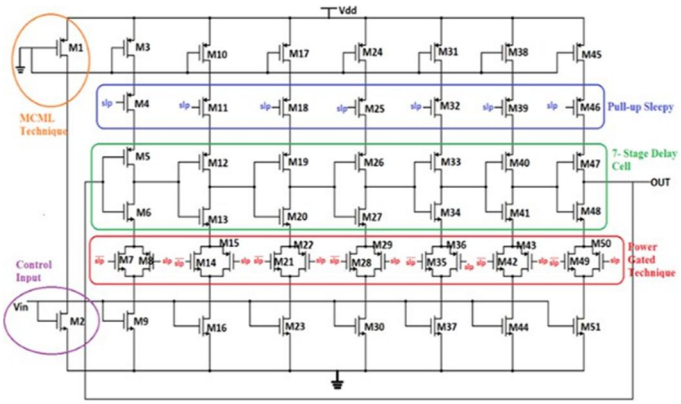


Fig.1 Power Gated VCO

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TABLE 1 Working Operation Of Power Gated VCO

Phase	Transistor State	Function
Initialization	M1, M2: ON; Others: OFF	Prepares circuit for oscillation
Sleep Mode	All OFF	Minimizes leakage in low-power sleep
Power Gating ON	M7–M50: ON; M1, M2, SLP: OFF	Restores power via gated paths
Charging Phase	PMOS: ON; NMOS: OFF	Charges delay-stage capacitors
Discharging Phase	NMOS: ON; PMOS: OFF	Discharges capacitors, enabling oscillation
Power-Off Mode	All OFF	Full shutdown to save energy

B. Frequency To Digital Converter (FDC)

The Frequency-to-Digital Converter (FDC) plays a crucial role in translating the frequency-modulated output of the Voltage-Controlled Oscillator (VCO) into a corresponding digital value that can be processed by digital systems[7-12]. This conversion is accomplished through a resettable counter mechanism. The FDC monitors the number of oscillation cycles produced by the VCO within a fixed and predefined time window, effectively quantifying the frequency in terms of digital code. The fundamental principle behind this operation is that the oscillation frequency of the VCO is directly proportional to the input control voltage. Hence, as the analog input voltage to the VCO varies, the frequency of its output signal changes accordingly, and the FDC captures this change by counting the pulses within the sampling interval.

The counter is reset at the beginning of each sampling period to ensure fresh accumulation of frequency data for every interval, enabling consistent and accurate digital representation. For instance, when the input voltage is at its minimum level, the VCO operates at its lowest frequency, generating fewer pulses. As shown in Figure 2, this results in the counter outputting a digital value of "0001" (binary), indicating that only one pulse was counted. Conversely, when the input voltage is at its maximum, the VCO oscillates at its highest frequency, producing 16 pulses within the same time interval. This leads the counter to register a digital value of "1111" (binary), reflecting the peak frequency.

The compact architecture of the FDC contributes to its suitability for integration in power-constrained systems. Its minimal logic depth and robust reset mechanism ensure low latency and reliable operation even at high speeds. Additionally, the monotonic nature of the conversion process where an increase in input voltage results in a proportional and predictable increase in digital output guarantees signal integrity and accuracy. Altogether, the FDC is a vital component in hybrid ADC systems, bridging the analog-to-digital gap with precision, speed, and energy efficiency.

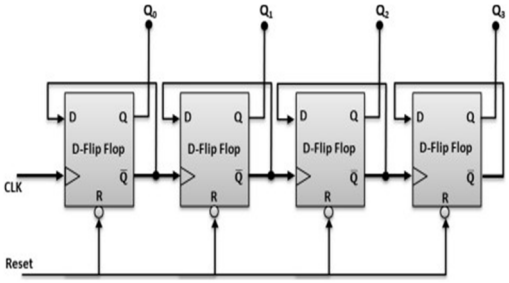


Fig.2 Frequency to Digital Converter

C. Sequence Generator

The sequence generator is a fundamental digital component in pseudo-DCO (Digitally Controlled Oscillator) architectures. It derives a set of orthogonal time-domain reference signals—called eigen rates—from a single master clock using a chain of D-type flip-flops. In a 4-bit implementation, it outputs four periodic signals (sb<0> to sb<3>) at fm/2, fm/4, fm/8, and fm/16, where *fm* is the master clock frequency. These signals have non-overlapping high periods, ensuring clean, conflict-free combination.

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The generator acts as a digital-to-frequency converter, where each bit of a 4-bit input control word (DIN) determines the inclusion of a corresponding eigen rate. AND gates are used to gate each eigen rate with its respective control bit, and the gated outputs are combined *via.*, a multi-input OR gate to form the final single-bit output sdco in Fig 3. The output frequency is the sum of the selected eigen rates, maintaining a linear relationship with the input word as shown in Fig 4.

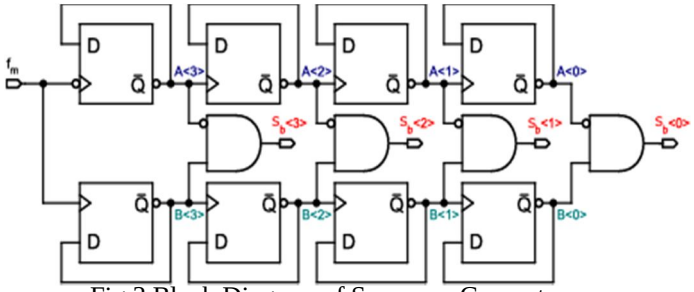


Fig.3 Block Diagram of Sequence Generator

To ensure deterministic and synchronized operation, particularly at startup, the flip-flops are equipped with an asynchronous reset. This initialization guarantees that all eigen rates start from a known logic state, maintaining phase alignment and preventing irregular output behaviour. Without proper reset, overlapping or unpredictable signal timing can degrade the accuracy of the synthesized frequency.

The design is scalable and resource-efficient, supporting shared use across multiple pseudo-DCOs in system-on-chip (SoC) architectures. In applications with parallel ADCs—such as sensor arrays—a single sequence generator can serve multiple channels, reducing area and power overhead. Additionally, operating the generator in an overrunning mode (higher master clock frequency) allows finer frequency resolution and phase accuracy. This adaptability, along with low power consumption, makes the sequence generator ideal for energy-constrained applications like biomedical sensing, wearable devices, and low-activity monitoring systems. The power consumed by the sequence generator is amortized across all channels, significantly enhancing overall efficiency.

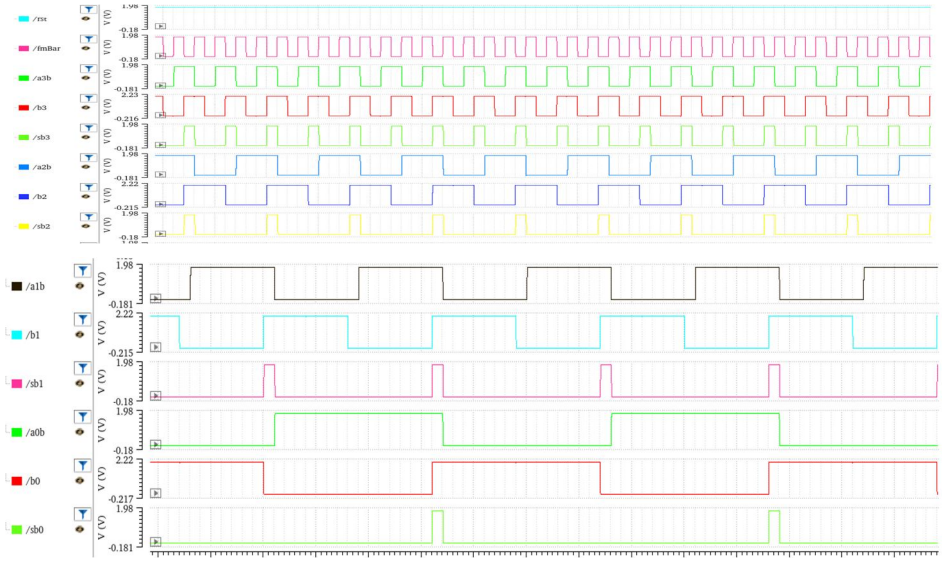


Fig.4 Sequence Generator

D. Pseudo Digitally Controlled Oscillator

The Pseudo-Digitally Controlled Oscillator (pseudo-DCO) is a fully digital circuit that translates a digital input into a frequency-modulated output without relying on analog components. It operates using a sequence generator, which derives four non-overlapping timing signals (eigen rates) by dividing a main clock frequency (e.g., fm/2, fm/4, fm/8, fm/16). A 4-bit input determines which of these signals are selected—each '1' enables a corresponding frequency, and the chosen signals are combined through digital logic (such as OR gates) to produce a single pulse train. The output frequency increases with the number of active signals, making it proportional to the digital input.

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While efficient, this architecture can introduce phase error due to the uneven spacing of output pulses. To mitigate this, a technique called overrunning is used, where the pseudo-DCO operates at a higher internal frequency and is slowed digitally using a counter, enhancing output stability and accuracy. Being entirely digital, the pseudo-DCO offers advantages such as reduced power consumption, lower area and better compatibility with advanced CMOS processes.

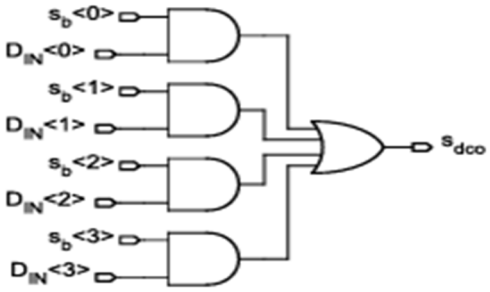


Fig. 5 Pseudo Digitally Controlled Oscillator

E. Subtractor Block

In VCO-based ADCs, the SUB0 and SUB1 blocks are critical to the digital feedback and output paths. SUB0 operates as a modulo subtractor, comparing the current VCO counter output (CNT0) with the previous pseudo-DCO output (Sb) to compute quantization error within a fixed bit range, ensuring overflow protection and enabling efficient digital feedback. SUB1 functions as a digital differentiator, computing the difference between successive pseudo-DCO outputs to implement first-order noise shaping, effectively pushing quantization noise out of the signal band. Together, SUB0 and SUB1 enable delta-sigma-like behaviour entirely in the digital domain, enhancing power efficiency, scalability and resolution making the architecture well-suited for biomedical, sensor, and IoT applications.

F. NON POWER GATED VCO

The image shows the circuit diagram of a current-starved ring oscillator using differential logic with stacked PMOS (Mp) and NMOS (Mn) transistors, where power gating and voltage-controlled delay elements regulate the oscillation frequency, producing a periodic output signal (Fout) in response to the input control voltage (Vin)[13].

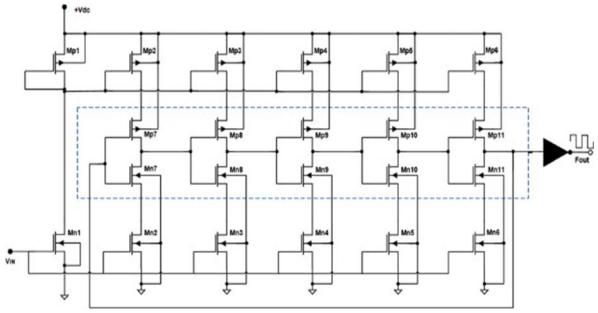


Fig.6 Non Power Gated VCO

Table 2 Working Operation Of Non Power Gated VCO

Phase	Active Transistors	Description
Startup	Mp1, Mn1 ON; others OFF	Circuit initializes and prepares for oscillation.
Charging Phase	Mp2–Mp6 ON; Mn2–Mn6 OFF	PMOS transistors charge the capacitors.
Discharging Phase	Mp2–Mp6 OFF; Mn2–Mn6 ON	NMOS transistors discharge the capacitors.

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A. Second Order True VCO ADC Applying Digital PSEUDO DCO

The second-order true VCO-based ADC with a digital pseudo-DCO converts an analog input into a frequency using a VCO, followed by digitization through counting. A digital subtractor compares this output with pseudo-DCO feedback, modulating the oscillator accordingly. The result is sampled and differenced to achieve second-order noise shaping, enabling efficient, low-power analog-to-digital conversion using primarily digital circuitry[1].

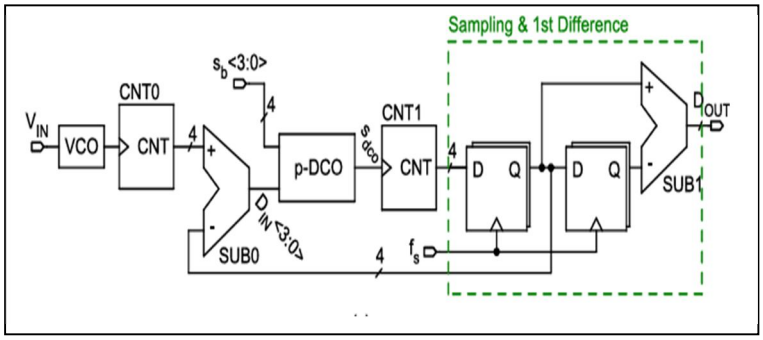


Figure 7 Proposed Second Order True VCO ADC Applying Digital Pseudo DCO

III.RESULTS AND DISCUSSION

The proposed Second-Order VCO-based ADC, featuring a power-gated seven-stage ring VCO and a pseudo-Digitally Controlled Oscillator (pseudo-DCO), was successfully implemented using 45-nm CMOS technology in the Cadence Virtuoso design environment. The simulation results confirm the effectiveness of the power-saving techniques and the accuracy of the analog-to-digital conversion process.

A. Power Gated VCO ADC

The proposed second-order low-power VCO-based ADC, incorporating a power-gated seven-stage ring oscillator and a fully digital pseudo-DCO, was successfully implemented and simulated using 45 nm CMOS technology in the Cadence Virtuoso environment. Comprehensive simulation results validate the architecture's effectiveness in reducing power consumption, ensuring linearity, and supporting digital scalability

B. Frequency To Digital Converter

The FDC accurately counts the pulses generated by the VCO within a defined sampling period. Its digital output increases monotonically with the control voltage, confirming reliable frequency quantization. The reset mechanism ensures clean initialization between measurement cycles, contributing to high precision and stability.

C. ADC Transfer Characteristics

The integration of the VCO and FDC results in a compact and efficient time-domain ADC. The digital output is directly proportional to the analog control voltage (Vin), indicating consistent frequency-to-digital conversion.

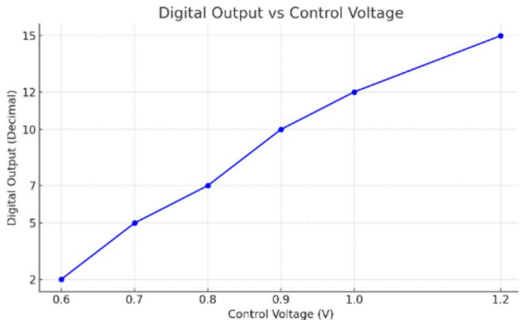


Fig.8 Digital Output Vs. Control Voltage

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As Vin increases from 0.6 V to 1.2 V, the digital output linearly rises from 2 to 14, indicating that the ADC provides accurate and proportional voltage-to-digital conversion suitable for precise low-power sensing applications.

D. Frequency Response Analysis

Three different VDC supply levels (0.9 V, 1.0 V, and 1.2 V) were applied to assess the frequency response. In all cases, the oscillation frequency increased monotonically with the control voltage.

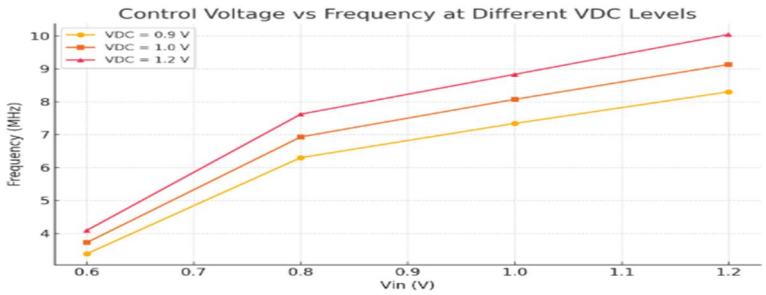


Fig.9 Frequency Vs. Control Voltage

As the control voltage Vin increases from 0.6 V to 1.2 V, the output frequency ranges approximately from 3.4 MHz to 8.3 MHz (at VDC = 0.9 V), 3.7 MHz to 9.1 MHz (at VDC =1.0 V) and 4.1 MHz to 10.0 MHz (at VDC = 1.2 V).
This demonstrates a consistent, monotonic rise in frequency with increasing input voltage and supply level, ideal for precision ADC applications.

E. Second Order Power Gated ADC Output With PSEUDO DCO

The graph shows the relationship between Control Voltage (Vin) and Digital Output for the pseudo-DCO stage of the ADC. As Vin increases from 0.6 V to 1.2 V, the digital output rises from 6 to 11, indicating a monotonic response.

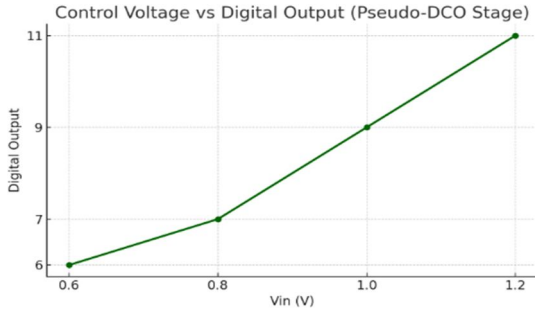


Fig 10 Digital Output with Pseudo DCO Vs. Control Voltage

F. Non Power Gated VCO ADC

The graph illustrates the relationship between Control Voltage (V) and VCO Output Frequency (MHz). As the control voltage increases, the oscillation frequency rises, demonstrating the voltage-controlled tuning behaviour of the VCO.

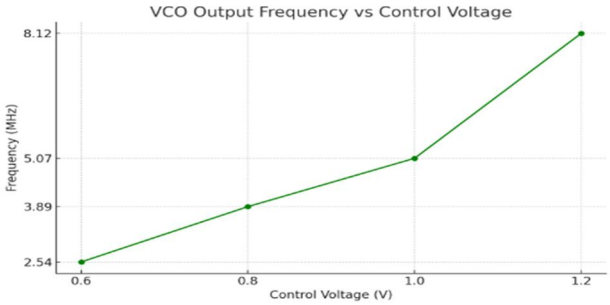


Fig.11 Frequency Vs. Control Voltage

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G. *Second Order Non Power GATED ADC With PSEUDO DCO*

The graph shows the relationship between Control Voltage (V) and Digital Output (Decimal). As the control voltage increases, the digital output rises, reflecting the behaviour of a voltage-to-digital conversion in a VCO-based ADC.

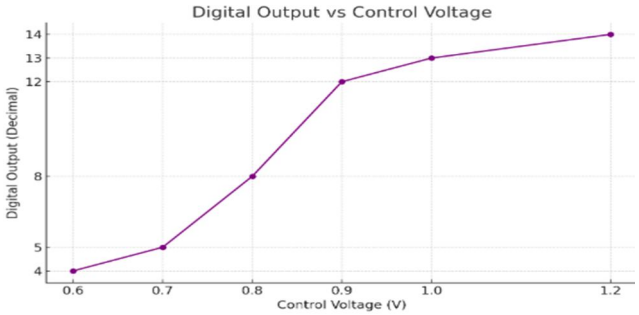


Fig.12 Digital Output with Pseudo DCO Vs. Control Voltage

H. *Power Comparison*

The following comparison underscores the substantial efficiency gains from power gating. The designed VCO employs MCML logic combined with power gating and pull-up sleepy techniques. The simulation results confirm that the oscillator operates correctly, exhibits expected behaviour during both active and sleep modes. Sleep transistors effectively isolate idle blocks, significantly reducing leakage current. The data shows a 67.8% reduction in static power and 60.2% reduction in dynamic power compared to the non-power-gated counterpart. This highlights the power-gated VCO's superior energy efficiency and makes it highly suitable for ultra-low-power applications.

Table 3 Power Comparison

Parameter	Power-Gated VCO ADC	Non-Power-Gated VCO ADC
Technology Node	45 nm CMOS	45 nm CMOS
Supply Voltage	1.0 V	1.0 V
VCO Architecture	Power-Gated 7-Stage Ring VCO	5-Stage Ring Current Starved VCO
ADC Architecture	VCO + Digital Pseudo-DCO	VCO + Digital Pseudo-DCO
ADC Order	Second-order	Second-order
Digital Resolution	4-bit output	4-bit output
Sampling Rate	1 MHz	1 MHz
Static Power (µW)	268.3	832.8
Dynamic Power (µW)	101.6	255.3
Total Power (µW)	369.9	1088.1

IV. RESULTS AND DISCUSSION

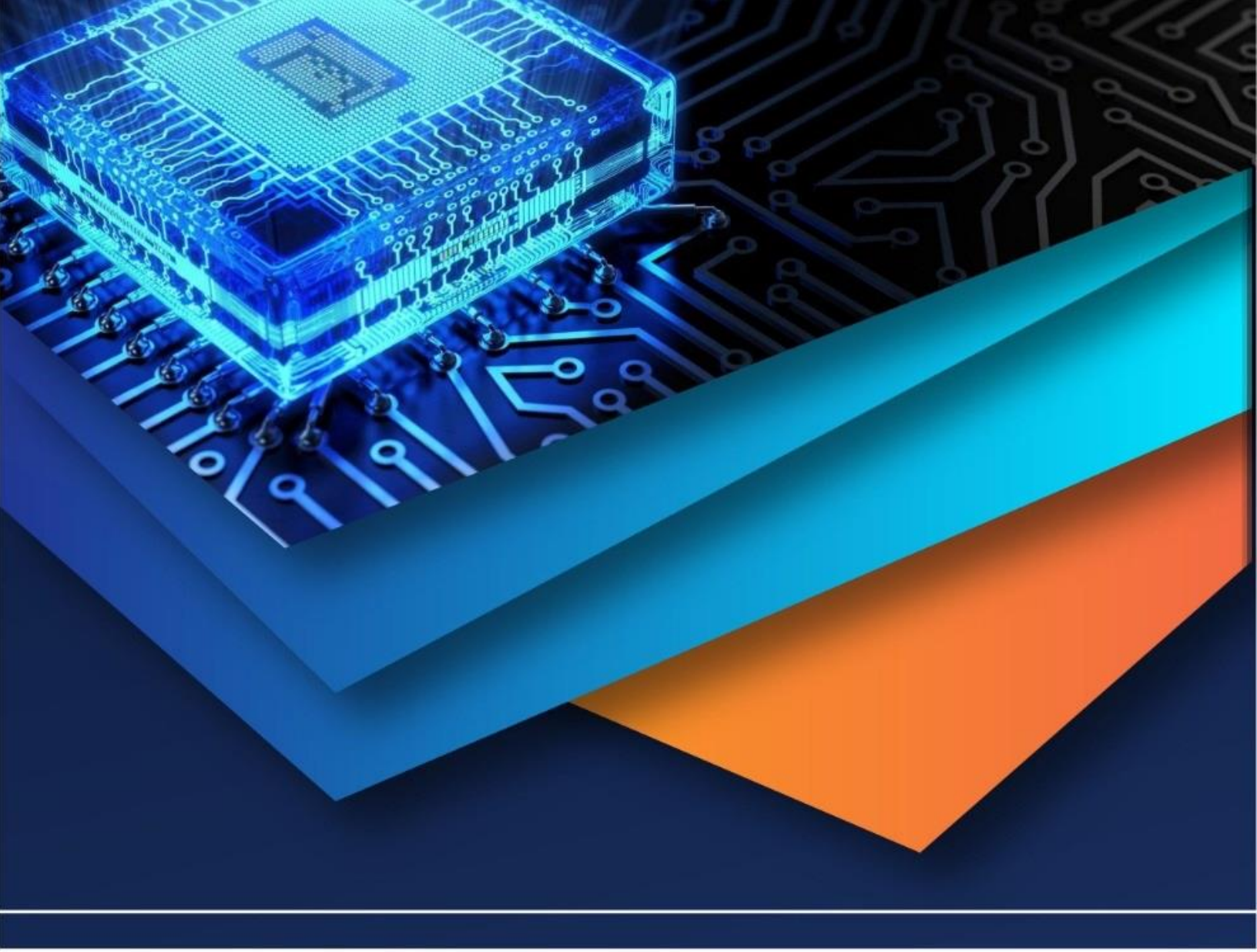
This paper presents a power-efficient, second-order VCO-based ADC architecture that integrates a power-gated, current-starved 7-stage ring VCO using MCML and a fully digital pseudo-DCO, implemented in 45 nm CMOS technology. By incorporating sleep transistors and hardware-level gating, the design achieves a 66% reduction in total power consumption—dropping from 1088.1 µW to 369.9 µW—while maintaining 4-bit resolution and a 1 MHz sampling rate. The scalable pseudo-DCO supports binary-weighted frequency generation, dynamic resolution control via Over-Running Ratio (ORR) tuning, and efficient multi-channel sharing, enhancing flexibility for SoC integration. By seamlessly combining digital control, frequency-domain processing and power-optimized circuit techniques, the proposed ADC delivers a compact, high-performance solution ideally suited for next-generation ultra-low-power applications in biomedical monitoring, wearable systems and IoT edge platforms.

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