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A Survey of Power Reduction Techniques for Ad-Hoc Wireless Sensor Networks

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Abstract: ***Wireless sensor networks (WSN) are the promising technology for telecommunication and network industry. It is provided with great potential to solve the number of problems in battlefields and other commercial applications such as traffic surveillance, health controlling, environment monitoring, construction structures, smart homes and offices. Large number of very small size, low cost, low power multifunctional sensor nodes constitute the WSN. These sensors sway the understanding of the physical world by sensing, processing and transmitting the data. The above functions are highly influenced by factors such as power, energy and lifetime of the sensor nodes. This technical paper explores various low power design architectures like reconfigurable hardware, sleep walker, variable dual VDD, modular architecture and folded tree architecture by presenting a comprehensive survey concerning passive and active power control mechanisms in WSN with investigation of the existing solution and evaluation.***

Keywords: Wireless sensor networks, power consumption, low power architectures, FPGA.

I. INTRODUCTION

Wireless sensor networks are the widely used platform to interact with physical world. Low power WSN design allows the wireless sensor networks to be used in applications such as military, agriculture, biomedical, structural and environment monitoring [1]. The major components of the wireless sensor nodes are the sensor, radio and microcontroller unit along with the power supply using battery. But the radio transmission consumes more energy, they must be designed such that they consume minimum power so as to extend the lifetime of the node [2]. The sensor processors are compact and reliable which can combine sensing, computation, storage, communication and power supplies into small form factors [3]. The sensor operation is dependent on power consumption as the sensors are inevitably used in remote area which is difficult to reach. The limitations of the sensors like reduced lifetime and difficulty in replacement has lead to the development in this field. The future emphasis is to increase the lifespan of the sensor with minimal usage of resources in efficient manner for all applications. Each sensor node operates by collecting the information from the surrounding and transfers them to the base station through wireless transmission. Since power required for the sensor node is more, battery is not sufficient due to its limited capacity. Wind and solar energy sources are not reliable to use although these sources are sufficient for WSN. Hence the design of WSN should use the low power architecture [4]. The basic design architecture of the sensor node consist of storage unit, power unit, transceiver, processing unit and sensing unit as shown in the Figure.1. The power generator is connected the power unit to provide power for the sensor node to operate.

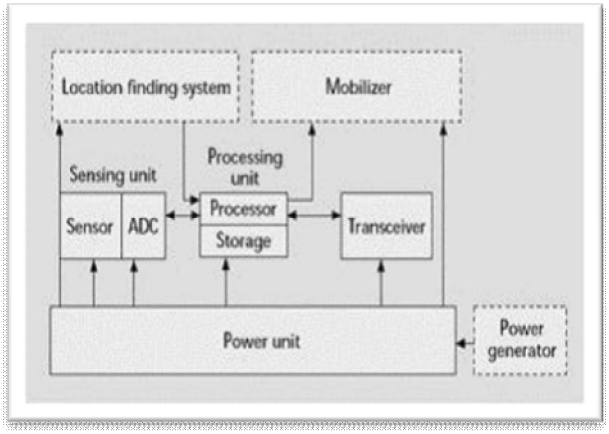


Fig.1 Sensor node architecture.

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The energy usage in sensor nodes can be reduced by reducing the duty cycle, dynamically changing the frequency, tuning the radio transceiver selectively. Xilinx and Altera are the two field programmable gate array (FPGA) major in the semiconductor marketplace as they offer up to 28 nm CMOS technology. This development in semiconductor field leads to produce energy efficient computing platforms. In some situation selective operation is enabled by selectively turning on the specific functional modules. Recent FPGAs includes energy efficient arithmetic components such as adders and multipliers operating at high speed with low power consumption. This paper is organized such that section II comprises of various design of WSN for its low power operation. The conclusion of this survey is given in Section III.

II. LITERATURE REVIEW

The following section consists of several architecture designs for WSN to undergo the survey to obtain the better solution for low power operation of WSN.

A. SNOC Architecture

Robert X. GAO et al developed a new architecture for sensory node controller (SNOC). This node uses dynamic voltage scaling (DVS) mechanism. DVS is used to minimize the energy required for running a given task by dynamically adjusting the supply voltage and the clock speed of the processor according to the time constraints prescribed by each task. Significant energy benefits have been reported by scheduling the computational load and utilizing the CPU idle time. Using DVS the power supply required becomes one fourth of the fixed power supply and the scheduled data acquisition results in the low energy consumption. This mechanism requires special software concept to handle the DVS mechanism in the power unit shown in figure 2. In designing the SNOC software, modularity and flexibility are the main attributes considered for the easy customization and reconfiguration of each SNOC for different applications with minimal overhead. The system-level software architecture of an SNOC is divided into three distinct partitions. The event-based energy control partition activates and controls the DVS algorithm for the SNOC operation. The control response to machine defects reported by the monitoring sensors are initiated at the knowledge-based data processing partition and depends on the relationship between physical signals and machine conditions, which are obtained from experimental studies. The data processing results and corresponding features extracted from the sensor data, the operation mode of a sensory node can be modified *in situ*. For example, when no defect features are identified, SNOC electronics will be forced into the sleep mode by working state control module. Consequently, the energy control module will reduce the supply voltage to the system, thus preserving battery capacity and the programming overhead is increased. This architecture reduces 43% of the energy by comparing with the traditional techniques [5].

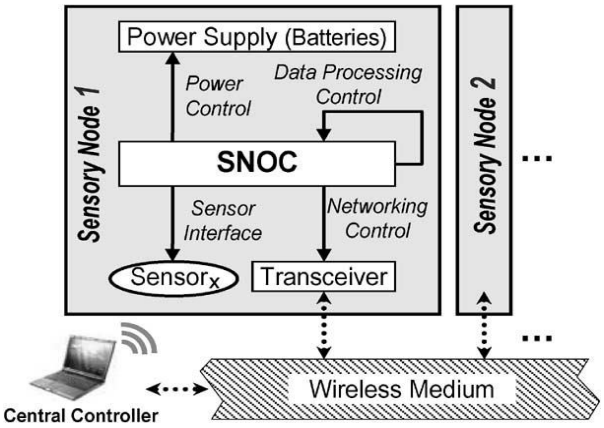


Fig.2 SNOC architecture

B. ASIC Design

Shilong Lu, Xi Huang, Li Cui introduced a new ASIC design of sensor network device in which the power is reduced by "Sleep – Event wake up" low power management mechanism. By the control of the crystal oscillator outside the chip, the clock input is divided into several slots for different power levels. By changing the on/off status of the clock, the power management component can wake up or shut down other modules individually to save energy. If there is any event that needs the CPU to deal with, the CPU can be waken up via the interrupt bus. The design is validated with the FPGA platform [6].

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C. Reconfigurable Hardware Design:

Y. Li Z. Jiao F. Liu S. Xie designed a novel partial dynamic reconfiguration-based WSN node for less power consumption. Internal configuration access port (ICAP) is the mechanism to configure the fabric of Xilinx FPGAs. Through ICAP, the internal registers can be accessed and configuration memory can be read and wrote. The ICAP wrapper is the module containing hardware controllers, which function as interaction between the software and ICAP. The ICAP wrapper and ICAP are contained in a module named ICAP Hardware system which is integrated with the rest WSN node. Inside ICAP wrapper, ICAP decoder is the main controller. It distinguishes the data as instructions and data, which are used as partial design reconfiguration (PDR) and send the signal to the corresponding modules in ICAP wrapper. The address controller and ICAP controller are used to control the flow of data within ICAP wrapper as the data can be both sent to the ICAP primitive or read back from ICAP. The data to ICAP primitive is the configuration file for FPGA configuration. The read back data represents the particular design of application for a region of the FPGA, which are pre-stored in configuration memory or data from the internal registers of ICAP. The dual port blocks ram (BRAM) works as buffer memory. Data to be written into ICAP or read back from ICAP are temporally stored into BRAM before it is used. For communicating, ETRX2 module from Telegesis is utilized as it is based on ZigBee and a low-power implementation. Through universal asynchronous receiver transmitter (UART) port, the module is managed by processor. Approximately 31 to 829 mW power can be saved for each implementation. The reconfigurable hardware design is given in figure 3 in which the ICAP mechanism is implemented in the ICAP system processor module.

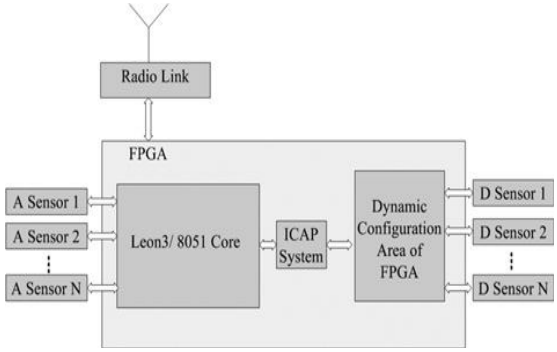


Fig.3 Reconfigurable Hardware Design

The major part of the processing work is carried by FPGA, which can be configured through JTAG (joint test action group) port. In the second solution, the power consumption significantly reduces. The 8051 core consumes less power than Leon core. The total energy saved is nearly 60% [7].

D. Modular Architecture

Rafael et al developed the architecture to reduce the power consumption by designing a miniaturized 3D architecture using cubic structure. The cubic structure full-fills the entire power requirement by the in-built battery by partitioning the node into six functional sub modules such as Sensing, Signal Conditioning, Processing, RF Link, Power and Spare. The first five are the basic building blocks of a standard node. The Spare sub module could be used for extra sensors, antenna mounting, extra memory, programming test connectors or other required extra functions. Each sub module is allocated to a separate circuit board.

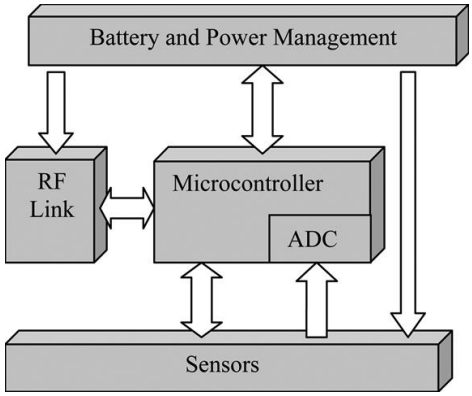


Fig.4: Modular architecture

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In the cubic structure, each board is of same size and has same pattern of I/O pads on one, two, or all four sides. This allows the use of a common "bus" layout between each board with a common allocation of power, ground and I/O positions on the "bus." The "bus" is implemented by a short length of single-sided flexible PCB interconnecting each board with its neighbor(s) in an overall cruciform rigid-flex assembly. The battery receptacle is a simple plastic frame. The six circuit boards, interconnected by flex PCB, are folded around the battery receptacle to completely enclose it. Contact to the battery is made by simple spring contacts on the back of the "top" and "bottom" circuit boards. The circuit boards can be clipped, screwed, or (in the case of rechargeable batteries) permanently fixed in place [8].

E. SRAM- FPGA-based Design

Muhammad Imran et al introduced energy-efficient SRAM FPGA-based wireless vision sensor node (VSN). VSN is designed using static RAM (SRAM) based FPGA when compared to FLASH based FPGA. For conserving energy, the VSN can be switched to a low-power state, referred to as the sleep state, when the required vision tasks have been performed. In sleep state, only the real-time counter is ON in order to keep track of the timing, whereas all other components, i.e., FLASH, FPGA, SRAM, and transceiver are OFF. The minimum sleep duration should be 235 ms in order to effectively utilize the SRAM-based FPGA for duty-cycled VSN applications. The average power consumed is 670 mW. The life time of the microcontroller is ~3.2 years [9].

F. Near-threshold Design

Jos Hulzink et al proposed design low power wireless sensor node for biomedical applications. This follows the data driven operations and single instruction multiple data (SIMD) mechanism. The low power consumption is achieved by power optimization at different abstraction layers including application optimization and mapping, system partitioning for effective duty cycling, multi-layer extensive clock gating, circuit level optimization for operating at near threshold and low power on-chip clock generation. There are 15 power domains. The data and program memories are divided into 13 different memory banks which can be individually put in retention mode or switched on or off. The processor is in a separate power domain without retention mode and can be only powered on or off. The rest of the system, including the peripherals, is in one power domain (the periphery domain) which is always on. To control the different domains, the power manager is equipped with two sets of configuration registers. One contains the configuration when the processor is running (awake), the other is used when the processor is switched off and the chip is in data collection mode (asleep). The power manager switches automatically to the asleep state when the processor finishes its running task and back to the awake state when the interrupt controller indicates there is an interrupt pending for the processor. The dynamic power consumed by these sensor nodes vary for different operating modes. High performance consumes more energy than the low performance and the data collection applications. A 13 pJ/cycle of power is achieved for single lead ECG [10].

G. Variable Dual Vdd Architecture:

Jianfeng Zhu et al proposed low power reconfigurable processor utilizing variable dual VDD. The power is reduced by applying variable dual-VDD method. The granularity of dual *V*DD is selected to be the interconnect, because this module is more power efficient than the ALU. Its POWER/DELAY is ten times larger than that of the ALU. The preferred design is to configure dual VDD for the interconnect rather than the ALU. As shown in figure 5.a two selecting transistors and 2-bit configurations are required to choose power supply from VDDH (the higher VDD) and VDDL and power gating for each interconnect instance. The additional cost of the variable dual-VDD method is an adjustable dc–dc converter. The buck converter and control circuits are adopted to generate the variable VDDL. Its input *N* is provided by a compiler. The output VDDL can be adjusted through software control. The power consumed is 1.2 μW when 0.7 volt is applied [11].

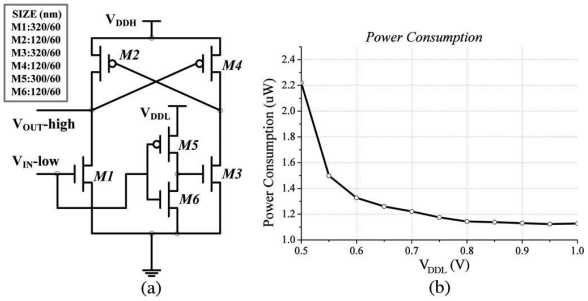


Fig. 5. (a) CLC. (b) Power of CLC as a function of *V*DDL.

The advantages and disadvantages of the various surveyed papers are given in Table-1.

Table 1: COMPARISON OF LITERATURE SURVEY

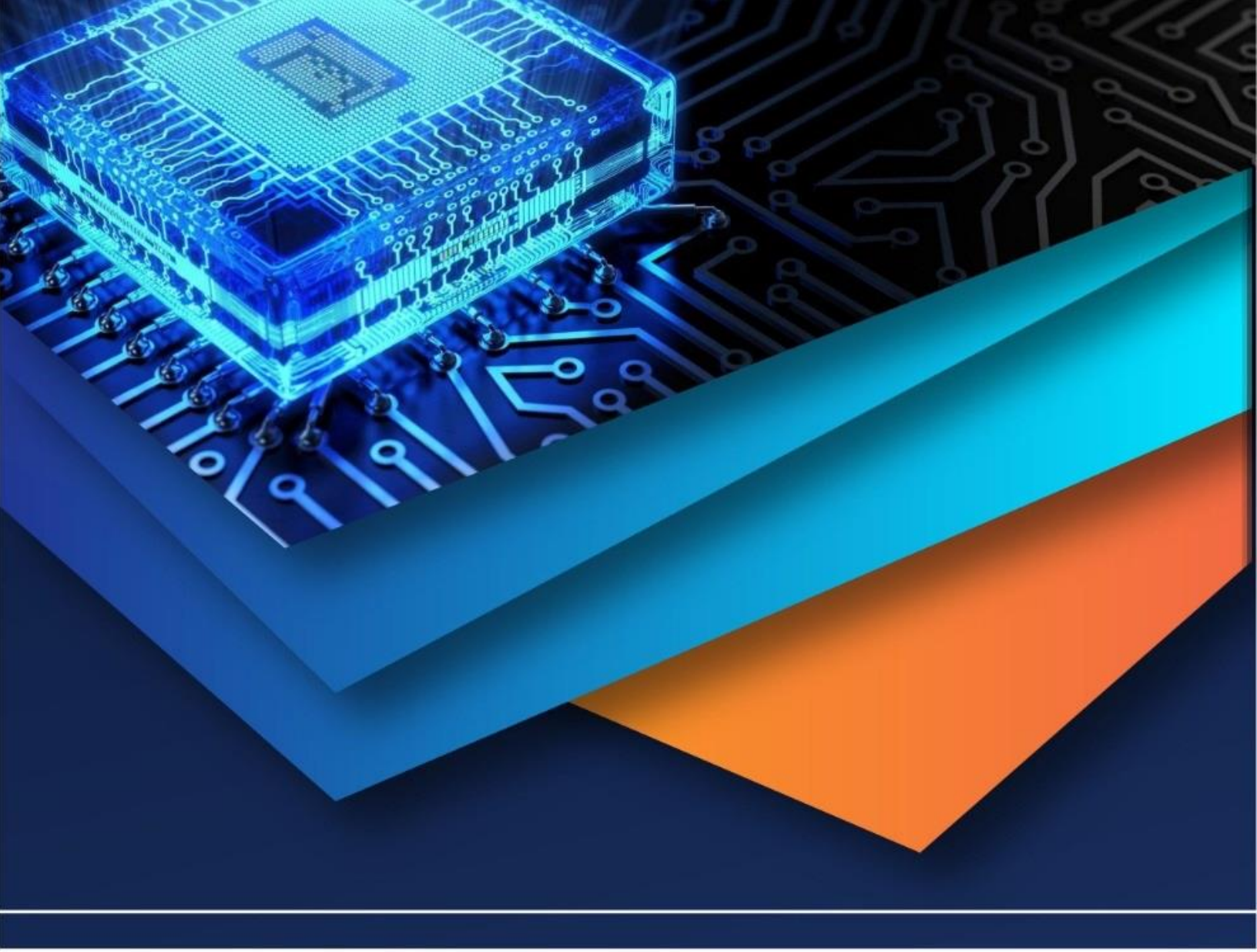
Ref. No	METHODOLOGY	PROS	CONS
[5]	Dynamic voltage scaling(DVS)	✓ Required power is one fourth of the fixed power supply.	❖ Increases the programming overhead.
[6]	Sleep –event wake up	✓ Security using un-resemble coder algorithm	❖ Applicable only for specific applications
[7]	Reconfiguring the hardware.	✓ Less area complexity	❖ Disconnection while programming.
[8]	Built-in battery in wireless sensor node	✓ No external battery requirement	❖ Needs a systematic approach to integrate the battery.
[9]	SRAM FPGA based WSN	✓ Life time is extended.	❖ Generic architecture supporting only duty cycling applications.
[10]	Data driven mechanism	✓ Very less power consumption	❖ Partitioning of the circuit.
[11]	Variable dual-VDD method.	✓ CMOS transistors are used.	❖ Requires reconfigurable processor

III. CONCLUSION

Power consumption is the vital factor to be considered in recent years, many researches are concentrating on low power architectures. Power consumption influences the performance and the lifetime of the sensor nodes in WSN. Various design architectures are surveyed and compared in this technical paper in terms of power and energy consumption. The above surveyed papers present the low power design along with other features such as lifetime enhancement, low area complexity.

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