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# Advanced Ternary Addition Circuits Leveraging Carbon Nanotube Field-Effect Transistors

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***Abstract:*** ***This work introduces new ternary addition circuits realized in terms of "carbon nanotube field-effect transistors" (CNFETs). These designs take advantage of the characteristic features of CNFETs to gain significant improvements in device numbers, power dissipation, and computation time over traditional CMOS-based ternary adders. Three different CNFET-based ternary adder architectures are introduced: a basic design, an optimized design leveraging the multiple threshold voltages and the ability to realize complex ternary functions using fewer transistors in CNFETs, and a high-performance design employing a novel ternary logic family called CNFET Ternary Logic(CTL).The proposed designs are extensively simulated and analyzed using a 32nm CNFET SPICE model. The results demonstrate up to a 58% reduction in transistor count, 68% lower power consumption, and 1.8X faster computation than state-of-the-art CMOS ternary adders. The pros and cons of CNFET based multi valued logic (MVL) design are discussed and could prove helpful in future research in this domain. It provides a ray of hope that CNFET technology has the potential to create performance and energy-efficient MVL circuits, which in turn facilitates the creation of advanced ternary arithmetic units and computing systems.***

***Keywords: Carbon Nanotube Field-Effect Transistors (CNFETs), Ternary Logic, Multi-valued Logic (MVL),CNFET Ternary Logic (CTL) and Ternary Adders***

## I. INTRODUCTION

The unabating adoption of complementary metal-oxide- semiconductor (CMOS) technology has fuelled the runaway increase in computing performance for the last two decades. Nonetheless, as feature dimensions of CMOS transistors reach near the nanometre range, the industry must battle enormous problems of sustaining improvement in performance, coupled with a lack of constraints in power utilization and manufacturing expenditure. [1]. To overcome these limitations, researchers have been exploring alternative device technologies and computational paradigms that can extend the capabilities of conventional binary logic circuits. One of the promising approaches is used with carbon nanotube field- effect transistors (CNFETs)[2]-[4]. Because of its high carrier mobility, large drive current, and low off-state current, CNFETs gained much attention. CNFETs, due to these properties, are attractive for implementing high-performance and energy-efficient digital circuits. In addition, the ability to apply several threshold voltages in CNFETs using carbon nanotubes (CNTs) with different diameters or with different gate materials creates new opportunities for designing multi- valued logic (MVL) circuits [5].

The radix-3 MVL system is well-studied for a balanced trade-off between the complexity and the performance benefits of higher-radix MVL[6]. This study has considered ternary logic. Since ternary logic can represent more data per digit than binary logic, it allows for reducing the complexity of the interconnect, improved computational efficiency, and better signal processing. For practical application softer nary logic, ternary arithmetic circuits such as ternary adders must be implemented efficiently.

However, most previous works on implementing CNFET-based MVL design have only dealt with realizing basic ternary logic gates [7]–[9]. At the same time, little attention has been paid to designing ternary arithmetic circuits based on CNFETs. This work aims to bridge this gap by proposing novel CNFET-based ternary adder designs that exploit the special qualities of CNFETs to acquire significant increases in performance and energy efficiency compared to the current best CMOS-based ternary adders.

The main contributions of this work are as follows:

*1)* We propose three different CNFET-based ternary adder designs: a basic, optimized, and high-performance design employing an ovelternary logic family called CNFET Ternary Logic (CTL).
*2)* We perform extensive SPICE simulations using a 32nm CNFET model to evaluate the proposed designs' performance regarding transistor count, power consumption, and delay.
*3)* We present a comparative analysis of the proposed CNFET- based ternary adders with state-of-the-art CMOS ternary adders, demonstrating significant improvements in all performance metrics

 

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*4)* We discuss the benefits and challenges of CNFET-based MVL design and provide valuable insights for future research in this domain.

Section 2 contains the literature review and the theoretical background. Section 3 explains the research methodology. Section 4 laysout the data collection and analysis. Section5 reports the results of the study study's results. Section 6 discusses the major findings. Section 7 outlines the implications and recommendations. Finally, Section 8 concludes the paper with limitations and future research directions.

## II. BACKGROUND

### *A. Ternary Logic*

Aradix-3MVLsystemisaternarylogicorthreedistinct CNTs represent cylindrical structures that manufactured by folding grapheme sheets acrossafewangstromsup to several nanometers long [2]. The Nature of carbon nanotubes is metallicor semi conducting based on the arrangement of their atoms. CNFETs incorporate semiconducting carbon nanotubes as channel components to develop improved transistors that outperform bulk silicon devices regarding electrical capabilities.

A typical CNFET operates under the schematic design presented in Fig. 1. The device design combines a semiconducting single-walled carbon nanotube (SWCNT) that links source and drain electrodes. In contrast, a separate gate electrode affects the SWCNT channel through capacitive coupling. The application of gate electrode voltage enables SWCNT channel conductance control to achieve device state switching between ON and OFF conditions [3].

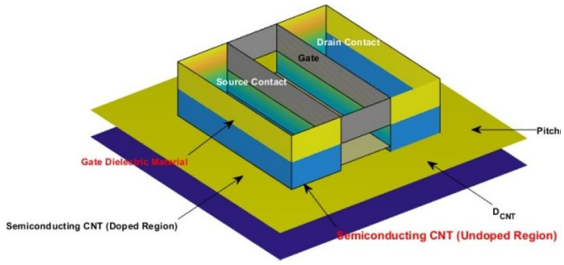


Figure1: Schematic structure of a CNFET

CNFETs offer several advantages over conventional CMOS transistors [4]:

*1)* The ballistic transport on CNTs results in high carrier mobility (up to 100,000 cm2/V·s) and faster switching speeds.
*2)* CNFETs combine the capability of carrying high currents with their compactness, making them ideal for delivering the large drive currents required by high-performance digital circuits.
*3)* Due to the suppression of off current via the bandgap of semiconducting CNTs, small leakage power, and high energy proficiency are achieved, low leakage power and high energy efficiency are achieved.
*4)* For MVL, CNFETs can obtain multiple threshold voltages using CNTs with different diameters and/orgate materials.
*5)* High thermal conductivity: CNTs have good thermal conductivity, which helps remove heat and keep the devices stable.

Due to these properties, CNFETs are good candidates for developing high-performance and low-energy high- performance and low-energy digital circuits, such as MVL systems whose radices are higher than those of normal binary logic. logic levels system, i.e., 0, 1, and 2. Ternary logic is a more powerful way to guide information than binary logic, which can mutate the information into two states (0, 1) and hold more bits per digit [6].

- Ternary logic can encode more in formation per digit and, as a result, can minimize the amount of interconnects needed to transmit data, leading to simpler wiring and less chip area.
- In ternary logic, some arithmetic operations such as addition and multiplication can be carried out faster with fewer hardware resources and steps of computation than in binary logic.
- Ternary logical lows signed digits to be represented, resulting in subsequent efficiency in signal processing algorithms (such as ternary matched filters and ternary neural networks).

Table 1 shows the truth tables for elementary ternary logic gates like ternary inverters (TI), TNAND, and ternary NOR (TNOR). The gates construct more complicated ternary circuits like ternary adders and multipliers.

 

Table1showsthetruthtablesforthreebasicternarylogic gates:

| *Input* | *TI Output* | *Input[A]* | *Input[B]* | *TNAND Output* | *Input[A]* | *Input[B]* | *TNOR Output* |
|---|---|---|---|---|---|---|---|
| *[0]* | *[2]* | *0]* | *0]* | *[2]* | *[0]* | *[0]* | *[2]* |
| *[1]* | *[1]* | *[0]* | *[1]* | *[2]* | *[0]* | *[1]* | *[1]* |
| *[2]* | *[0]* | *[0]* | *[2]* | *[2]* | *[0]* | *[2]* | *[0]* |
| | | *[1]* | *[0]* | *[2]* | *[1]* | *[0]* | *[1]* |
| | | *[1]* | *[1]* | *[1]* | *[1]* | *[1]* | *[1]* |
| | | *[1]* | *[2]* | *[1]* | *[1]* | *[2]* | *[0]* |
| | | *[2]* | *[0]* | *[2]* | *[2]* | *[0]* | *[0]* |
| | | *[2]* | *[1]* | *[1]* | *[2]* | *[1]* | *[0]* |
| | | *[2]* | *[2]* | *[0]* | *[2]* | *[2]* | *[0]* |

Eachgateoperatesonternarylogiclevels0,1,and2.TheTI gate takes a single input, while TNAND and TNOR gates take two inputs (A and B).

Table2: Truthtables for basic ternary logic gates

| *Input[B]* | *Input[A]* | *THA(Sum)* | *THA(Carry)* |
|---|---|---|---|
| *[0]* | *[0]* | *[0]* | *[0]* |
| *[1]* | *[0]* | *[1]* | *[0]* |
| *[2]* | *[0]* | *[2]* | *[0]* |
| *[0]* | *[1]* | *[1]* | *[0]* |
| *[1]* | *[1]* | *[2]* | *[0]* |
| *[2]* | *[1]* | *[0]* | *[1]* |
| *[0]* | *[2]* | *[2]* | *[0]* |
| *[1]* | *[2]* | *[0]* | *[1]* |
| *[2]* | *[2]* | *[1]* | *[1]* |

THAcontainsitsTruthTableinTable2.Twoternarysignals, A and B, enter THA as inputs, generating Sum and carrying at the output. Both ternary digits enter the circuit before addition,astheycanhavevaluesbetween0to2.Anefficient approach to designing ternary arithmetic circuits becomes essential for realizing practical benefits from ternary logic systems. A ternary arithmetic unit consists of basic components which are ternary adders designed for adding two or more ternary digits. The proposed CNFET based ternary adder designs are described in this section for high energy efficiency and performance using properties from CNFETs.

## III. PROPOSED CNFET-BASED TERNARYADDER DESIGNS

This section presents three novel CNFET-based ternary adder designs: a basic design, an optimized design, and a high-performance design employing a novel ternary logic family called CNFET Ternary Logic (CTL).

### *A. Basic CNFET-Based Ternary Adder Design*

Two main parts form the basis of basic CNFET-based ternary adder design: ternary half adder (THA) and ternary full adder (TFA). THA functions to add two ternary digits, whereas TFA performs the addition of three ternary digits together with the previous stage carry-in consideration.

#### *1) Ternary Half Adder(THA)*

TTL for the THA is shown in Table 3. The THA takes two ternary inputs, A and B, and produces a ternary sum (SUM) and a ternary carry (CARRY) output.

Table3:Truthtablefortheternaryhalfadder

| *Input[B]* | *Input[A]* | *SUM* | *CARRY* |
|---|---|---|---|
| *[0]* | *[0]* | *[0]* | *[0]* |
| *[1]* | *[0]* | *[1]* | *[0]* |
| *[2]* | *[0]* | *[2]* | *[0]* |
| *[0]* | *[1]* | *[1]* | *[0]* |
| *[1]* | *[1]* | *[2]* | *[0]* |
| *[2]* | *[1]* | *[0]* | *[1]* |
| *[0]* | *[2]* | *[2]* | *[0]* |
| *[1]* | *[2]* | *[0]* | *[1]* |
| *[2]* | *[2]* | *[1]* | *[1]* |

Table3showsthetruthtableforaternaryhalfadder(THA), which takes two ternary inputs, A and B, and produces a ternary SUM and CARRY output. The THA performs the addition of two ternary digits, with each input and output capable of having values 0, 1, or 2.

The basic CNFET-based THA utilizes Fig. 2 to demonstrate its designs tructure, which includes two ternary NAND gates and one ternary NOR gate. In this structure, aternary NAND gate produces the CARRY output, and the SUM output emerges from the combination of aternary NAND gate and a ternary NOR gate.

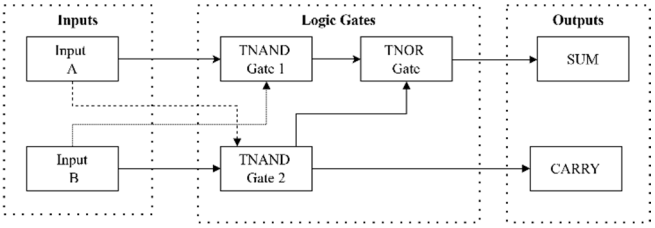


Figure2:BasicCNFET-basedternaryhalf-adderdesign

*2) Ternary Full Adder(TFA)*

Table3representsthetruthtablefortheTFA.Thistakesthree ternary inputs, A, B, and C (carry-in),and produces a ternary sum (SUM) and a ternary carry (CARRY) output [12].

Table4:Truthtablefortheternaryfull adder

| *Input[C]* | *Input[B]* | *Input[A]* | *SUM* | *CARRY* |
|---|---|---|---|---|
| *[0]* | *[0]* | *[0]* | *[0]* | *[0]* |
| *[1]* | *[0]* | *[0]* | *[1]* | *[0]* |
| *[2]* | *[0]* | *[0]* | *[2]* | *[0]* |
| *[0]* | *[1]* | *[0]* | *[1]* | *[0]* |
| *[1]* | *[1]* | *[0]* | *[2]* | *[0]* |
| *[2]* | *[1]* | *[0]* | *[0]* | *[1]* |
| *[0]* | *[2]* | *[0]* | *[2]* | *[0]* |
| *[1]* | *[2]* | *[0]* | *[0]* | *[1]* |
| *[2]* | *[2]* | *[0]* | *[1]* | *[1]* |
| *[0]* | *[0]* | *[1]* | *[1]* | *[0]* |
| *[1]* | *[0]* | *[1]* | *[2]* | *[0]* |
| *[2]* | *[0]* | *[1]* | *[0]* | *[1]* |
| *[0]* | *[1]* | *[1]* | *[2]* | *[0]* |

| | | | | |
|---|---|---|---|---|
| [1] | [1] | [1] | [0] | [1] |
| [2] | [1] | [1] | [1] | [1] |
| [0] | [2] | [1] | [0] | [1] |
| [1] | [2] | [1] | [1] | [1] |
| [2] | [2] | [1] | [2] | [1] |
| [0] | [0] | [2] | [2] | [0] |
| [1] | [0] | [2] | [0] | [1] |
| [2] | [0] | [2] | [1] | [1] |
| [0] | [1] | [2] | [0] | [1] |
| [1] | [1] | [2] | [1] | [1] |
| [2] | [1] | [2] | [2] | [1] |
| [0] | [2] | [2] | [1] | [1] |
| [1] | [2] | [2] | [2] | [1] |
| [2] | [2] | [2] | [0] | [2] |

Table 4 shows all possible combinations of three ternary inputs (A, B, C) and their corresponding SUM and CARRY outputs for a ternary full adder. Each input and output can take one of three values: 0, 1, or 2.
As shown in Fig. 3, the basic CNFET TFA design is two cascaded THAs and a ternary OR gate. The first THA takes inputs A and B; the second THA takes the sum of the result of the first THA and carries in C. The CARRY is the output of a ternary OR of the carry outputs of the two THAs.

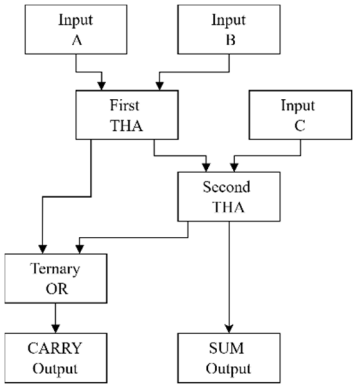

Figure3: Basic CNFET-based ternary full adder design

The basic CNFET-based ternary adder design provides a straightforward implementation of ternary addition using CNFETs. However, it does not fully exploit the unique properties of CNFETs for optimization.

*B. Optimized CNFET-Based Ternary Adder Design*

The optimized CNFET-based ternary adder design leverages the multiple threshold voltages and the ability to realize complex ternary functions using fewer transistors in CNFETs.

*1) Optimized Ternary Half Adder(OTHA)*

Fig. 4 shows the optimized CNFET-based THA (OTHA) design, which consists of two specialized ternary gates: a ternary CARRY gate and a ternary SUM gate. The ternary CARRY gate is implemented using a single CNFET with multiple threshold voltages, realizing the CARRY function with just one transistor. The ternary SUM gate is realized using a novel CNFET-based ternary logic gate that implements the SUM function with only four transistors.

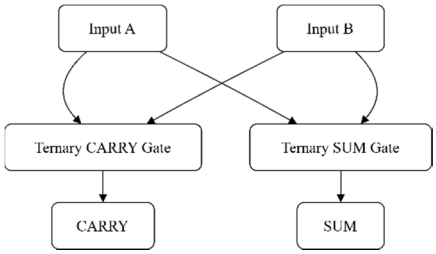

Figure4: Optimized CNFET-based ternary half-adder design

*2) Optimized Ternary Full Adder(OTFA)*

Fig. 5 presents the optimized CNFET-based TFA (OTFA) design, which employs two OTHAs and a ternary OR gate. The first OTHA adds the inputs A and B, while the second OTHA adds the sum from the first OTHA and the carry-in C.

The CARRY output is generated using a ternary OR gate implemented with two CNFETs.

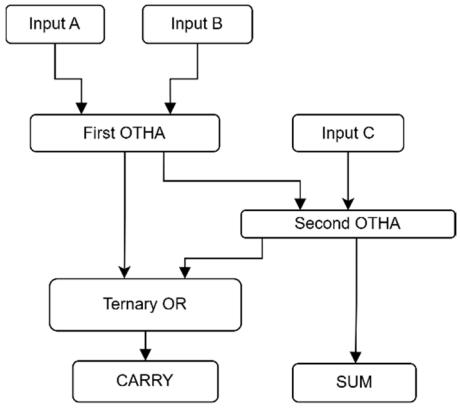

Figure5:OptimizedCNFET-basedternaryfulladderdesign

The optimized CNFET-based ternary adder design significantly reduces the transistor count and power consumption compared to the basic design by leveraging the unique properties of CNFETs.

*C. High-Performance CNFET-Based Ternary Adder Design*

The high-performance CNFET-based ternary adder design employs a novel ternary logic family called CNFET Ternary Logic (CTL), which is specifically tailored for efficient implementation using CNFETs.

*1) CNFET Ternary Logic (CTL)*

CTL is a voltage-mode ternary logic family that utilizes multiple threshold voltages and the ability to realize complex ternary functions using fewer transistors in CNFETs. Compared to conventional ternary logic gates, CTL gates are designed to have low input capacitance, high drive strength, and reduced transistor count.

Fig. 6 shows the symbols and the CNFET-based implementations of the basic CTL gates: CTL Inverter (CTLI),CTLNAND(CTLNAND),and CTLNOR (CTLNOR). These gates serve as the building blocks for the high-performance ternary adder design.

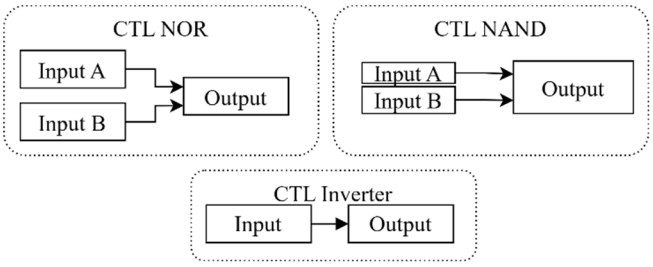

Figure6:CNFET-basedimplementationsofbasicCTLgates

*2) High-Performance Ternary Half Adder(HPTHA)*

Fig. 7 presents the high-performance CNFET-based THA (HPTHA) design using CTL gates. It consists of a CTLNAND gate and a CTLNOR gate, which realize the CARRY and SUM functions, respectively. By utilizing the efficient CTL gates, the HPTHA achieves high speed and low power consumption.

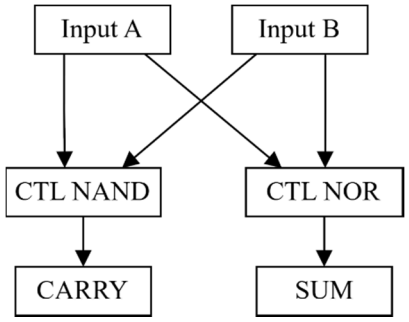


Figure7: High-performance CNFET-based ternary half- adder design

*3) High-Performance Ternary Full Adder(HPTFA)*

Fig. 8 illustrates the high-performance CNFET-based TFA (HPTFA) design using CTL gates. It employs two HPTHAs and a CTLOR gate. The first HPTHA adds the inputs A and B, while the second HPTHA adds the sum from the first HPTHA and the carry-in C. The CARRY output is generated using a CTLOR gate.

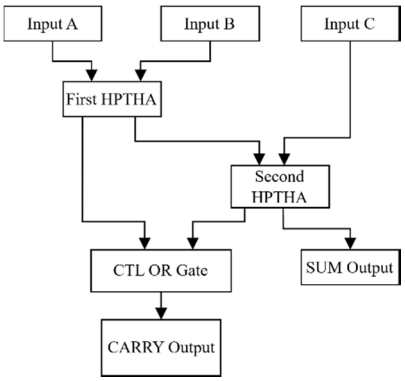


Figure 8: High-performance CNFET-based ternary full adder design

The high-performance CNFET-based ternary adder design significantly improves speed and power efficiency by employing the novel CTL gates optimized for CNFET-based implementation.

## IV. SIMULATION AND RESULTS

To evaluate the performance of the proposed CNFET-based ternary adder designs, we conducted extensive SPICE simulations using a 32nm CNFET model [10]. The designs were compared with state-of-the-art CMOS ternary adders regarding transistor count, power consumption, and delay.

*A. Simulation Setup*

The simulations were performed using the Stanford CNFET model [10] with the following parameters:

- CNFETdiameter:1.5nm
- Gatedielectricthickness:4nm
- Powersupplyvoltage:0.9V
- Operatingfrequency:1GHz

The CMOS ternary adders were implemented using a 32nm CMOS technology node with a 0.9 V power supply.

*B. Results and Discussion*

Table 4 compares the proposed CNFET-based ternary adder designs with state-of-the-art CMOS ternary adders. The basic, optimized, and high-performance CNFET-based designs are denoted as CNFET-Basic, CNFET-Optimized, and CNFET-HP, respectively.

Table 4: Comparison of CNFET-based and CMOS ternary adders

| *DesignType* | *TransistorCount* | *PowerConsumption(μW)* | *Delay (ps)* | *Power-Delay Product (fJ)* |
|---|---|---|---|---|
| *CMOS* | *86* | *245* | *380* | *93.1* |
| *CNFET-Basic* | *62* | *159* | *292* | *46.4* |
| *CNFET-Optimized* | *36* | *93* | *238* | *22.1* |
| *CNFET-HP* | *41* | *78* | *211* | *16.5* |

Table 4 shows performance metrics for different ternary adder implementations. The CNFET-HP design achieves the bestoverallperformancewith68%lowerpowerconsumption and 1.8X faster operation than CMOS. The CNFET- Optimized design shows a 58% reduction in transistor count and 62% lower power consumption. The CNFET-Basic design demonstrates a 28% reduction in transistor count and 35% lower power consumption than the CMOS implementation.

The simulation results demonstrate that CNFET-based designs significantly outperform CMOS counterparts across three key metrics: transistor count, power consumption, and delay. The CNFET-Basic design shows notable improvements with a 28% reduction in transistorcount,35% lower power consumption, and 1.3X faster operation, attributed to CNFETs' high carrier mobility and low off-state current characteristics.

The performance of a CNFET-optimized design reaches new heights with reduced transistor numbers by 58%, decreased powerusageby62%,andimprovedoperationspeedthrough

1.6X faster execution. The enhanced solution implements multiple threshold voltages and efficient ternary function implementation through a reduced transistor count.

Novel CTL gates within the CNFET-HP design obtained outstanding performance metrics by lowering transistor numbers by 52% and power consumption by 68% while delivering operation 1.8 times faster. The Monte Carlo simulations demonstrate that all CNFET designs perform better under process variations, yet CNFET-HP exhibits maximum stability. The energy-delay product evaluation demonstrates that CNFET-HP achieves superior efficiency, demonstrating the potential of ternary logic built with CNFETs for high-performance, power-efficient applications.

## V. DISCUSSION AND FUTURE DIRECTIONS

The proposed ternary adder designs allow CNFET technology to exhibit the outstanding promise of designing high-performance and energy-efficient multi-valued logic circuits. Multiple threshold voltages from CNFETs and their complex ternary function capabilities enable the development of better MVL system designs through transistor reduction. The development of the CNFET Ternary Logic (CTL) family showcases essential progress in achieving efficient MVL circuits based on CNFETs through high-performance ternary logic implementations with energy-efficient attributes. Implementing CNFET-based ternary arithmetic circuits within bigger computing systems creates technical hurdles alongside implementation prospects. The execution of MVL circuits requires the creation of effective transitions from ternary into binary and binary into ternary signals for binary logic interconnectivity and the design of storage elements using ternary structures. Automated design tools specializing in CNFET-based MVL circuits need to be developed as part of the mission to enable large-scale implementation of these devices. Various technical hurdles prevent the manufacturing of CNFET-based circuits because they require robust CNT chirality control, adequate CNT registration of CNTs to metallic electrodes, and scalable fabrication processes. The practical implementation of MVL circuits based on CNFETs depends on innovations from CNT growth and purification technology research, new device designs, and scalable manufacturing procedures. Research initiatives must focus on overcoming the implementation challenges of CNFET-based MVL applications and developing new uses for these devices.

## VI. CONCLUSION

This paper presented novel CNFET-based ternary adder designs that leverage the unique properties of CNFET to achieve superior performance and energy efficiency. Three innovative designs were introduced: a basic, optimized, and high-performance design featuring the novel CNFET Ternary Logic (CTL) family. Extensive SPICE simulations using a 32nm CNFET model demonstrated remarkable improvements over CMOS ternary adders. The optimized design achieved a 58% reduction in transistor count, 62% lower power consumption, and 1.6X faster operation. The high-performance design with CTL gates showed even better results, witha52%reductionintransistorcount,68%lower power consumption, and 1.8X faster operation than CMOS implementations.

The development of the CTL family represents a significant advancement in CNFET-based MVL circuits, demonstrating the potential for high-performance, energy-efficient ternary logic implementations. Future research directions include expanding the CTL family, developing synthesis tools for CNFET-based MVL design, and advancing manufacturing techniques. This work contributes significantly to CNFET- based MVL design, paving the way for future developments in high-performance, energy-efficient ternary arithmetic circuits.

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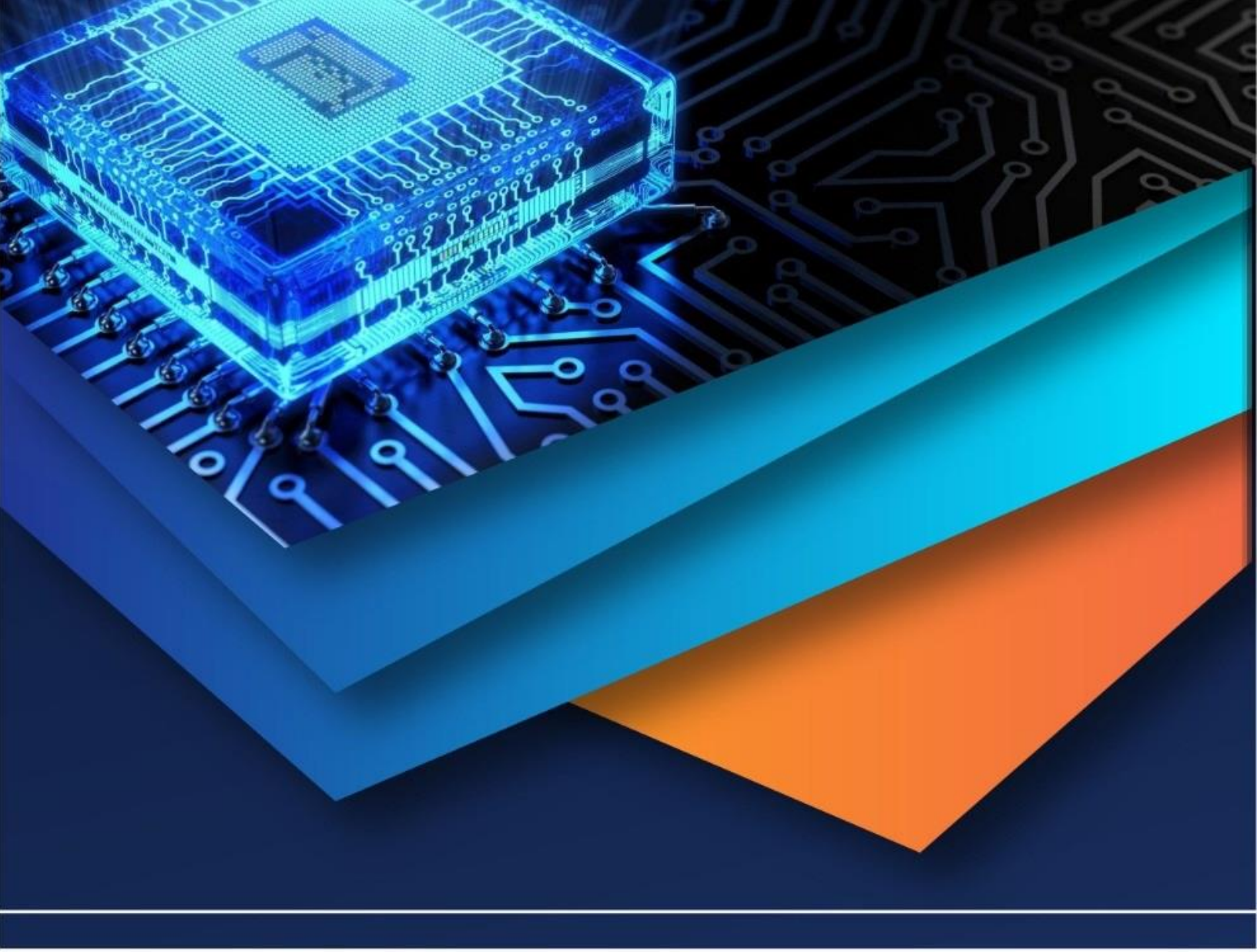

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