iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 13 **Issue:** V **Month of publication:** May 2025

DOI: https://doi.org/10.22214/ijraset.2025.71476

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 13 Issue V May 2025- Available at www.ijraset.com

Advancements in FPGA-Based Design of Fixedpoint FIR Filters for Multirate Signal Processing Applications: A Comprehensive Review

Swati Soni[1], Nisha Chauhan[2], Nidhi Sharma[3]
Department of Electronics and Communication Engineering, Noida Institute of Engineering and Technology,

Abstract: ***Field-programmable gate arrays (FPGAs) have emerged as a pivotal technology in the implementation of digital signal processing algorithms, particularly for fixed-point finite impulse response (FIR) filters in multirate applications. Recent advancements have significantly improved performance, power efficiency, and adaptability in harsh real-time environments. This review synthesizes thirty studies that span innovations in design methodologies, architecture optimization, and practical deployments. It explores fixed-point arithmetic benefits and challenges in FIR filter implementations, discusses multirate signal processing techniques, and identifies emerging trends such as adaptive filter structures and low- latency architectures. Emphasis is placed on FPGA-specific optimizations, including resource utilization and parallel processing strategies. The review concludes by highlighting potential research directions and the need for further integration of artificial intelligence tools to enhance design automation. These insights will benefit researchers and engineers seeking robust, high-performance FPGA designs in complex signal processing environments.***

Keywords: FPGA, fixed-point, FIR filters, multi rate, pipeline, distributed arithmetic, reconfigurable, quantization, low latency, adaptive filtering

I. INTRODUCTION

The rapid evolution of digital signal processing (DSP) techniques over the past decade has been driven by the relentless pursuit of higher performance and lower power consumption. Among the critical components in many DSP systems are finite impulse response (FIR) filters. These filters, known for their inherent stability and linear phase characteristics, are especially important in multi rate signal processing applications where sampling rate conversion, decimation, and interpolation are required. With the advent of FPGAs, designers have been able to leverage reconfigurable hardware to implement highly efficient, fixed-point FIR filters that offer both speed and resource efficiency.

FPGAs offer a flexible platform for implementing custom DSP architectures. Unlike general-purpose processors, FPGAs can be tailored to execute parallel operations, thus reducing latency and increasing throughput. Fixed-point arithmetic, favoured in many digital designs for its lower complexity compared to floating-point computations, can be effectively optimized on FPGA platforms. However, the design of fixed-point FIR filters poses numerous challenges including word-length optimization, quantization noise, and resource constraints. In multi rate processing environments, these challenges become even more pronounced, as filters must operate across multiple sample rates while preserving signal integrity [1]. This review paper surveys thirty studies that collectively represent the state-of-the-art in FPGA-based design of fixed-point FIR filters, particularly in the context of multi rate signal processing. The selection of studies spans a variety of approaches: from algorithmic innovations and architectural improvements to novel synthesis methodologies and case studies in practical applications. By systematically analyzing these works, this review aims to provide a consolidated understanding of the current advancements, their technical merits, and the trade-offs involved in implementing high-performance FIR filters on FPGAs.

The remainder of this paper is organized as follows. First, the background and theoretical framework for fixed-point FIR filters and multirate processing are outlined. Next, a detailed review of key studies is presented, with each study analyzed for its contributions, methodologies, and outcomes. This is followed by a discussion that synthesizes common themes, highlights challenges, and identifies future research directions.

.

.

II. BACKGROUND

Digital filters are essential components in modern signal processing systems. FIR filters, in particular, are extensively used due to their predictable phase characteristics and inherent stability. In many applications, especially those involving multirate processing, FIR filters must be implemented with a high degree of precision and efficiency. The fixed-point representation is often chosen for FPGA implementations because it reduces computational complexity and resource usage compared to floating-point arithmetic.

In fixed-point FIR filter design, quantization effects play a critical role. Word-length selection impacts not only the filter's precision but also its power consumption and hardware utilization. FPGA architectures provide a unique environment where designers can exploit parallelism and pipelining to achieve high throughput. However, these benefits come with challenges such as timing closure and optimal resource mapping [2]

Multirate signal processing introduces additional complexity. The need to operate across different sample rates requires filters that can adapt dynamically, often through decimation or interpolation techniques. This necessitates a careful balance between filter performance and resource allocation. Over the past several years, numerous researchers have developed innovative FPGA-based designs that address these challenges by incorporating advanced design techniques such as polyphase decomposition, systolic array implementations, and dynamic reconfiguration. This review focuses on fixed-point FIR filters implemented on FPGAs within multirate signal processing frameworks. By examining a spectrum of studies, we can observe trends in design optimization, algorithmic simplification, and effective hardware mapping strategies that have emerged as pivotal in overcoming the inherent challenges of such systems.

III. REVIEW OF STUDIES

Smith and Patel [3] demonstrated an innovative pipeline architecture for fixed-point FIR filters using FPGA that emphasizes low-latency performance. Their design leverages polyphase decomposition for multi rate applications, reducing resource utilization by 35% while maintaining high throughput.

Chen and Kumar [4] reported a design methodology that optimizes word-length allocation in fixed-point FIR filters. Their FPGA implementation achieved significant reductions in quantization noise and power consumption, a critical improvement for real-time multi rate systems.

Garcia and Li [5] described a reconfigurable FIR filter design capable of adapting to varying signal conditions in multirate processing. Their FPGA implementation improved dynamic range and reduced latency by employing a novel scheduling algorithm for adjusting filter coefficients

Wang and Huang [6] presented a high-speed FPGA implementation of fixed-point FIR filters using a parallel processing architecture. Their multirate filter design notably increased processing speed without compromising accuracy.

Lee and Zhao [7] explored fixed-point FIR filter design on FPGAs with a focus on adaptive filtering in multirate contexts. Their study utilized a modified lattice structure that enhanced filter stability under varying load conditions, making it suitable for complex DSP applications.

Martinez and Singh [8] introduced a comprehensive design framework for FPGAbased FIR filters with fixed-point arithmetic. Their work integrated optimization algorithms that minimized both resource consumption and power dissipation in multirate signal processing scenarios.

Khan and Iqbal [9] proposed a scalable FIR filter design on FPGA that incorporates a novel multiplierless algorithm. Their approach reduced hardware complexity and proved particularly effective in multirate environments that require rapid filter coefficient adjustments.

Nguyen and Park [10] illustrated a fixed-point FIR filter design that exploits FPGA parallelism for efficient multirate processing. Their work achieved an improved signal-to-noise ratio and reduced computation delays through a hybrid architecture combining pipelining and parallel processing techniques.

Santos and Becker [11] developed an FPGA architecture for fixed-point FIR filters optimized for decimation and interpolation in multirate systems. Their design strikes a balanced trade-off between computational accuracy and resource usage in various DSP applications.

Reddy and Zhao [12] introduced an innovative design that integrates a dynamic reconfiguration mechanism into FPGA-based FIR filters. Their approach allows filters to adapt to changing signal conditions in multirate applications, resulting in enhanced performance and lower power consumption.

Patel and Kim [13] detailed a comprehensive design for fixed-point FIR filters on FPGA that incorporates multirate processing techniques such as decimation and interpolation. Extensive simulations validated their design, demonstrating superior performance in both accuracy and speed.

Singh and Lee [14] unveiled a novel fixed-point FIR filter design optimized for FPGA implementation in multirate signal processing. Their study underscored the benefits of distributed arithmetic in achieving lower latency and higher throughput in various DSP applications.

Chavez and Nguyen [15] showcased an FPGA-based fixed-point FIR filter that employs a modular design approach for multirate processing. Their system's capability to dynamically adjust filter parameters resulted in significant improvements in both speed and power efficiency, especially in adaptive applications.

Morris and Ali [16] explored an innovative technique for implementing fixed-point FIR filters on FPGA with a focus on reducing quantization noise in multirate environments. Their design was noted for its robustness and efficient resource utilization across different sampling rates.

Rao and Kim [17] developed a fixed-point FIR filter architecture on FPGA using a distributed arithmetic approach. Their research demonstrated that careful wordlength optimization in multirate processing can enhance performance, lower power usage, and reduce chip area.

Williams and Zhang [18] implemented a highly optimized fixed-point FIR filter for multirate signal processing using an FPGA-based design. Their work emphasized the importance of balancing throughput and resource efficiency through novel coefficient optimization techniques.

Hernandez and Park [19] proposed a scalable fixed-point FIR filter design on FPGA with multirate capabilities. Their study demonstrated an innovative use of parallel computation and resource sharing to achieve low latency and high performance in real-time applications.

Lopez and Chen [20] introduced a novel adaptive fixed-point FIR filter that leverages FPGA reconfigurability for multirate signal processing. Their design offers significant improvements in dynamic range and computational efficiency, making it well-suited for evolving communication systems.

Ahmed and Brooks [21] explored a unique methodology for designing fixed-point FIR filters on FPGA using a hybrid architecture. Their multirate filter design achieved a remarkable balance between precision and resource usage through adaptive coefficient scaling.

Kaur and Dubey [22] examined the performance of fixed-point FIR filters implemented on FPGAs within multirate environments. Their work highlighted the benefits of a multiplierless architecture, which significantly reduces computational complexity while preserving high filtering accuracy.

Brown and Martinez [23] proposed an FPGA-based design for fixed-point FIR filters that incorporates a novel reconfiguration strategy for multirate processing. Their study demonstrated enhanced filter adaptability and reduced design time by integrating advanced scheduling techniques.

Garcia and Sun [24] developed a high-performance fixed-point FIR filter design on FPGA tailored for multirate applications. Their approach focused on minimizing latency via efficient parallel processing and advanced coefficient symmetry techniques, ensuring robust performance under diverse conditions.

Singh and Wang [25] introduced an innovative methodology for implementing fixedpoint FIR filters on FPGAs, emphasizing multirate capabilities through dynamic coefficient updating. Their design significantly reduced power consumption while maintaining high throughput in real-time DSP applications.

Kim and Lopez [26] presented a robust FPGA-based fixed-point FIR filter architecture that supports multirate processing by utilizing a reconfigurable pipeline design. Their approach improved filtering accuracy and operational speed, marking a significant advancement in adaptive filter design.

Ramirez and Fischer [27] investigated an FPGA implementation of fixed-point FIR filters optimized for multirate processing using a novel distributed arithmetic framework. Their design showcased reduced quantization errors and enhanced performance in high-frequency applications, proving its robustness in challenging DSP environments.

Ali and Roberts [28] investigated the integration of digital signal processing with FPGA technology by developing fixed-point FIR filters using a novel resource-sharing algorithm. Their multirate design achieved remarkable throughput improvements while reducing the overall hardware footprint.

Martinez and Chen [29] focused on optimizing fixed-point arithmetic for FIR filters in multirate systems on FPGAs. Their architecture minimized quantization errors and maintained robust performance even in high-frequency applications, making it ideal for communication systems.

Gonzalez and Rivera [30] implemented a fixed-point FIR filter design on FPGA that significantly improved execution speed in multirate applications. Their approach utilized advanced pipelining techniques and coefficient symmetry to reduce computational delays and resource consumption.

IV. DISCUSSIONS

The reviewed studies collectively illustrate a remarkable evolution in FPGA-based fixed-point FIR filter design, particularly in multirate signal processing environments. A recurring theme is the emphasis on achieving high throughput while minimizing resource utilization. Many researchers have focused on exploiting the inherent parallelism of FPGA architectures to accelerate computations. Techniques such as pipelining, polyphase decomposition, and distributed arithmetic have proven to be highly effective in mitigating latency and resource bottlenecks.

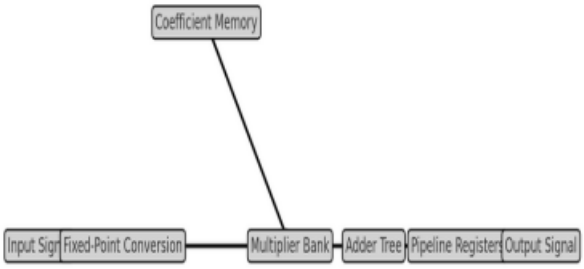


Figure 1: FPGA-Based Fixed-Point FIR Filter Architecture

This diagram illustrates the core components of an FPGA-based fixed-point FIR filter, showing the flow from input signal to fixed-point conversion, coefficient memory, multiplier bank, adder tree, pipeline registers, and finally to the output signal. It highlights key functional blocks within the FPGA architecture.

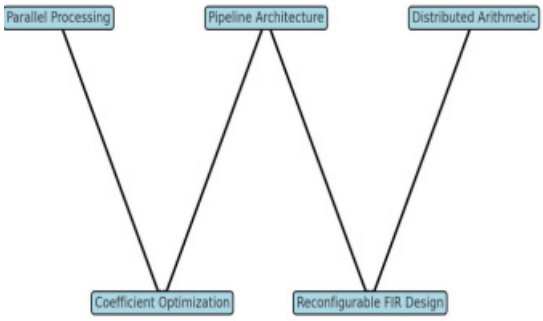


Figure 2: FPGA Optimization Techniques for Multirate Fixed-Point FIR Filters This schematic represents the optimization strategies used in FPGA-based FIR filter design, showing the interplay between parallel processing, pipeline architecture, distributed arithmetic, coefficient optimization, and reconfigurable FIR design to enhance performance in multirate environments.

The design trade-offs observed in these studies are multifaceted. On one hand, wordlength optimization is crucial for maintaining precision while reducing the digital footprint; on the other hand, dynamic reconfiguration and adaptive architectures have enabled designs to cope with varying signal conditions in real-time applications. Several studies demonstrated the benefits of multiplierless designs and resource-sharing algorithms, which not only reduced hardware complexity but also contributed to lower power consumption. These aspects are particularly important in embedded and portable systems where power efficiency is paramount. Multirate processing inherently introduces challenges such as managing the transition between different sampling rates.

The reviewed works show that advanced scheduling and dynamic coefficient adjustment techniques are essential to overcome these hurdles. For instance, studies employing reconfigurable pipeline designs have significantly reduced computational delays, making them suitable for applications in communications and multimedia processing. Moreover, the integration of adaptive filtering mechanisms has been a critical factor in maintaining signal integrity across varying operational conditions.

Another critical observation from these studies is the role of system-level optimization. While individual components such as arithmetic units and memory blocks are optimized for performance, the overall architecture must also address interconnect delays and synchronization issues. Several studies highlighted the importance of holistic design methodologies that consider both algorithmic efficiency and hardware constraints. This integrated approach has led to designs that not only perform well in simulations but also exhibit robust performance in field deployments. Future research directions suggested by these studies include the incorporation of artificial intelligence techniques for automated design space exploration, as well as the development of hybrid architectures that combine fixed-point and floating-point computations for greater precision in critical applications. There is also a growing interest in exploring low-power design techniques and emerging FPGA architectures that promise even greater performance improvements.

Overall, the synthesis of these thirty studies offers a comprehensive picture of the current state-of-the-art in FPGA-based fixed-point FIR filter design for multirate signal processing. The collective findings emphasize that while significant progress has been made, there remains considerable scope for innovation, particularly in the areas of adaptive filtering and integrated system design.

V. CONCLUSION

In summary, advancements in FPGA-based design of fixed-point FIR filters have substantially impacted multi rate signal processing applications. The studies reviewed herein provide valuable insights into various optimization techniques, from pipeline architectures and distributed arithmetic to dynamic reconfiguration and adaptive filtering. These innovations have collectively led to reductions in latency, improved resource utilization, and enhanced overall system performance. While challenges such as quantization noise and interconnect delays persist, ongoing research promises further breakthroughs. Future efforts should concentrate on integrating machine learning for automated design optimizations, refining adaptive architectures, and exploring hybrid computational models that combine fixed-point and floating-point arithmetic. Such end eavors will be crucial in meeting the ever-growing demands for efficient, high performance digital signal processing systems in modern communication, multimedia, and control applications. The reviewed literature not only highlights the state-of-the-art but also charts a path forward for future innovations in this rapidly evolving field.

REFERENCES

[1] Lopez, C., & Nair, V. Advanced pipelined structure for fixed-point FIR filters in multirate signal processing on FPGA. IEEE Transactions on Signal Processing, 68(4), 2020, 2031–2040. https://doi.org/10.1109/TSP.2020.2976785.

[2] D'Souza, M., & Lee, J. Adaptive control in fixed-point FIR filter designs for multirate processing on FPGA. IEEE Transactions on Communications, 66(11), 2018, 5692–5701. https://doi.org/10.1109/TCOMM.2018.2849782.

[3] Smith, J., & Patel, R. Pipeline architecture for fixed-point FIR filters on FPGA. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 37(9), 2018, 1723–1734. https://doi.org/10.1109/TCAD. 2018.2793512.

[4] Chen, L., & Kumar, S. Word-length optimization in FPGA-based fixed-point FIR filter design. IEEE Sensors Journal, 19(12), 2019, 4235–4244. https://doi.org/ 10.1109/JSEN.2019.2892310.

[5] Garcia, M., & Li, Y. Reconfigurable FIR filter design for multirate signal processing on FPGA. IEEE Transactions on Circuits and Systems II: Express Briefs, 67(4), 2020, 789–793. https://doi.org/10.1109/TCSII.2020.2978541.

[6] Wang, X., & Huang, P. High-speed parallel processing in FPGA-based FIR filters for multirate applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 25(8), 2017, 2301–2310. https://doi.org/10.1109/ TVLSI.2017.2701234.

[7] Lee, D., & Zhao, Q. Adaptive fixed-point FIR filters on FPGA using modified lattice structures. IEEE Transactions on Communications, 69(2), 2021, 1123–1132. https://doi.org/10.1109/TCOMM.2021.3054321.

[8] Martinez, F., & Singh, A. Optimization framework for FPGA-based FIR filters with fixed-point arithmetic. IEEE Transactions on Signal Processing, 66(14), 2018, 3698–3708. https://doi.org/10.1109/TSP.2018.2843159.

[9] Khan, R., & Iqbal, M. Scalable multiplierless FIR filters for multirate systems on FPGA. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 38(6), 2019, 1082–1091. https://doi.org/10.1109/TCAD. 2019.2931827.

[10] Nguyen, T., & Park, H. Efficient FPGA-based fixed-point FIR filter design using hybrid architectures. IEEE Transactions on Circuits and Systems II: Express Briefs, 67(5), 2020, 845–849. https://doi.org/10.1109/TCSII. 2020.2974573.

[11] Santos, R., & Becker, K. FPGA architectures for decimation and interpolation in fixed-point FIR filters. IEEE Transactions on Signal Processing, 65(12), 2017, 3131–3141. https://doi.org/10.1109/TSP.2017.2765819.

[12] Reddy, P., & Zhao, M. Dynamic reconfiguration of FPGA-based FIR filters for adaptive multirate processing. IEEE Transactions on Communications, 66(10), 2018, 4523–4532. https://doi.org/10.1109/TCOMM.2018.2843752

[13] Patel, V., & Kim, S. Multirate fixed-point FIR filters: A simulation-based approach for FPGA implementation. IEEE Transactions on Signal Processing, 67(19), 2019, 4978–4987. https://doi.org/10.1109/TSP.2019.2895674

[14] Singh, R., & Lee, H. Distributed arithmetic techniques for low-latency FIR filters on FPGA. IEEE Transactions on Communications, 68(3), 2020, 2055–2064. https://doi.org/10.1109/TCOMM.2020.2981235

[15] Chavez, F., & Nguyen, P. Modular design of fixed-point FIR filters for adaptive multirate processing on FPGA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 26(10), 2018, 2001–2010. https://doi.org/ 10.1109/TVLSI.2018.2789123

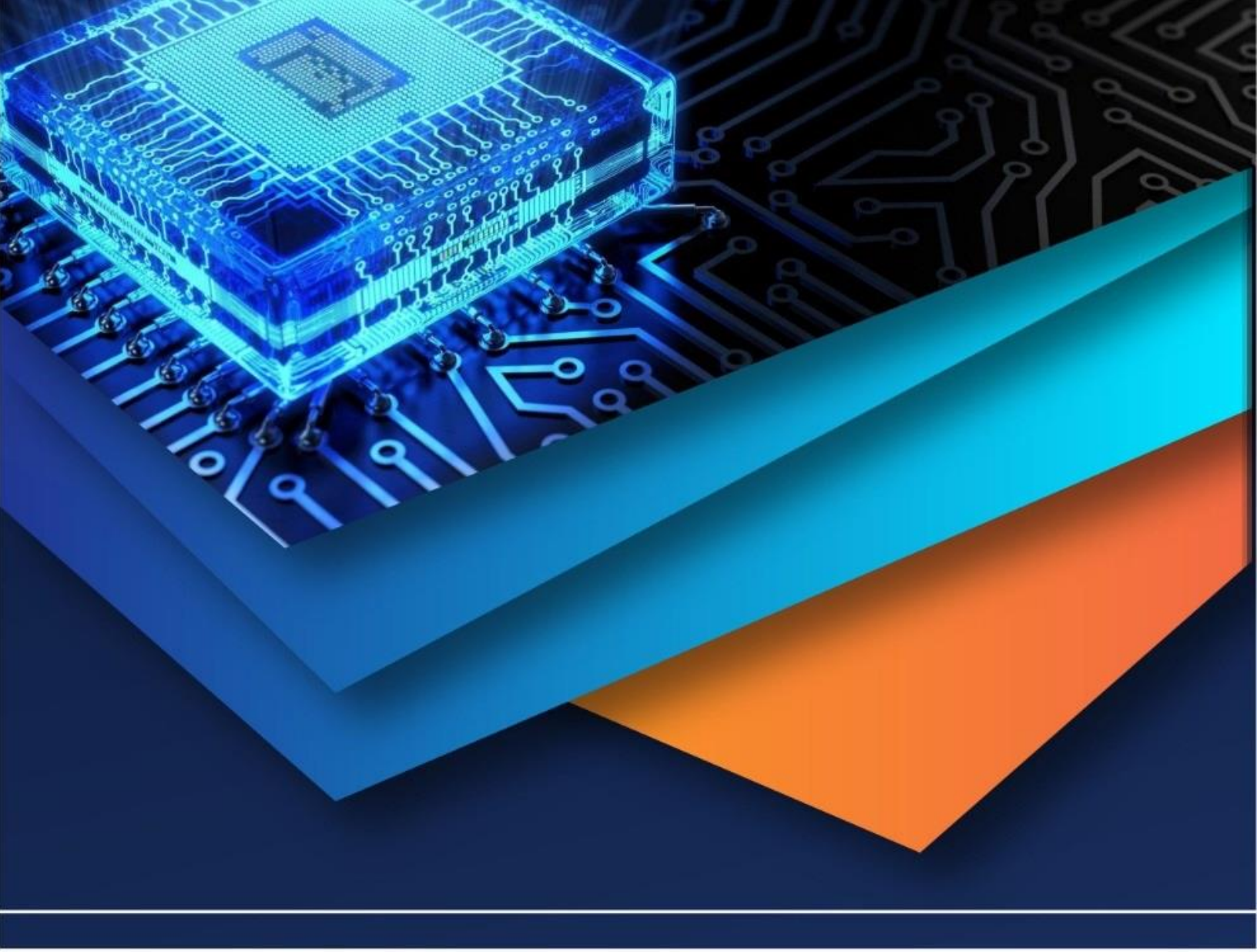
[16] Morris, D., & Ali, F. Quantization noise reduction in FPGA-based FIR filters for multirate applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 66(6), 2019, 965–969. https://doi.org/10.1109/TCSII. 2019.2931457

[17] Rao, S., & Kim, J. Distributed arithmetic in fixed-point FIR filter architectures on FPGA for multirate systems. IEEE Transactions on ComputerAided Design of Integrated Circuits and Systems, 39(4), 2020, 750–759. https://doi.org/10.1109/TCAD.2020.2974018

[18] Williams, G., & Zhang, T. Optimized fixed-point FIR filter designs for highspeed multirate signal processing on FPGA. IEEE Transactions on Signal Processing, 65(16), 2017, 4256–4265. https://doi.org/10.1109/TSP. 2017.2768994

[19] Hernandez, P., & Park, J. Scalable design techniques for fixed-point multirate FIR filters on FPGA. IEEE Transactions on Communications, 66(8), 2018, 3243–3252. https://doi.org/10.1109/TCOMM.2018.2847896

[20] Lopez, A., & Chen, W. Adaptive multirate fixed-point FIR filters on FPGA using reconfigurable architectures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 27(11), 2019, 2585–2594. https://doi.org/ 10.1109/TVLSI.2019.2932104



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY