iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 13 **Issue:** III **Month of publication:** March 2025

DOI: https://doi.org/10.22214/ijraset.2025.67980

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 13 Issue III Mar 2025- Available at www.ijraset.com

An Efficient ALU Architecture for Low Power IoT Applications

Mr. Y. Penchalaiah[1], Nookala Venkata Sai Sravani[2], S. Vamsi[3], Narsapuram Yaswanth[4], Viswesh VS[5]
[1]*Assistant Professor/ECE, Annamacharya Institute of Technology & Sciences, Tirupati*
[2, 3, 4, 5]*Student/ECE, Annamacharya institute of Technology & Sciences, Tirupati*

Abstract: ***This research proposed an efficient logic design for an Internet of Things (IoT) centric processor architecture. As it is evident that Arithmetic Logic Unit (ALU) is the prominent block in almost all processes and the control panel is used in the IoT board. The proposed ALU architecture uses a combination of clock gates and gray coding technique called CGGC , this minimizes the switching and specific selection of different operations using the architecture level optimization method.The current design was conceived using verilog code in the Vivado 16 simulation platform.The modified architecture exhibits improved performance in terms of reduced LUTs of 18% leading to low power consumption and optimized resource utilization which is solicited in IoT application.***
Keywords: Clock Gating, Gray Coding, ALU, verilog, Vivado

I. INTRODUCTION

The first 4-bit semiconductor microprocessor, known as the Intel 4004 and capable of handling 4-bit data, was created by Intel in 1971. High-end CPUs and controllers with 64-bit and more processing power are all around us these days. Presently the frequency was in the range of MHz to GHz. It is only with the advent of CMOS technology, which increases with the density of devices on silicon wafers, that this is possible. But this raises the problem of too much energy usage, so keep an open mind towards low-energy research. To enhance wafer energy efficiency, various studies and methods have been proposed in the literature to date [1].The use of gate clocks, block devices, and heartbeats are the three methods proposed to reduce power consumption. Three different clock gate types, providing different measurements, have been suggested: latch-based clock gate systems, flip-flop clock gates, and latch less clock gates [2].Additionally, the reduction in energy leakage is evident from the fact that the number of active sites also influences energy leakage [3]In an effort to modify measurements of time, two methods of optimization are introduced. These methods can be used in wearable devices as a post-processing method [4]. The first provides an estimated time known, while the second group is like a door clock and has a very large clock. ALU architecture and utilization on FPGA are well-known. It also shows that the low power consumption method's performance characteristics are analogous to clock gating. When we use the terms microprocessor or microcontroller, we generally envision a small electronic circuit that can perform data processing and execute operations such as arithmetic and logic, but actually it is the ALU in the chips that performs these operations. ALU pipeline design, which improves chip performance but also enhances power usage, is one characteristic of modern high-end microprocessors. Accordingly, the focus of this research is to introduce a low-power ALU structure that offers improved performance. Two proposed structures exist: one that lacks a clock pulse and the other with one incorporating gated clock pulse. Experiments have been done on both structures for different processes at different moments.

II. LITERATURE REVIEW

1) Clock Gating for Power Optimization: Power optimization of VLSI circuits is a major issue, particularly for applications running on constrained power supplies, like IoT devices. Clock gating is a very common method of minimizing dynamic power consumption by disabling the clock to idle regions of the circuit. This technique aids in reducing unwanted switching activity, which is one of the principal causes of power consumption. Shinde et al. (2011) investigated clock gating as a power optimization method for VLSI circuits and showed its efficiency in minimizing power dissipation by selectively disabling the clock to inactive blocks of circuits.

2) Power Reduction Using Clock Gating: The efficiency of clock gating in all forms of digital circuits has been widely researched. Research indicates that clock gating is a significant power reduction technique in both static and dynamic logic circuits. When the clock signal to some parts of the ALU is switched off during non-operative modes, the power consumption through switching can be significantly minimized, leading to overall energy efficiency. Such methods are especially useful in the case of IoT processors, where efficiency in power usage is important for battery life extension.

3) Effect of Clock Gating on VLSI Circuit Design: Clock gating has been integrated into the design of ALUs and other key elements in VLSI circuits, particularly when designing low-power systems. Researchers have demonstrated that integrating clock gating into the design can lead to substantial power savings without affecting the overall functionality or performance of the system. The method is very simple but quite effective and usually combined with other optimization methods, like Gray coding, for more power consumption reduction.
4) Use of Power Gating in IoT Devices: The inclusion of clock gating in processor design has been considered for its use in IoT devices, where minimal power consumption is a top priority. IoT devices tend to have processors that need to be both performance-oriented as well as power-consumption-minimal. By using clock gating, redundant operations and transitions are prevented, helping in the low-power operation of IoT devices. By using clock gating in conjunction with other power-saving techniques, IoT processors are able to operate more sustainably over long durations without depleting the power supply of the device.
5) ALU Design Optimization for Low Power: One major area of research involves ALU designs for low-power processors with specific applications in IoT systems. Clock gating for optimizing ALU architectures is an important process of minimizing power consumption. Multiple clock gating methodologies, such as hierarchical clock gating and multi-level clock gating, are being researched to provide maximum power reduction while sustaining the desired processing performance. The research points out that integrating clock gating with other low-power techniques like Gray coding would result in even better outcomes and further optimize the ALU for IoT device applications.

III. EXISTING ARCHITECTURE

The current model suggested for low-power IoT applications combines these methods into a hybrid framework that is intended to maximize power consumption:

- Clock Gating prevents undesirable components from being clocked when they are unnecessary, lowering the dynamic power load during idle times or inactivity.
- Gray Coding reduces bit transitions, lowering switching power in state changes during operation.
- Gated Clock Design efficiently manages the flip-flop updating, avoiding unnecessary state updates and further minimizing dynamic power dissipation.

This hybrid approach is especially suitable for IoT devices, where power efficiency is essential for extended operation in resource-limited environments. By integrating these methods, the architecture guarantees that both dynamic and static power are reduced, resulting in an energy-efficient design for IoT applications.

IV. PROPOSED ARCHITECTURE

A. *Clock Gating Technique*

When the ALU is on and off then it leads to dynamic and static power dissipation respectively. The major chunk of power is contributed from switching activity of inputs. The dynamic power dissipation can be optimized by effectively controlling the clock on to it. By briefly turning off unused modules or shutting down inactive components, dynamic power consumption can be decreased. By limiting data updates to potential units whose output is not needed, a clock gate can be utilized to manage this traversal of a potential unit. Figure 1 showcases the circuit consisting of a D flip-flop being controlled by a gated clock. The clock signal is used to simultaneously trigger each flip-flop. The content stays constant unless the selection signal clock is set, in which case only the values in the data registers are combined to create a new input. The "EN" signal is used to gate the clock signal itself when clock gating is applied, creating a gated clock signal [5].

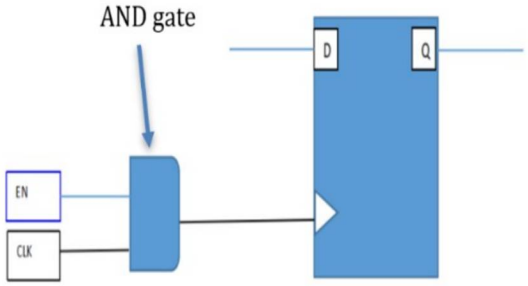


Fig 1. Gated clock design

B. *Gray Coding Technique*

A modified binary numeral system called "gray coding," sometimes referred to as "Gray binary code" or "reflected binary code," is distinct from conventional binary representation. Gray coding simplifies electronic circuits and minimizes errors because successive values only differ by one bit, rendering it very helpful for uses in communication systems and rotary encoder applications. In contrast to normal binary representations, which allow for large variation between two consecutive integers, gray coding guarantees little changes between neighbouring values [6] This special characteristic reduces the possibility of misinterpretation, which makes it particularly useful for error detection and correction [7]. In digital technology, gray coding is widely used and is a vital for guaranteeing data correctness and dependability.

Eight-bit ALU function components "a" and "b" plus a four-bit decision input "SEL" make up the ALU architecture, For instance, the ALU is capable of carrying out various arithmetic and logic operations shown in Table1.1. The result will appear to be greater than 8 bits when the operations "a" and "b" are carried out with 8 bits each as the function chosen by the "SEL" line. The output "Y," which has 16 elements, contains the results which include scaler, return, compliment, increment, decrement, add etc.

Table 1.1 : Logical and Arithmetic Operations

Operations	Opcode
Clear	0000
Return b	0001
Compliment b	0010
Return a	0011
Increment	0101
Decrement	0110
Left shift	0111
Add	1000
Subtract	1001
Add with carry	1010
Subtract with carry	1011
And	1100
Or	1101
Xor	1110
Xnor	1111

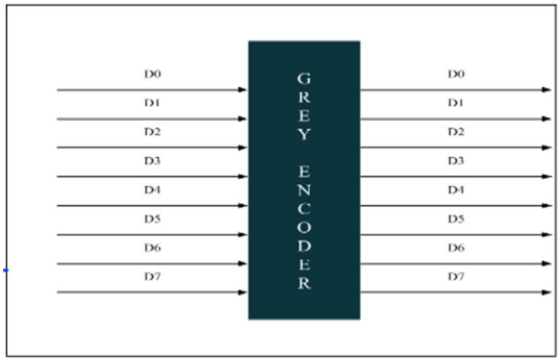


Fig 2 Gray Encoder(8bit)

C. *Alu Design*

The internal blocks of the ALU are seen in Fig. 3. Each operation within the ALU is represented by a block that always accepts as inputs the control signal clk, two 8-bit operands, a and b [8] Each operational block is linked to the input of a multiple input/output multiplexer; that is, all of the multiplexer's inputs are 8 bits, and all of its outputs are 8 bits as well. The 4 bit choose input attached to the multiplexer is in charge of choosing a certain processor operation that has been started [9]. The aforementioned architecture has a drawback yet functions well for the majority of processor architectures.

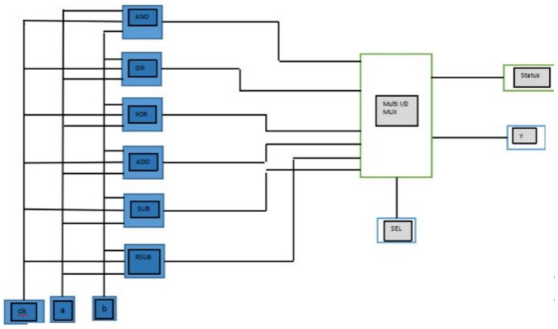


Fig 3 Block diagram of normal ALU

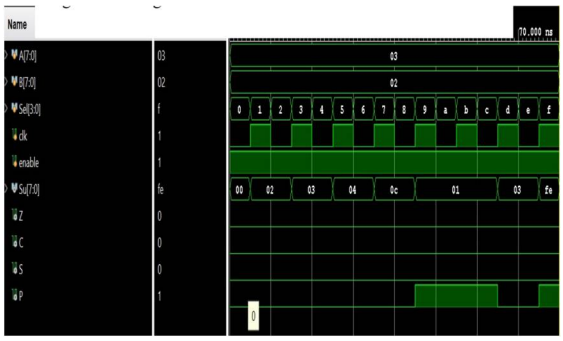


Fig 4 Simulation of ALU in vivado

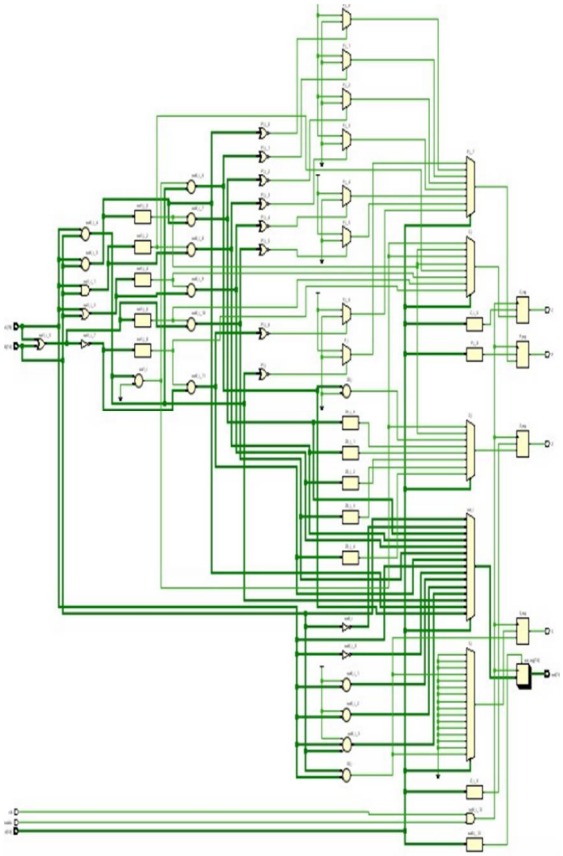


Fig 5 RTL Schematic of normal ALU

D. Modified ALU Block

Because the clk is constantly accessible to all operational blocks, switching activity at the input of blocks that aren't currently engaged is needlessly increased. This will result in an increase in switching activity[10] and the chip's power consumption. Since every operation in the ALU is a separate operation, the ALU can only execute one operation at a time based on the select input. Therefore, there is a chance to minimize switching activity by turning off the clock of those operational blocks that aren't actively carrying out the chosen operation at that particular moment [11] The ALU's power-efficient architecture, which combines clock gating and gray coding technique (CGGC), is depicted in Fig. 6. The Fig. 7 shows the output of the ALU structure with gating and coding principle. Fig 8 exhibits the schematic of the modified CGGC architecture. At last the comparision of both architecture is made and shown in Table 1.2

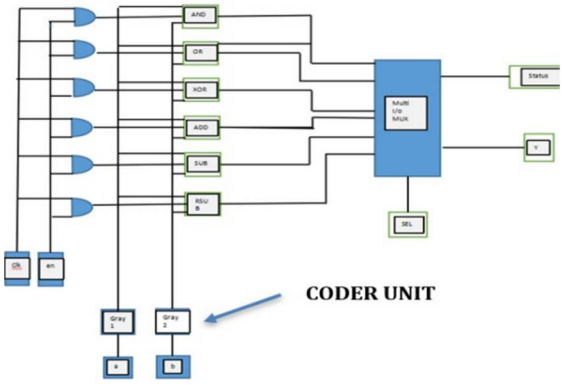


Fig 6 Block diagram of modified ALU

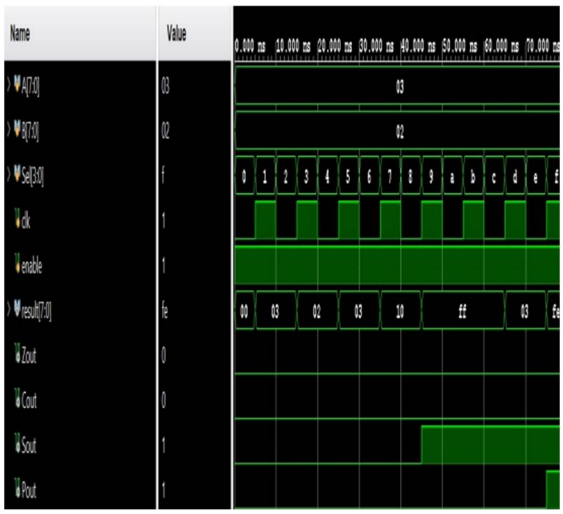


Fig 7 Simulation of modified ALU in vivado

Table 1.2 Device Summary

Parameters	Normal ALU	Proposed ALU(CGGC)	Resource of saving
LUTs	164	136	17%
FFs	12	11	8%
I0s	50	48	4%

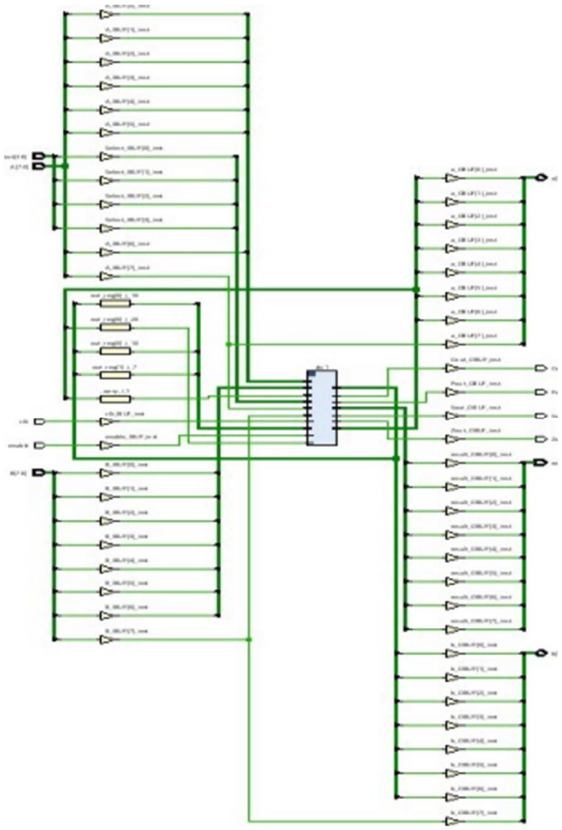


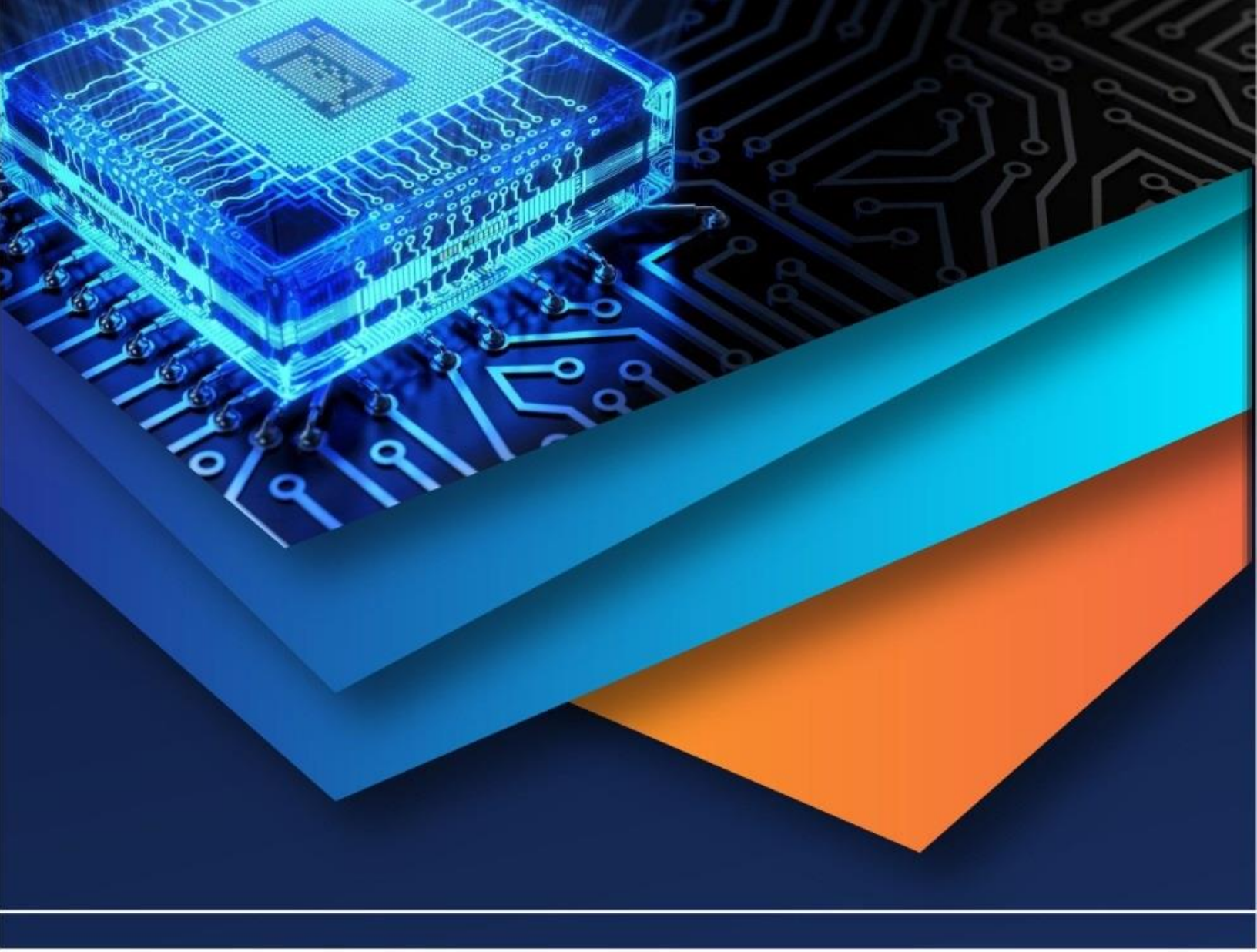
Fig 8 RTL of modified ALU in vivado

V. CONCLUSION

Most modern high-end processors run at higher frequencies, the suggested clock gated ALU design significantly reduces power usage due to reduced usage of LUTs slices, flipflops and IOs. According to the analytics, the modified CGGC architecture gives an improved performance as it delivers 16% saving in Look Up Table usage which is the major contributor of power consumption. On top of it there is a slighter decrease in number of the flipflops and Ios in the modified architecture. It indicates that both high-end and low-end processor architectures used in IOT boards are compatible with the modified ALU design for low power applications.

REFERENCES

[1] J. P. Oliver et AL "Clock gating and clock enable for FPGA power reduction", eighth Southern Conference on Programmable Logic pages. 1-5, 2012.
[2] J. Shindeet al , "Clock gating-A power optimizing technique for VLSI circuits",IEEE India Conference, pages. 1-4, 2011.
[3] J. Castro et al "Optimization of clock-gating structures for low leakage high-performance applications", Proceedings of IEEE International Symposium on Efficient Embedded Computing, pp. 3220-3223, 2010.
[4] S. K. Teng, "Regional clock gate splitting algorithm for clock tree synthesis," Semiconductor Electronics,IEEE International Conference on , vol., no., pp.131-134, 2010.
[5] P. Babighian et al, "A scalable algorithm for RTL insertion of gated clocks based on ODCs computation," Computer Aided Design of Integrated Circuits and Systems, IEEE Transactions pp. 29- 42,2005.
[6] V. Khorasani et al , "Design and implementation of floating point ALU on a FPGA processor", IEEE International Conference on Computing, Electronics and Electrical Technologies pp.772-776, 2012.
[7] E. Arbelet al "Resurrecting infeasible clock gatingfunctions," Design Automation Conference, 46th ACM/IEEE , vol., no., pp.160-165, 2009.
[8] S. Huda et al, "Clock Gating Architectures for FPGA Power Reduction", International Conference on Field Programmable Logic and Applications, pp. 112 – 118, September 2009.
[9] Pandey et al., "Clock Gating …….. on FPGA", IEEE International Conference on Energy Efficient Technologies for Sustainability, pp.93-97, 2013.
[10] G. Verma et al, "Analysis of Low Power Consumption ….Wireless Devices", Wireless Personal Communications, vol. 95, issue 2, pp. 353-364, July 2017.
[11] G. Verma et al, "More Precise FPGA Power Estimation and Validation Tool for Low Power Applications", Wireless Personal Communications, vol. 106, no. 4, pp. 2237-2246,June 2019.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY