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An Efficient and Advanced Transition Fix Strategies for Multi-Voltage Channel-Based SoCs with Power and Timing Optimization

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Abstract: ***As the semiconductor industry advances toward lower technology nodes, the adoption of multi-voltage designs within channel-based SoC architecture presents both significant opportunities and complex challenges, particularly in the context of stringent power optimization requirements. These designs inherently introduce complex issues related to voltage domain transitions, which are critical to managing signal integrity and timing closure. Transition phenomena between voltage domains represent a major concern, directly impacting the chip's power, performance, and area (PPA) metrics. This paper provides an in-depth analysis of transition mechanisms in multi-voltage channel-based SoC designs, identifying root causes and quantifying their effects on timing and signal integrity. It further proposes robust, practical methodologies and design techniques to mitigate transition-related issues, ensuring these solutions integrate seamlessly without compromising design integrity or chip specifications. By systematically addressing the intricacies of multi-voltage transitions in channel-based SoCs, we deliver comprehensive and efficient strategies validated through real-world implementations.***
Keywords: Transition , Multi-voltage Domian , Channel Based SoC.

I. INTRODUCTION

In the ongoing drive to enhance the performance and energy efficiency of System-on-Chip (SoC) designs, multi-voltage architectures have emerged as a prominent technique for power optimization. By enabling different functional blocks to operate at distinct voltage levels, significant power savings can be achieved without compromising overall system performance. However, the integration of multiple voltage domains introduces complex transition challenges at domain interfaces, which critically impact timing, power integrity, and design reliability. As semiconductor technology advances toward increasingly scaled nodes, these transition issues become more pronounced, presenting substantial challenges for physical design engineers tasked with optimizing power in sophisticated multi-voltage SoCs. The intricate interplay between voltage domain crossings, level shifting, isolation, and synchronization demands careful consideration to maintain design robustness and meet stringent power-performance-area (PPA) targets. This paper provides a comprehensive analysis of transition-related challenges inherent in multi-voltage SoC architecture. It further proposes practical and effective methodologies, supported by real-world case studies, to mitigate transition-induced issues. The presented solutions aim to facilitate reliable timing closure, minimize power overhead, and enhance overall design efficiency, thereby enabling scalable and robust SoC implementations in advanced technology nodes.

II. TRANSITION AND MULTI VOLTAGE DOMAINS

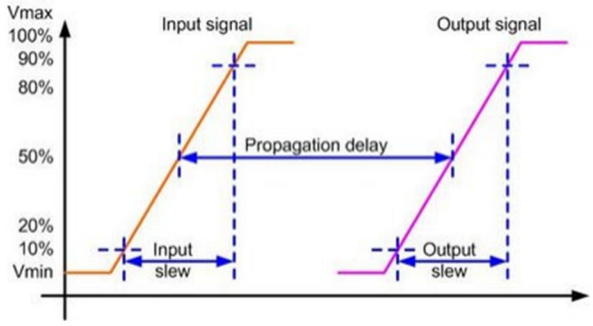
A. Overview of Transition and Slew

In digital electronics, transition or slew refers to the rate at which a signal changes its voltage level from one logic state to another, typically from low to high (rising edge) or high to low (falling edge). This change is not instantaneous; rather, it occurs over a finite period, characterized by the rise time and fall time of the signal. The rise time is defined as the duration it takes for the signal to increase from a specified low voltage level (commonly 10% of the maximum voltage) to a high voltage level (commonly 90% of the maximum voltage). Similarly, the fall time is the duration for the signal to decrease from 90% to 10% of the maximum voltage. The slew rate, often expressed in volts per nanosecond (V/ns), quantifies how quickly this voltage transition occurs.

The importance of transition or slew lies in its direct impact on both timing and signal integrity within digital circuits.

A fast transition, characterized by a steep slope, enables quicker data propagation and improved timing margins. However, excessively fast transitions can induce signal integrity issues such as ringing, crosstalk, and electromagnetic interference (EMI) due to abrupt changes in current and voltage, which excite parasitic inductances and capacitances in the circuit.

Conversely, slow transitions reduce these high-frequency effects but can lead to timing violations, including setup and hold time failures in sequential elements, because the signal takes longer to reach stable logic levels.



Types of Transitions : In digital designs, two critical types of transitions affect timing and performance: clock transitions and data transitions.

Clock transition refers to the slew rate of the clock signal as it propagates through the clock distribution network. Variations in clock rise and fall times impact the clock duty cycle and timing accuracy at sequential element inputs, as characterized in standard cell libraries (.lib). This is especially critical in multi-voltage designs, where differing supply voltages influence transistor switching speeds, necessitating careful control of clock slew to maintain timing integrity.

Data transition denotes the slew on functional (non-clock) signal paths. Inaccurate data slew leads to deviations from characterized cell delays, causing setup and hold violations. Multi-voltage designs complicate data transitions due to level shifters and isolation cells between voltage domains. Proper voltage domain partitioning and slew management are essential to ensure timing correctness and signal integrity.

B. Transition issues in ASIC: Characterization , Causes and Mitigation

In advanced ASIC design flows, each standard cell is rigorously characterized in a Liberty (.lib) timing library, which defines maximum permissible input transition times also known as slew rate limits - for accurate modeling of timing, power, and noise behavior. These maximum input transition constraints represent the upper bound on signal slew for which the cell's delay and power parameters have been precisely characterized through silicon or transistor-level simulations.

If the actual input transition at a cell's pin exceeds this specified maximum slew threshold, the timing and power models provided in the .lib file become invalid. This discrepancy leads to inaccuracies in static timing analysis (STA), as the delay values computed no longer reflect the true cell behavior under the given slew conditions. As a result, the standard cell may exhibit degraded timing performance, failing to meet setup and hold time requirements, which can cascade into functional failures at the system level.

Required Transition	Actual Transition	Transition Slack	Library Constraint
0.9087	1.2472	-0.3385	0.9087
0.3341	0.6726	-0.3385	0.3341
0.3341	0.6726	-0.3385	0.3341
0.3341	0.6698	-0.3357	0.3341
0.3341	0.6686	-0.3345	0.3341
0.3341	0.6680	-0.3339	0.3341
0.3341	0.6675	-0.3334	0.3341
0.3341	0.6668	-0.3327	0.3341
0.3341	0.6666	-0.3325	0.3341
0.3341	0.6647	-0.3306	0.3341
0.3341	0.6646	-0.3305	0.3341
0.7305	1.0607	-0.3302	0.7305
0.3341	0.6639	-0.3298	0.3341
0.3341	0.6632	-0.3291	0.3341

The challenge intensifies in multi-voltage or multi-domain designs, where cells operate under varying supply voltages and load conditions. Different voltage domains inherently affect transistor switching speeds and capacitive loading, increasing the likelihood of slew violations due to mismatched drive strengths or inter-domain signal crossings. This variability necessitates meticulous control and optimization of input slew rates to maintain timing closure and signal integrity.

Therefore, addressing transition violations through design techniques such as buffer insertion, driver upsizing, and careful voltage domain partitioning is critical. These measures ensure that the actual input slew remains within the characterized liberty limits, thereby preserving the validity of timing models and achieving reliable, predictable operation across all voltage domains in the ASIC.

Transition issues in ASIC designs arise due to a combination of electrical, physical, and architectural factors that affect signal slew rates and timing integrity.

C. The Primary Technical Causes Include

1) Excessive Net Length and Routing Complexity: Long interconnects introduce significant parasitic resistance (R) and capacitance (C), increasing the RC delay and thus slowing signal transitions. Routing nets over extended distances especially on lower metal layers with higher resistivity exacerbates this effect, causing signals to slew more slowly than expected.
2) Insufficient Driver Strength: Drivers with inadequate driving capability cannot charge or discharge the load capacitance efficiently, leading to prolonged rise and fall times. This is particularly problematic when weak drivers are tasked with driving large capacitive loads or long nets, resulting in sluggish transitions.
3) High Fanout Loads: A single driver feeding multiple sinks increases the total capacitive load, which can overwhelm the driver's ability to maintain fast transitions. High fanout scenarios cause increased input capacitance and degrade the slew rate at the driver's output pin.
4) Crosstalk and Coupling Noise: When signal nets run in close parallel proximity over significant lengths, capacitive and inductive coupling occurs between aggressor and victim nets. This coupling can induce unwanted noise and delay variations on the victim net, distorting its transition characteristics and potentially causing timing violations.
5) Routing on Lower Metal Layers: Lower metal layers typically have narrower widths and higher sheet resistance compared to upper layers. Signals routed predominantly on these layers experience increased resistive losses, which slow down signal transitions and increase delay.
6) Process, Voltage, and Temperature (PVT) Variations: Variations in manufacturing process parameters, supply voltage fluctuations, and temperature changes affect transistor switching speeds and interconnect resistance, leading to unpredictable slew behavior and potential transition violations.
7) Multi-Voltage Domain Interactions: Signals crossing between different voltage domains often require level shifters and isolation cells, which introduce additional delays and can degrade transition times if not properly sized or inserted.
8) Inadequate Buffering or Repeater Insertion: Failure to insert buffers or repeaters on long nets results in excessive RC loading and slow transitions. Proper buffer placement is essential to restore signal integrity and maintain slew within characterized limits.
9) Congestion and Placement Constraints: Physical design congestion can force suboptimal routing paths and limit driver upsizing opportunities, indirectly causing slower transitions due to increased load and routing detours.
10) Incorrect Library Characterization or Misuse: Using standard cell libraries without accurate slew characterization for the target technology or voltage domain can lead to underestimated transition times and unexpected violations.

D. How to Resolve transition Issues

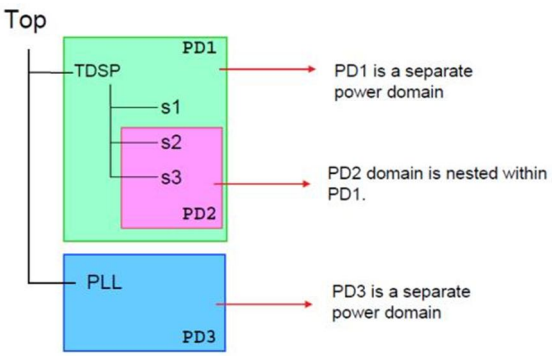
1) Buffer Insertion: Insert repeaters along long interconnects to segment nets, reducing RC delay and restoring slew within characterized limits. Optimal buffer sizing and spacing are essential to balance delay, power, and area overhead.
2) Driver Upsizing: Increase cell drive strength to enhance current drive capability, accelerating signal transitions on high-capacitance or long nets. Placement constraints and power impact must be carefully managed.
3) Metal Layer Promotion: Route critical nets on upper metal layers with lower resistance and capacitance to minimize transition delay and improve slew.
4) Fanout Reduction: Limit driver fanout by inserting buffers or restructuring logic to reduce capacitive loading, thereby maintaining faster slew rates.
5) Crosstalk Mitigation: Increase spacing between aggressor and victim nets, apply shielding techniques, and optimize routing to reduce capacitive coupling and slew degradation.
6) Level Shifter Optimization: In multi-voltage designs, size and place level shifters and isolation cells to minimize additional slew and delay during voltage domain crossings.
7) Physical Optimization: Utilize timing-driven placement and routing to alleviate congestion, enabling effective driver upsizing and buffer insertion.
8) Slew-Controlled Library Cells: Employ standard cells with inherent slew control or characterized for fast transitions to maintain slew within limits.
9) Voltage Domain Partitioning: Strategically partition voltage domains to minimize inter-domain crossings, reducing complexity and slew violations.

Technique	Description	Diagram Concept
Buffer Tree Insertion	Hierarchical buffering to split load	Driver → Buffers → Sinks
Driver Upsizing + Partitioning	Increase driver strength + split fanout	Upsized Driver + Buffers
Wire Length & Layer Promotion	Shorter wires on upper metal layers	M3 long wire → M7 shorter wire
High-Drive/Fast-Slew Cells	Use cells with stronger drive and faster slew	Standard cell → High-drive cell
Logical Restructuring	Duplicate logic or buffer to reduce fanout	Signal → Multiple buffers → Sinks
Slew-Aware Synthesis	Tool-based optimization with slew constraints	Input: fanout/slew → Output: optimized netlist

III. MULTI VOLTAGE DOMAINS BASICS AND CELLS

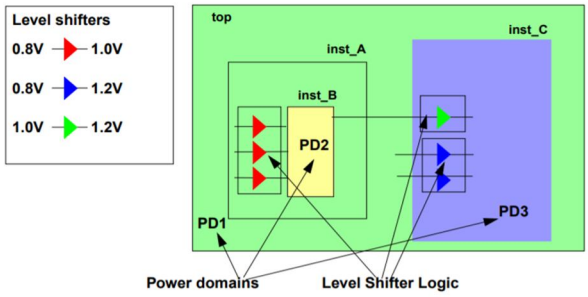
The chip is partitioned into distinct voltage domains, each powered by a separate supply voltage. For example, core logic might operate at a low voltage (e.g., 0.9 V) for power efficiency, while I/O circuits use a higher voltage (e.g., 3.3 V) for signal integrity.

Power Domain Creation by Logical Hierarchy

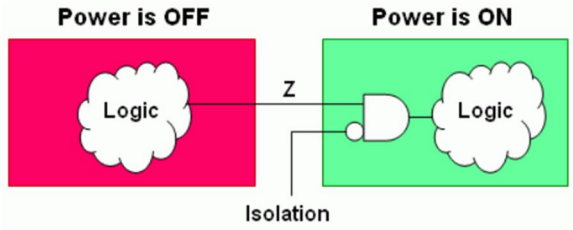


Level shifter cells are specialized standard cells used in integrated circuit designs to safely and reliably transfer digital signals between different voltage domains operating at distinct supply voltages.

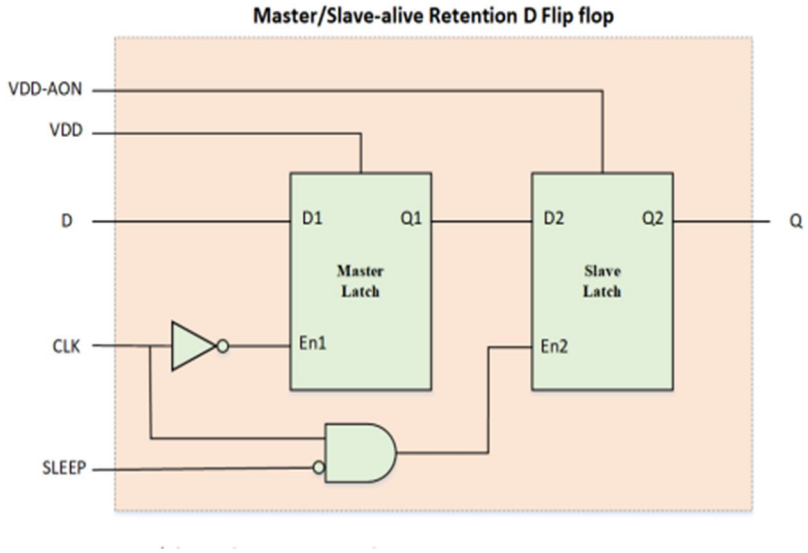
Operating Voltage (OV)	Instances Operating on OV	Libraries characterized for OV	Power Domains for OV
VDD1: 0.8	top, inst_A	lib1 lib2	PD1
VDD2: 1.0	inst_B	lib3	PD2
VDD3: 1.2	inst_C	lib4	PD3



Isolation cells are specialized standard cells used in multi-voltage or power-managed ASIC and SoC designs to maintain signal integrity and prevent erroneous behavior when parts of a design are powered down or operated at different voltage levels.

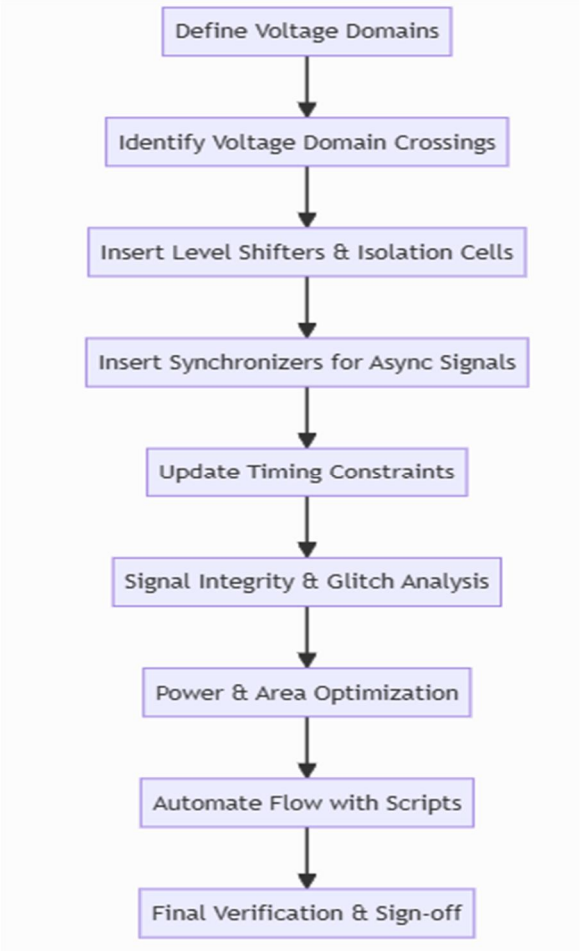


Retention cells are sequential cells that can hold their internal state when the primary power supply is shut down and can restore the state when the power is brought up.



IV. MULTI SUPPLY DESIGN TRANSITION CHALLENEGS

Below is the snippet of the basic flow for transition fixes in a multi-voltage channel Based SoC



This sample script : that focuses on detecting voltage domain crossings, inserting level shifters, and applying timing constraints.

```
# Define voltage domains
set_voltage_domain -name "VDD_1p2" -voltage 1.2
set_voltage_domain -name "VDD_0p9" -voltage 0.9

# Assign voltage domains to design modules or instances
set_instance_voltage_domain -instance "chip/channelA/*" -domain "VDD_1p2"
set_instance_voltage_domain -instance "chip/channelB/*" -domain "VDD_0p9"

# Identify voltage domain crossings (VDC)
report_voltage_domain_crossings -verbose > vdc_report.txt

# Parse VDC report (example: extract crossing nets)
set crossing_nets [split [read_file vdc_report.txt] "\n"]

# Insert level shifters on crossing nets
foreach net $crossing_nets {
    # Assuming level shifter cell is named 'LSHIFT_1p2_to_0p9'
    insert_level_shifter -net $net -cell "LSHIFT_1p2_to_0p9" -side "source"
}

# Insert isolation cells on nets crossing into power-gated domains
insert_isolation_cells -domain "VDD_0p9" -isolation_cell "ISO_CELL"

# Add timing exceptions for voltage domain crossings
foreach net $crossing_nets {
    set_false_path -from [get_ports -of_net $net] -to [get_ports -of_net $net]
    # Add multi-cycle path if applicable
    set_multicycle_path 2 -setup -from [get_ports -of_net $net] -to [get_ports -of_net $net]
}

# Update timing libraries for multi-voltage domains
set_operating_conditions -name "VDD_1p2" -voltage 1.2 -process "typical" -temp 25
set_operating_conditions -name "VDD_0p9" -voltage 0.9 -process "typical" -temp 25

# Run timing analysis with updated constraints
update_timing
```

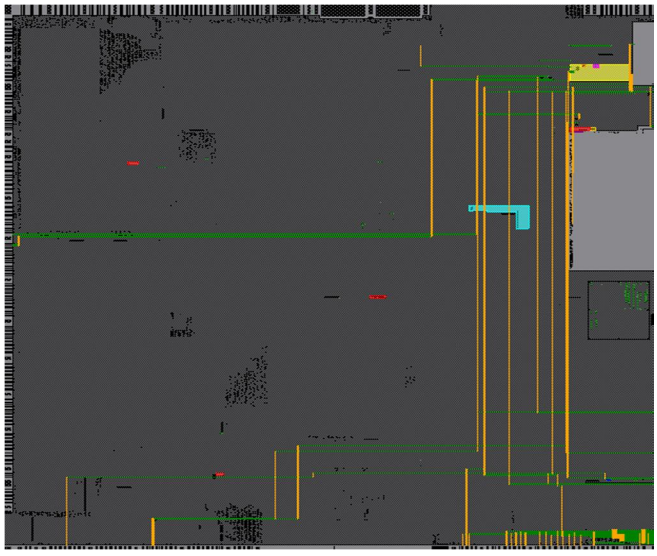
To establish a rigorous theoretical framework for signal transition management in multi-voltage designs, it is essential to integrate both conceptual principles and practical methodologies. This section explores advanced, technology-aware strategies and design techniques implemented during the physical design and verification stages to systematically mitigate transition-related challenges, ensuring timing integrity and robust operation in complex multi-voltage environments.

Let us consider some scenarios based on the Inter power domain Signal Connectivity.

1) Scenario 1: Based on the sink and driver being in same power domain , yet signal passing through another domain.

Voltage Hopping for the Nets highlighted in Green and Orange :

a) The drivers for these nets are situated on the left side, while the sink is positioned on the righ side. Although both reside within the same voltage domain, the routing path traverses a different voltage domain , with approx. length of 1900 um. The drivers were upsized to X24 (max allowed cells) , while the nets were custom routed in M8 and M9 (the highest Metal Layer available).



b) The drivers for these nets are situated on the bottom side (Port) , while the sink is positioned on the Top side. Although both reside within the same voltage domain, the routing path traverses a different voltage domain , with approx. length of 1500 um. The drivers were upsized to X24 (max allowed cells) , while the nets were custom routed in M8 and M9 (the highest Metal Layer available).

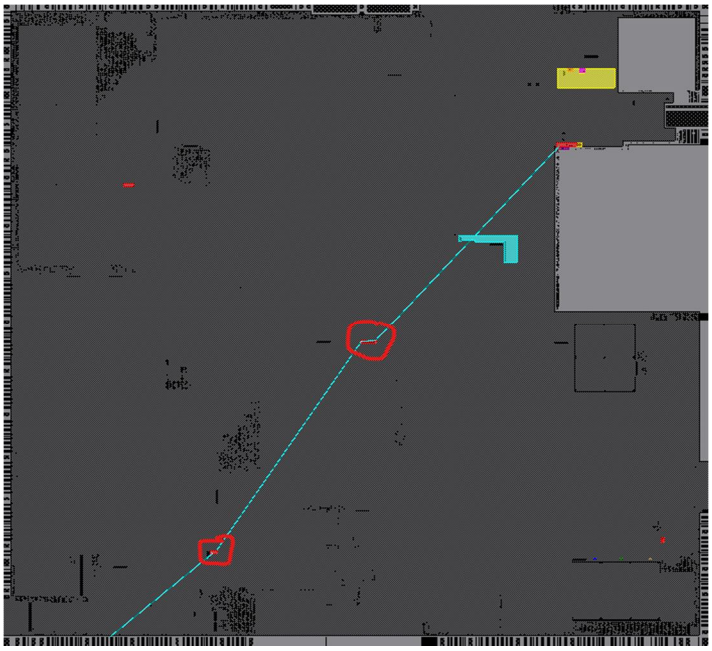
2) Scenario 2: Based on the sink and driver being in same power domain , yet the routes are longer.

On Route Buffering for these nets with Max allowed Buffer at regular intervals can help solving the transition issues.

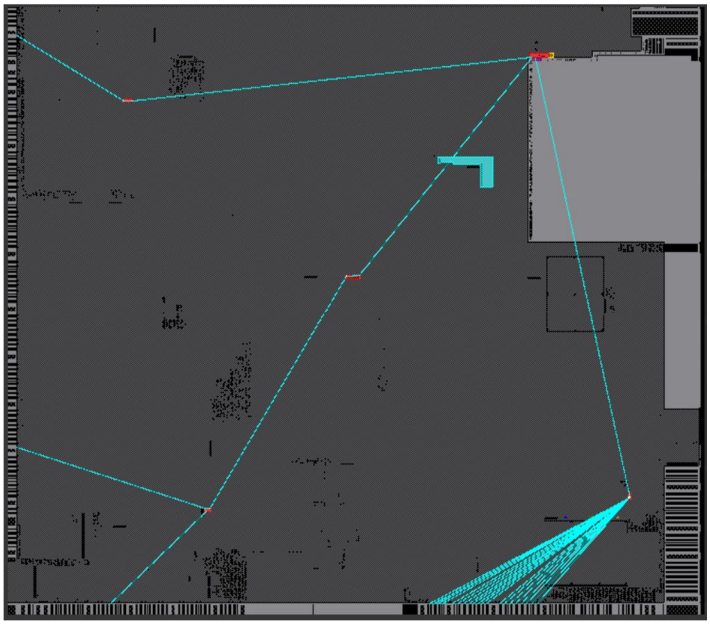
eco_add_repeater -net core_inst/MSB_PD1_Nets -cells ULT_BUF_S_8 -first_spread_distance 50 -spread_distance 250

3) Scenario 3: Creating smaller voltage islands and placing the buffers only for breaking the distance.

The circled ones in Red are the smaller voltage islands create at the floorplan stage for the Buffering.



Multiple voltage islands have been created for these Nets travelling across the different Pads.



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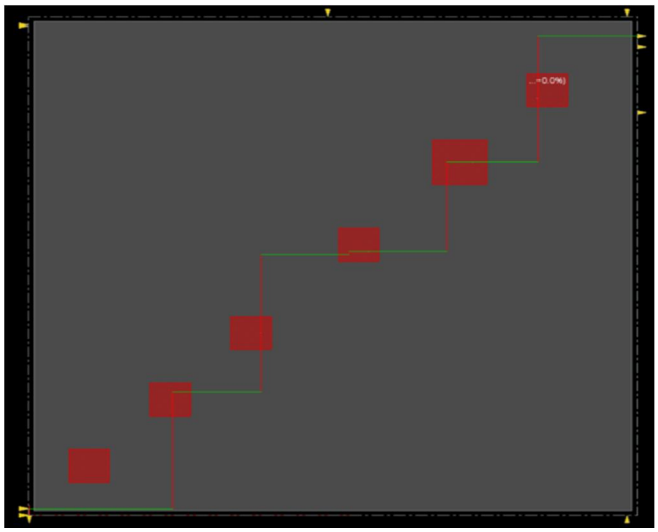
4) Scenario 4 : buffer the feedthrough ports of different power domains using normal buffers.

In certain designs, top-level signals that traverse through a block (feedthrough) may belong to different power domains than that of the block itself. To address slew violations on these feedthrough nets, it is necessary to insert buffers within the block.

- *Using Always-On Buffers:* Ensure that the always-on cell library is properly associated with the always-on power domain and that always-on buffers are enabled for use (i.e., set_dont_use is set to false).
- *Using Standard Buffers with **the Gas Station Method**:* When employing standard buffers, the gas station approach is required. This involves creating multiple isolated power domain regions where normal buffers can be inserted to maintain slew within acceptable limits - analogous to refueling a vehicle multiple times during a long journey to sustain its performance.



V. CONCLUSION

Addressing transition challenges in multi-voltage designs is critical for achieving robust and power-efficient systems. This paper bridges the gap between theoretical concepts and practical implementation by identifying the root causes of transition violations and presenting validated solutions to overcome them without performance degradation. By applying these methodologies, designers can ensure standard cells operate within their characterized .lib parameters, meet power-performance-area (PPA) targets, preserve signal integrity across voltage domains, and maintain clock quality without compromising power efficiency. As semiconductor technology continues to advance, adopting such holistic approaches is vital for the successful development and deployment of complex SoCs. Further enhancements can be made by implementing this strategy on designs with more congestion and multiple power domains.

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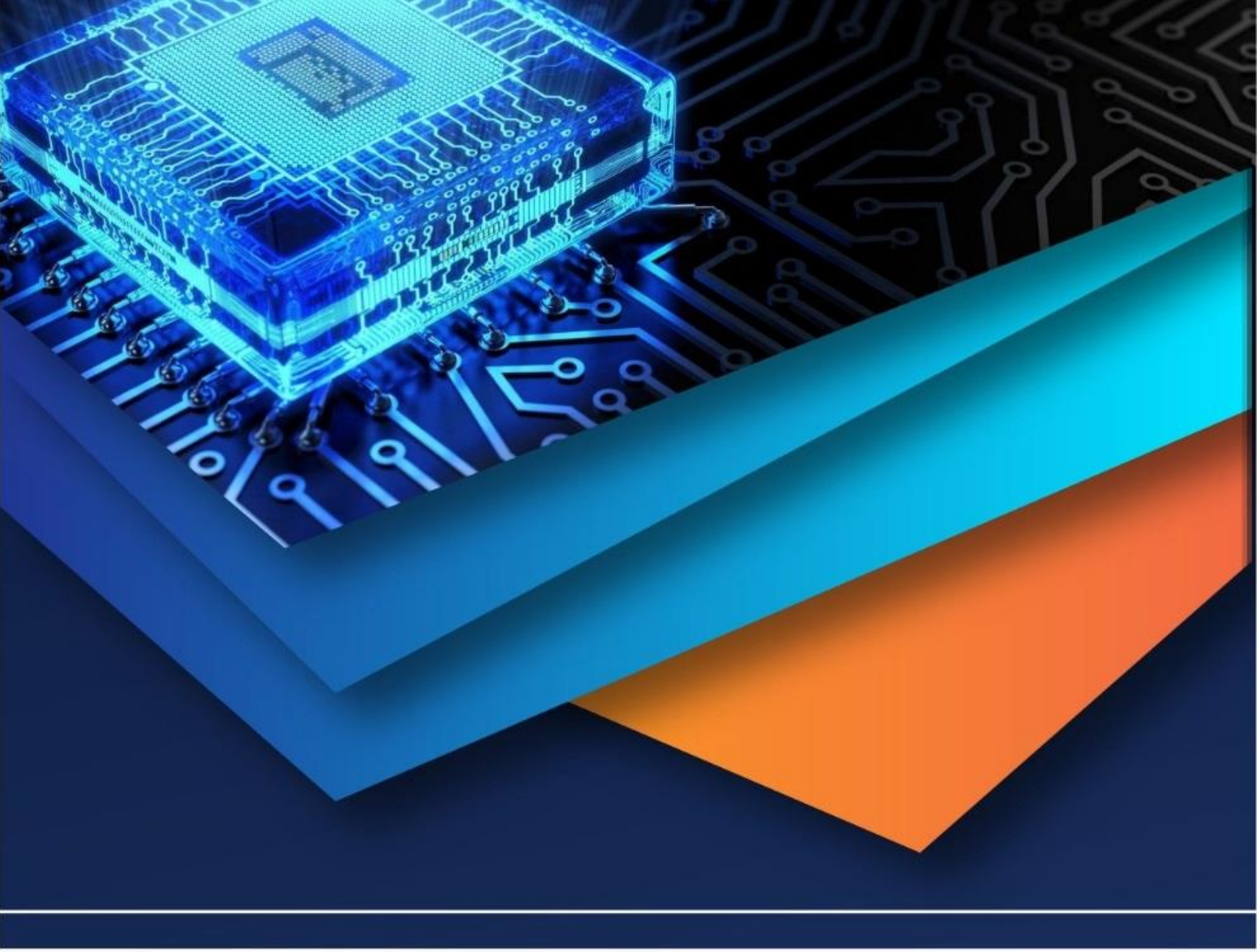

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