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An Enhanced Strong ARM Comparator Circuit for Analog to Digital Converter Architectures

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Abstract: ***Technological innovations in the current century period have motivated professionals to make electronic gadgets smarter. These advancements are progressing at a brisk pace, facilitating faster changes and increase in computing power. Various technologies such as virtual reality, augmented reality, mobile internet, artificial intelligence, cloud computing, biometric devices, 3D printing machines, genomics, quantum computing, block-chain, industrial automation and robotics. In all these technologies, communications with nearby devices play a major role in its effective functioning. The demand for realizing a smart and better usage experience puts forth strict requirements on the design aspects of next-generation high speed low power CMOS receiver design. One of the major modules in the implementation of high speed low power CMOS receiver device is the analog to digital converter (ADC) architecture. In the process of conversion from analog to digital signals, Quantization and sampling operations are vital and are realized using comparator circuits. The comparator design has a significant role in the design of data converter architecture. Several comparator architectures exist, but StrongARM topology is discussed and implemented in this work due to its negligible static power dissipation and rail to rail output voltages. The proposed novel comparator architecture is designed and simulated in 180nm CMOS process using Cadence Virtuoso tool and operated at supply voltage of V_{DD}=1.8V, a clock frequency of 50MHz.***

Keywords: Low offset, Kick back noise; Comparator; StrongARM; Double-tail; Single-tail; Low power; L.

I. INTRODUCTION

Integrated circuit innovations in the current century period have inspired specialists to make electronic appliances smarter. These advancements are progressing at a brisk pace, facilitating faster changes and increase in computing power. Various technologies such as virtual reality, augmented reality, mobile internet, artificial intelligence, cloud computing, biometric devices, 3D printing machines, genomics, quantum computing, block-chain, industrial automation and robotics. In all these technologies, communications with nearby devices play a major role in its effective functioning. The fourth generation and fifth generation communications evolved to offer reliable and steadfast data transfer globally. At present the usage of high performance electronic gadgets enables high speed and safe access to the internet. The ever increasing demand of lower latency values, better connectivity, stable and high speed data transmission poses stringent requirements for next level high speed communication designs. The above high performance requirements are met by the inclusion of an efficient Analog to Digital Converter (ADC) architecture in the communication transceiver hardware. ADC architectures are essential and omnipresent in all receiver architectures.

Data converter architectures are key modules and are crucial in the implementation of various electronic equipment. Data converter architectures are classified as analog to digital converter (ADC) and digital to analog converter. ADCs transform continuous time voltage signals (i.e. real time measurement) to discrete time voltage signals (i.e. digital), whereas the DACs convert discrete time voltage signals (i.e. discrete in nature) to continuous time signals. Mixed mode architecture implementation requires both the ADC and DAC circuits on the same chip. The converter architectures operate on the principle of Nyquist theorem. The theorem specifies that the original analog signal voltage can be accurately restored from the obtained samples of the input analog voltage waveform only if waveform sampling rate is greater than or equal to two times the highest bandwidth of the input analog signal. This statement is very important in the signal conversion techniques and it also corresponds to the operating speed of the whole integrated circuit. Applications that demand high speed operation are augmented reality, mobile internet, artificial intelligence, cloud computing, home automation, biometric devices, virtual reality, 3D printing machines, genomics, quantum computing, block-chain, industrial automation and robotics. Thus the efficient design of a analog to digital converter circuit architecture is very important module to be considered in the implementation for these applications. In literature, several ADC architectures exist such as Flash type, successive approximation register type, sigma-delta type, two-step flash type, single slope and dual slope type etc., although the proposed comparator design is targeted for Flash type ADC architecture. The flash ADC is a very fast data converter architecture used for conversion of input analog signal voltages to digital signal voltages.

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The conversion of signal takes place in one cycle time-period. Even though the speed of operation is very high; it does suffer from drawbacks such as increased circuit complexity due to increase in resolution size, and inclusion of additional circuit block namely thermometer to binary code which inevitably rises the power consumption of the whole circuit..

Several comparator architectures are available in the previous works such as Single-stage, Two-stage, Open-loop, Push-pull, comparator driving large capacitive loads, Singe-tail, Double-tail, Triple-tail latch, Switched capacitor comparator, StrongARM comparators, Regenerative comparators, Fully-differential two and three stage latch comparators, and high speed comparator circuits comprising of cascaded preamplifiers, latches and output driver circuits. Circuit designers often trade-off with different specifications and prefer double-tail comparators for use in high speed data converter circuits. On the whole a comparator circuit is realized by a differential input pair consisting of PMOS and NMOS transistors followed by an active load stage, decision stage and an amplifying stage. For high speed circuits additional amplification stage may be added to the circuit. The different stages in a classic comparator circuit are presented in Fig.1.

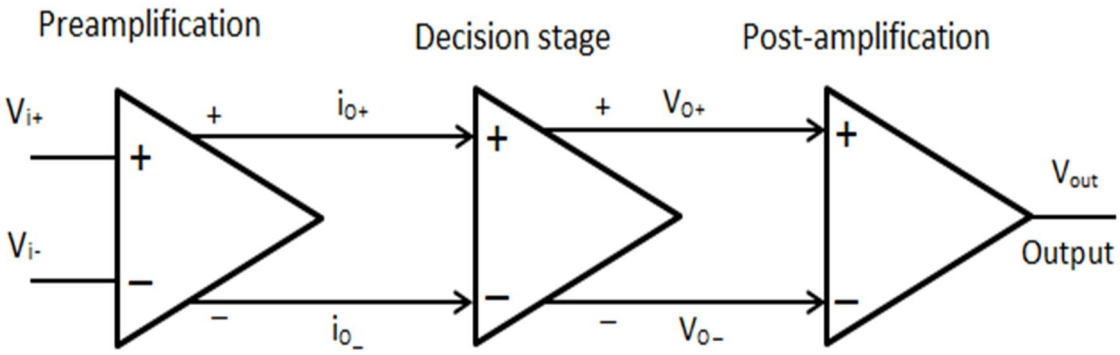


Figure 1. Inner blocks of a Comparator circuit

In general, a comparator circuit equates two signals (given input voltage with a standard reference voltage) and delivers a output discrete value i.e. logic or high levels.

The comparator circuits can also be used to detect a random signal whenever it crosses above zero or below zero reference voltage levels. The input preamplification stage circuit provides sufficient signal amplification levels before it is being fed at the output stage. This stage reduces the inherent kick-back voltage produced by the decision stage. The amplification of the circuit should be higher so as to provide necessary positive feedback in the circuit. The final stage also known as post-amplification stage is necessary to avoid the loading effect of the next following stages.

Kobayashi et. al. of Toshiba corporation has initially proposed the original StrongARM latch configuration for a 0.512MB high-speed static RAM circuit [1]. It includes a low powered current controlled latch sense amplifier for memory and interface circuits and the simulation results demonstrate the access time (pico-seconds) is minimized. The StrongARM comparator circuit is a familiar and extensively used topology in data converter architectures and flip-flop circuits for various high speed and low power transceiver circuits. It is a unique and robust circuit with features such as high sensitivity, offers rail-to-rail output voltage, very high input impedance for time varying signals, low input referred offset voltage arising due to only one differential pair and virtually no static power dissipation [2]- [3]. The authors in [4] describe a novel and simple dynamic bias comparator in 0.065micrometer CMOS technology. A complete mathematical analysis is carried out in both weak inversion and strong inversion operating regions of the comparator. The simulation results in this work demonstrate that the DC power consumption reduces by a factor of 2.5 times at an input common mode level of half the VDD. Mohtashemi et al., presented a novel comparator circuit exhibiting wider bandwidth [5]. The circuit doesn't use spiraled inductors and simulated at VDD=1.2Vdc and implemented in 130nm CMOS process. The authors in [6] compare strongARM and double-tail comparator circuits which include offset voltage compensation circuits. A parallel path based strongARM latch circuit is proposed in [7]. The simulation results in 0.065micrometer technology report that the operating speed enhances by almost 50% at a bandwidth of 3gigahertz. K.S.Kumar et al. described the design of a low offset voltage and high speed double-tail comparator for use in comparator array of a flash analog to digital converter architecture [8]. The comparator circuit is operated at VDD=1.8V and consumes power of 0.124mW. Ramamurthy et al. proposed a digital calibration technique to enhance the signal to noise distortion ratio almost to 20dB [9]. The authors in [10] present a novel pipelined ADC architecture in 180nm CMOS process. The methodology is based on by inserting a buffer circuit in second stage due to which offset voltage is eliminated without any delay.

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The proposed circuit was able to detect differences at the input differential stage. Khorami et al. describes the design of a two stage dynamic bias comparator which consists of p-channel MOS transistors in both the stages of the comparator architecture [11]. The modified strongARM comparator architecture along with its working details are discussed in Section-2, while Section-3 provides the simulated results and its discussion. To sum up Section-4 presents the conclusions of the presented work.

II. IMPLEMENTATION OF THE PROPOSED STRONGARM COMPARATOR ARCHITECTURE

The proposed modified StrongARM comparator circuit shown in Figure 2 operates in different phases namely reset, amplification and regeneration. The circuit consists of MOS switches M_{S1}, M_{S2}, M_{S3} and M_{S4}, a differential pair with a clock source (V_{CK}) and triple cross-coupled differential pairs (M_1 & M_2), (M_3 & M_4) and (M_5 & M_6) [12]- [13]. The tail transistor is driven with a clock source. The differential output voltage is taken at the drain nodes of M_5, M_6, M_7 and M_8. Correspondingly, the voltage at these nodes is designated as V_A and V_B. The main feature of this proposed StrongARM configuration is that it delivers rail-to-rail output voltages at nodes A and B.

The circuit responds to difference in the input voltages (V_{i1}-V_{i2}). In the first phase when the clock voltage is low i.e. V_{CK}=low, then the transistors M_1 and M_2 are off and accordingly the internal capacitances at nodes A, B, X and Y are precharged to the supply voltage V_{DD} through the MOS switches M_{S1}, M_{S2}, M_{S3} and M_{S4}.The next stage is the amplification phase, which gets initiated, when the clock voltage is high i.e. V_{CK}=high. With these connections, the MOS switches M_{S1}, M_{S2}, M_{S3} and M_{S4} are off and the charged voltage gets discharged through M_7, while M_1 and M_2 are conducting [14]- [16]. Transistors M_1 and M_2 are biased by a constant common mode voltage (V_{CM}). When there is a small difference in differential currents applied at M_1 and M_2 due to minute differences in (V_{i1}-V_{i2}), then the capacitances at the nodes X and Y are discharged at marginally different discharging rates.

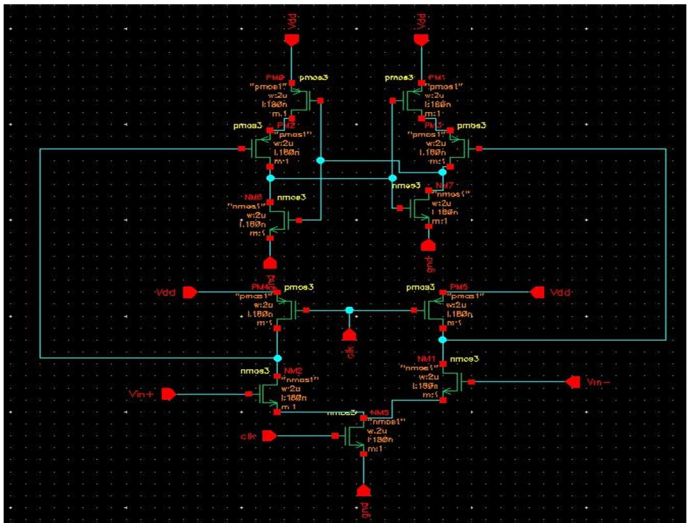


Figure 2. StrongARM comparator circuit

When voltages at X and Y drop to (V_{DD}-V_{tn}), transistors M_5 and M_6 turn ON. In this phase, the voltage $|V_X$-$V_Y|$ increases and certainly beyond (V_{i1}-V_{i2}). Hence in this stage, voltage amplification is achieved. The MOS transistors M_3 and M_4 are ON and its drain nodes are precharged to V_{DD}. Next when clock is its high level, the MOS transistors M3 and M4 are switched OFF. The transistor at the lower end of the circuit i.e. the tail transistor is switched ON and the capacitances at the drain nodes of M_3 and M_4 are discharged rapidly. Under these discharging conditions, the resulting common mode current flows through the tail transistor. Due to this the gate to source voltage of the input differential paper consisting of MOS transistors M_1 and M_2 is reduced, and thus creates a dynamic biasing voltage for the input differential pair [17]- [18]. The voltage keeps reducing until the effective voltage at the source of both the M_1 and M_2 transistors reach the minimum value of difference between inverting input, non-inverting input and threshold voltages. Correspondingly at this instant of time one of the input transistors either M1 or M2 is switched off. The other transistor which is conducting at the same instant of time will continue to discharge through its drain node. The preamplification stage consumes around (60 to 70) % of the total power dissipation of the circuit. To get lower noise, the overdrive voltage of the input differential transistors must be minimized.

Assuming $g_{m\,1,2}$ as the transconductance of the input transistors M_1 and M_2, the voltage difference is written as

$$|V_X - V_Y| = \left(\frac{g_{m\,1,2}\,(v_{i1}-v_{i2})}{C_{X,Y}}\right) * t \qquad (1)$$

The voltage gain in this phase is given by

$$A_V = \frac{g_{m\,1,2,3,4} * V_{tn}}{I_m} \qquad (2)$$

When the available voltage at nodes A or B reduces to the difference between the power supply voltage and threshold voltage of the p-type MOS transistor, due to this transistors M_7 or M_8 will be switched on to conduct, while the transistors M_5, M_6, M_3, M_4 remain in off state. Due to this operation, the voltage at nodes A or B reach either V_{DD} or logic low or vice-versa.

III. RESULTS AND DISCUSSIONS

The design and simulation of the proposed strongARM comparator circuit is carried out in 90nm CMOS process and the simulated transient analysis waveforms obtained at node 'A', Node 'B' and clock signal are displayed in Figure 3. The waveform consists of reset phase, amplification phase and regeneration phase. When the input differential voltage becomes more than or equal to 0.005V, then the comparator output produces a rail-to-rail swing voltage at the output side. The inherent clock feed through problem becomes negligible in both reset and amplification phases. In this proposed design, the amplification phase and regeneration phases operate slower than the reset phase time-periods.

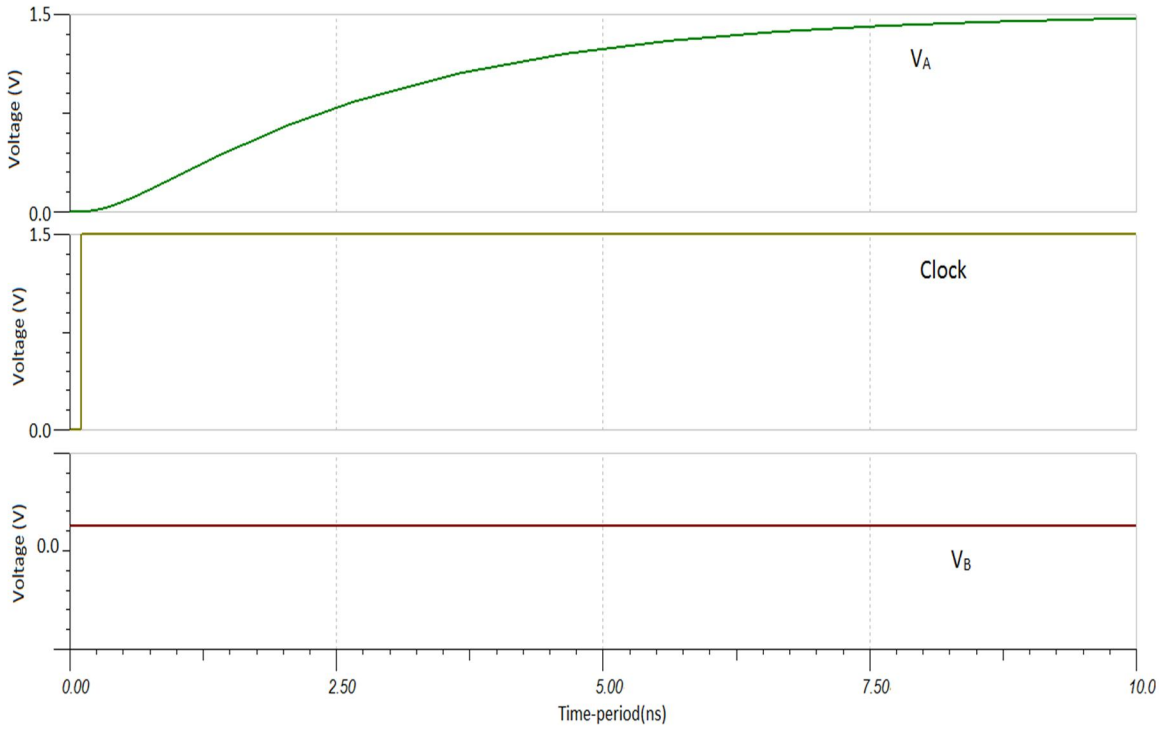


Figure 3. Simulated transient analysis waveforms

The simulated graphs related to the propagation delay (ps) versus differential input voltage are presented in Figure 4. The results illustrate that the proposed comparator circuit operates at lesser delay and correspondingly at higher speeds. The graphs illustrate that as the difference voltage (V_{i1}-V_{i2}) increases; there is a matching increase in operating speeds.

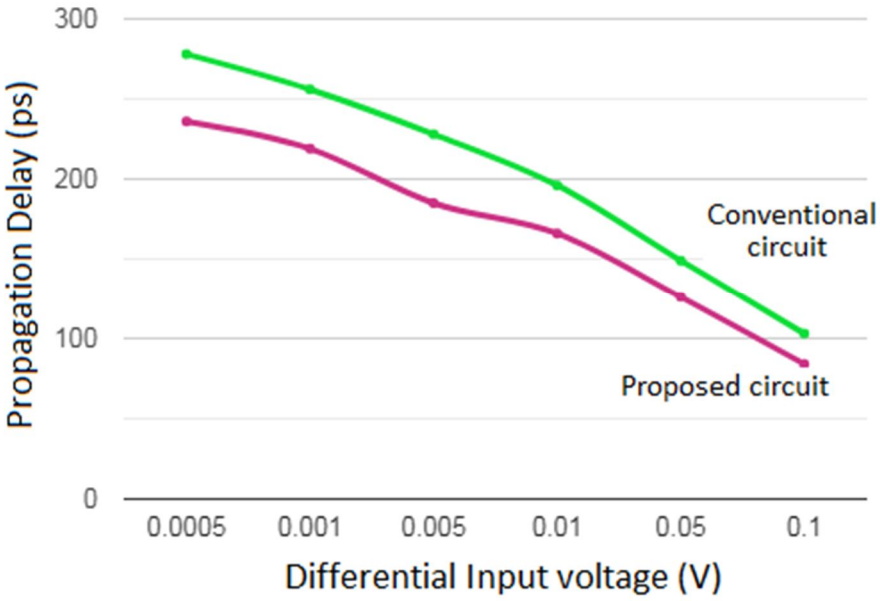


Figure 4. Simulated propagation delay versus differential input voltage

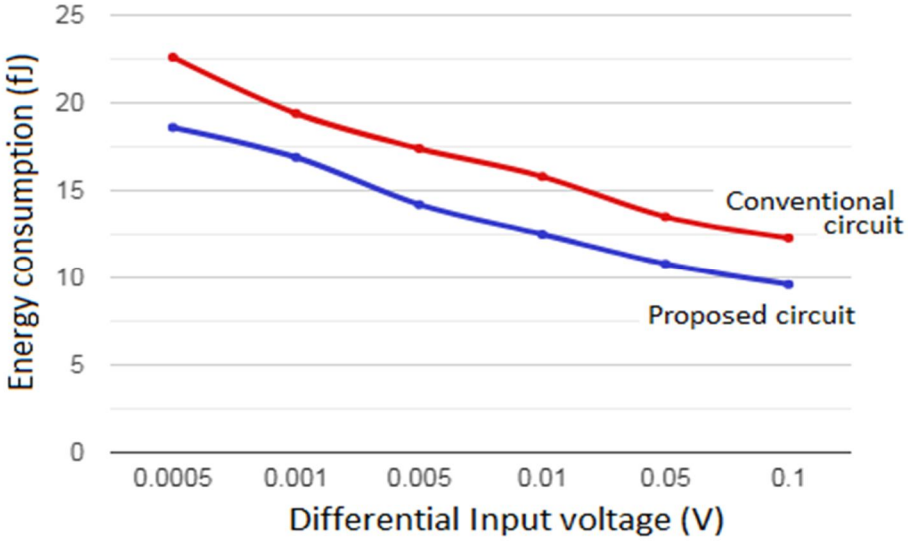


Figure 5. Simulated energy consumption versus differential input voltage

The simulated graphs related to the energy consumption (fJ) versus differential input voltage are displayed in Figure 5. The results illustrate that the proposed comparator circuit operates at reduced power levels. The graphs confirm that as the difference voltage (V_{i1}-V_{i2}) increases, there is a corresponding decrease in energy consumption levels.

IV. CONCLUSIONS

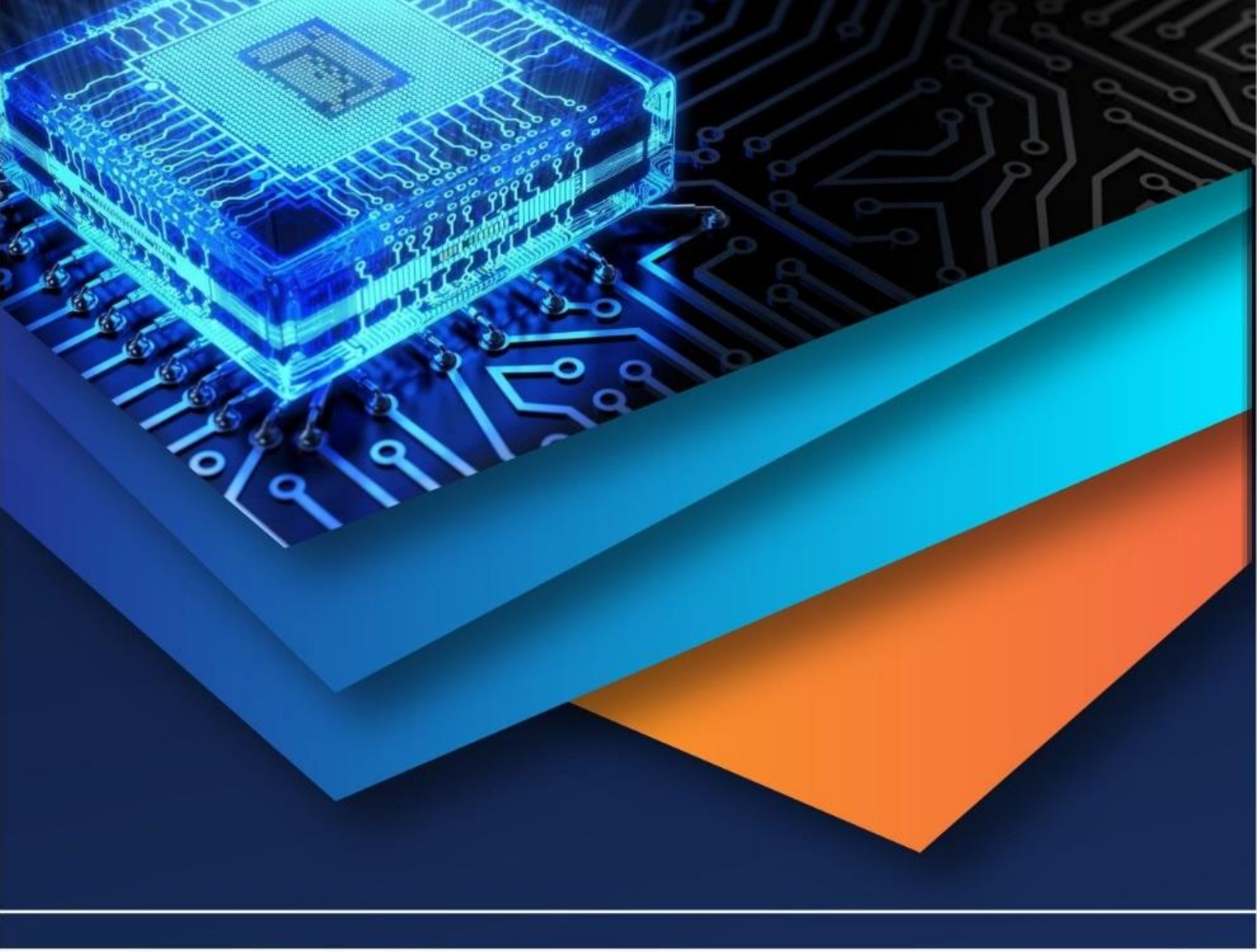
Due to the ever-increasing requirement of high performance comparator architectures, there is a strong need to make the transistor to operate at their saturation limits. The need for low voltage operation enforces severe requirements on the detection of quantized voltage levels. The presented work shows a modified novel strongARM latch circuit for analog to digital converter architectures. The comparator circuit is designed and simulated in 180nm CMOS process using Cadence Virtuoso tool and operated at supply voltage of V_{DD}=1.8V, a clock frequency of 100MHz. Consequently the proposed comparator architectural design would be an important choice in the implementation of a comparator bank in high speed flash analog to digital converter.

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