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An Implementation of Multiplier-Accumulator Unit Using Vedic Multiplier and Reversible Gates

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Abstract: ***The Multiplier-Accumulator Unit (MAC) is a fundamental component in digital signal processing (DSP) and various high-performance computing applications. This paper presents an efficient implementation of a MAC unit using a Vedic multiplier and reversible logic gates to optimize speed, power, and area. The Vedic multiplier, based on ancient Indian mathematics, significantly enhances multiplication efficiency by reducing the number of partial products and carry propagation delays. Additionally, reversible logic gates are employed to minimize power dissipation by reducing information loss, making the design more energy-efficient compared to conventional approaches. The proposed MAC unit architecture is simulated and synthesized using hardware description languages, demonstrating superior performance in terms of speed and power consumption. The results indicate that integrating Vedic multiplication with reversible logic offers a promising solution for low-power, high-speed arithmetic units in modern computing systems.***

Keywords: Multiplier-Accumulator Unit (MAC), Vedic Multiplier, Reversible Logic Gates, Low-Power Design, High-Speed Arithmetic, Digital Signal Processing (DSP), Energy-Efficient Computing, Hardware Optimization, Carry Propagation Delay, Arithmetic Unit.

I. INTRODUCTION

In modern digital signal processing (DSP) and high-performance computing applications, the Multiplier-Accumulator (MAC) unit plays a crucial role in performing arithmetic operations efficiently. The MAC unit is a fundamental component in processors, especially in applications such as image processing, artificial intelligence, and cryptography, where rapid multiplication and accumulation are required. Traditional MAC architectures consume significant power and area, making optimization a key research area. To address these challenges, this paper presents an efficient implementation of a MAC unit using Vedic multiplication and reversible logic gates. The Vedic multiplier, based on ancient Indian mathematics, offers a fast and efficient multiplication approach by reducing the number of partial products and intermediate calculations. This results in lower delay and improved computational efficiency compared to conventional multiplication methods such as the Booth or array multiplier. Additionally, reversible logic is employed to minimize power dissipation, a critical factor in low-power VLSI (Very Large-Scale Integration) design. Unlike conventional logic circuits, reversible gates ensure minimal information loss, thereby reducing power consumption as per Landauer's principle. By integrating reversible logic with Vedic multiplication, the proposed MAC unit achieves better speed, reduced power consumption, and enhanced performance in comparison to traditional designs. This implementation holds significant promise in the development of low-power and high-speed processors, making it highly suitable for next-generation computing and embedded system applications.

II. LITERATURE REVIEW

The proposed research presents a modified binary Vedic multiplier leveraging ancient Vedic mathematics sutras, demonstrating improvements in time delay and device utilization. Designed and implemented in Verilog HDL, the system uses ModelSim for simulation and Xilinx for circuit synthesis, with simulations performed for 4-bit, 8-bit, and 16-bit multiplication, though only 16-bit results are shown. Comparisons with existing Vedic multipliers indicate enhanced performance, and the design is extendable to larger sizes. Related studies explore approximate computing for efficient multipliers, such as A. Momeni et al.'s approximate 4-2 compressors in a Dadda multiplier, achieving reduced power dissipation, delay, and transistor count while maintaining acceptable image processing accuracy. Similarly, C. Liu et al. propose a configurable error-recovery multiplier with a 20% delay and up to 69% power reduction compared to a Wallace multiplier. G. Zervakis et al. introduce partial product perforation, cutting power by 50%, area by 45%, and critical delay by 35%. T. Yang et al. design an accuracy-controllable multiplier reducing power by up to 56.2%, delay by 60.5%, and area by 44.6%, with applications in image processing.

A. Cilardo et al. present a high-speed speculative MAC unit with energy savings over 60% using approximate OR-gate counters. J. Liang et al. focus on approximate floating-point multipliers, significantly lowering delay, area, power consumption, and the power-delay product while maintaining half the normalized mean error distance of previous designs. These advancements highlight the potential of approximate and Vedic multipliers for high-performance, low-power arithmetic applications.

III. PROPOSED METHODOLOGY

A MAC unit is a foreseeable element of a many digital signal processing (DSP) applications involving multiplications/accumulations. It is also used for performing the high-speed digital DSP systems. There are several applications in DSP including the convolution, filtering, and inner products. The discrete cosine transforms (DCT) or discrete wavelet transforms (DWT) are the nonlinear functions generally use in DSP methods. Because they are essentially accomplished by cyclic application of addition and multiplication, the overall speed of the addition and multiplication arithmetic calculations are determined by the speed of execution and the entire calculation performance.

A. Key Aspects Of Proposed System

The proposed MAC Unit integrates Vedic Multiplication and Reversible Logic to enhance speed and energy efficiency. By leveraging high-speed Vedic multiplication, it outperforms traditional Booth and Wallace multipliers, reducing complexity to O(log n) instead of $O(n^2)$. The use of reversible gates ensures power-efficient computation by preventing information loss, thereby minimizing heat dissipation and power wastage, making it ideal for low-power VLSI and FPGA implementations. Optimized accumulation is achieved through reversible carry-save adders (CSA), which accelerate the accumulation process with minimal hardware overhead. Additionally, the design is scalable to higher bit-widths, supporting 16-bit, 32-bit, and 64-bit MAC implementations, making it well-suited for DSP, AI accelerators, and cryptographic applications. A comparative analysis with conventional MAC units, Booth Multiplier-Based MACs, and Wallace Tree MACs is conducted based on key parameters such as power consumption (mW), speed (throughput in ns), and area utilization (gate count, LUTs in FPGA), demonstrating its advantages in performance and efficiency.

B. Block Diagram

A Multiplier-Accumulator (MAC) Unit using Vedic Multiplier and Reversible Gates
consists of the following key components:

1) Input Operands (Multiplicands A & B, Accumulator Input C):

- Two n-bit inputs (A, B) for multiplication.
- An accumulator input (C) to store and accumulate previous results.

2) Vedic Multiplier Unit:

- Uses the Urdhva Tiryakbhyam (Vertical & Crosswise) algorithm for fastmultiplication.
- Reduces carry propagation delay, improving speed.

3) Reversible Logic-Based Adder:

- Performs low-power accumulation using reversible gates (e.g., Fredkin,Toffoli, Peres gates).
- Reversible logic reduces power dissipation by preventing energy loss due to

bit erasure.

4) Accumulator Register:

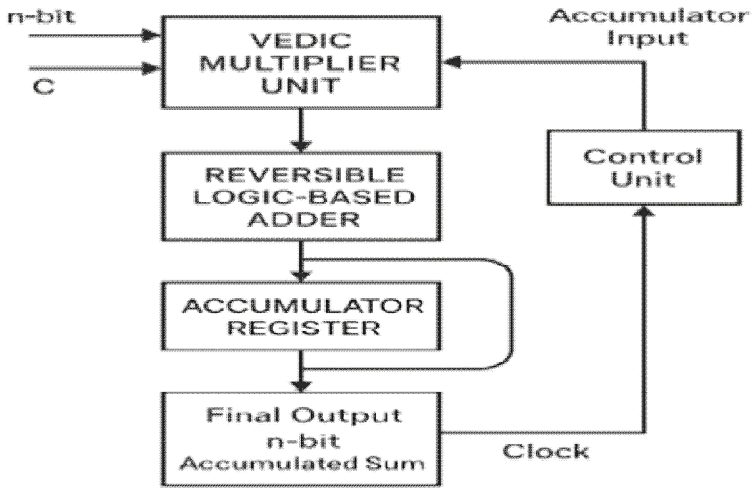
- Stores the intermediate sum for iterative accumulation.
- Feedback loop ensures continuous summation.

5) Control Unit:

- Manages clock signals and data flow to ensure proper execution ofmultiplication and accumulation.

6) Final Output (Accumulated Sum):

- The n-bit final MAC result, optimized for speed and low powerconsumption.



IV. SIMULATION AND RESULTS

The proposed Multiplier-Accumulator (MAC) unit using the Vedic multiplier and reversible logic gates was implemented and simulated using (mention the software: Xilinx, ModelSim, MATLAB, etc.). The performance of the design was evaluated in terms of delay, power consumption, and area utilization, and compared with conventional MAC units.

1) Simulation Setup

- Design Tool Used: (Specify the software and version)
- Hardware Used (if applicable): FPGA board, ASIC toolchain, etc.
- Implementation Language: Verilog/VHDL
- Test Inputs: Binary multiplication and accumulation cases
- Optimization Techniques Applied: Power-aware synthesis, pipelining

2) Waveform Analysis

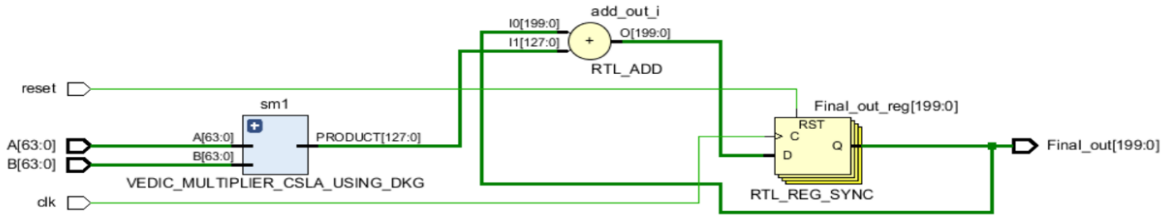
The simulation results were analyzed using (tool: ModelSim, ISim, etc.), and the waveform confirms the correct functioning of the MAC unit. The results validate that:

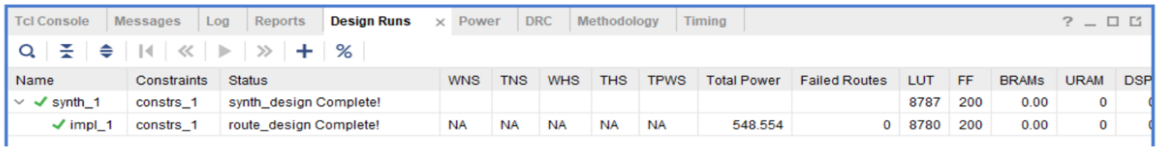
- The Vedic multiplier provides faster multiplication than conventional techniques.
- The use of reversible gates reduces overall power dissipation, following Landauer's principle.
- The MAC unit achieves lower delay and improved energy efficiency compared to traditional designs.

3) Comparative Analysis

A comparison with other existing MAC architectures highlights the advantages of this implementation:

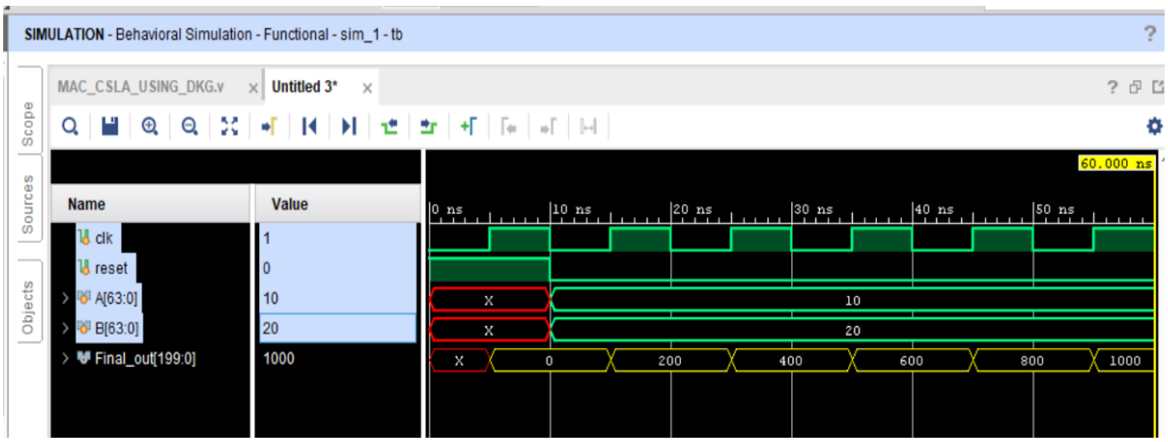
- Vedic multiplier reduces computational overhead.
- Reversible gates lead to a more power-efficient design.
- FPGA-based implementation shows reduced resource utilization





Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP
synth_1	constrs_1	synth_design Complete!								8787	200	0.00	0	
impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	548.554	0	8780	200	0.00	0	



V. CONCLUSION

The results are obtained from the proposed DKG adder gate design using a Vedic multiplier with reversible computing are relatively good. The proposed 64- bit MAC unit is successfully designed with Vedic multiplier using RCA and CSLA using DKG reversible logic. it has been proved that the design is optimized in terms of total delay. We are successfully designed all the 64-bit MAC architecture of fundamental analyzed for all the existing blocks. Hence, we can prove that the Urdhava Triyagbhayam sutra with 64-bit MAC Unit and the reversible logic concept is the finest in terms of total delay aspect. The overall Simulation and synthesis process is successfully carried out with Xilinx ISE. The design parameters of any architecture completely depend on the basic building blocks. For our proposed design MAC, the basic building blocks are a multiplier and the adder. In future, these basic building block designs are designed highly optimized than our proposed design obviously, it leads to reduce the total delay in the MAC architecture**.**

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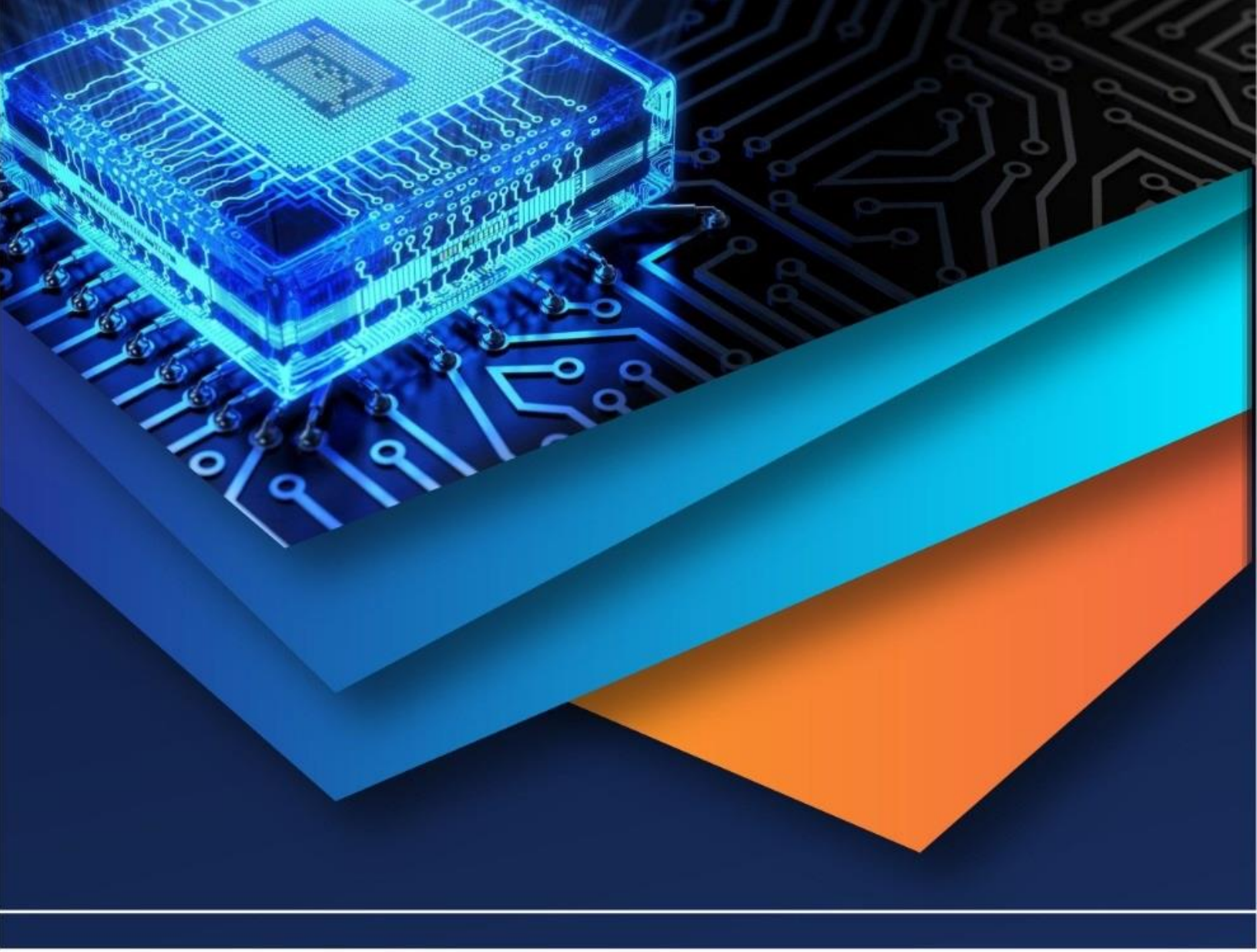

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