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An Optimization-Enhanced Low Power ALU Design using Clock Gating and Power Gating

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Abstract: ***Low-power Arithmetic Logic Units (ALUs) form the computational backbone of modern energy-efficient digital systems, particularly in battery-powered and thermally constrained platforms such as Internet of Things (IoT) devices, mobile processors, and large-scale data centers. As semiconductor technologies continue to scale, power dissipation due to switching activity and leakage currents has emerged as a dominant limitation, often constraining performance, reliability, and system lifetime. Although conventional low-power techniques such as clock gating and power gating have shown promise, their static and heuristic-driven application is often insufficient to cope with dynamic workload variations and complex architectural interactions.***

This work presents an Optimization-Enhanced Low-Power ALU (O-ALU) that integrates metaheuristic-driven control with adaptive power management to achieve superior energy efficiency without compromising computational performance. The proposed architecture employs workload-aware activity monitoring combined with clock gating and power gating mechanisms that are dynamically optimized using intelligent search algorithms. This enables fine-grained, real-time adaptation of ALU sub-modules based on operational demand.

The O-ALU is implemented and evaluated on an FPGA platform, and its performance is analyzed in terms of hardware resource utilization, dynamic and static power consumption, and execution efficiency. The experimental results demonstrate that the proposed design achieves significant reductions in both switching and leakage power while maintaining comparable throughput and latency to conventional ALU architectures. Moreover, the modular organization and adaptive control logic ensure scalability and robustness across varying workloads and technology nodes.

Overall, the O-ALU provides a practical and effective solution for next-generation low-power processor design, offering a balanced trade-off between energy efficiency, performance, and architectural complexity.

Keyword: Low-Power ALU, Clock Gating, Power Gating, Metaheuristic Optimization, FPGA, Energy-Efficient Computing, Embedded Systems, VLSI Design

I. INTRODUCTION

The rapid evolution of embedded and digital systems demands high-performance, energy-efficient ALUs. Power consumption, driven by dynamic switching and leakage currents, is a major bottleneck in VLSI design. Techniques such as clock and power gating, combined with intelligent optimization, enable reduced energy consumption without sacrificing computational performance.

The design of low-power ALUs has become a central focus in modern digital systems due to the growing demand for high performance, energy efficiency, and environmental sustainability. With the rapid expansion of portable devices, embedded platforms, and high-performance computing systems, power consumption has emerged as a primary design constraint alongside speed and functionality. Consequently, techniques such as clock gating, power gating, operand isolation, and architectural restructuring are now essential for achieving efficient ALU operation across diverse computing platforms.

Low-power ALUs are particularly critical for battery-powered devices such as smartphones and IoT nodes, where extended operational life is required, as well as for data centers and supercomputers, where power and cooling costs are significant. However, implementing these techniques introduces challenges related to design complexity, area overhead, latency, and process variability in advanced semiconductor technologies. Therefore, designers must carefully balance power savings with performance, reliability, and manufacturing cost. In conclusion, optimized low-power ALU architectures represent the foundation of modern energy-efficient computing. By effectively integrating clock gating, power gating, and advanced optimization strategies, these ALUs enable high-speed computation within strict energy budgets, thereby supporting a sustainable and scalable digital ecosystem ranging from embedded systems to exascale computing platforms.

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A. Overview of ALU

The ALU is the core computational unit of a processor that performs arithmetic and logical operations, generates status flags, and controls decision-making and program flow.

1) Components of ALU: An ALU consists of arithmetic and logic units, a shifter, multiplexer, status register, and a control interface that together execute and manage all operations.
2) Classification of ALU: ALUs are classified into ripple carry, carry look-ahead, bit-slice, and high-speed ALUs based on their speed, complexity, and scalability.
3) ALU Architectures: ALU architectures include ripple carry, carry look-ahead, parallel, and multi-operand designs, each offering different trade-offs between speed, power, and area.
4) Role of ALU in Modern Processors: The ALU determines CPU performance and throughput, supports pipelining, and enables parallel and specialized computation in multicore processors.
5) Challenges in Conventional ALUs: Traditional ALUs suffer from high power consumption, leakage at nanometer scales, thermal issues, and area constraints, especially in embedded systems.
6) Power Consumption in Digital Circuits: Power consumption in digital circuits is a critical design concern, dominated by dynamic switching and static leakage currents.
7) Sources of Power Dissipation: Power dissipation arises mainly from dynamic power during switching and static power due to leakage in transistors.
8) Dynamic Power: Dynamic power is consumed when circuit capacitances are charged and discharged during logic transitions [1].
9) Static Power (Leakage): Static power results from subthreshold leakage, gate oxide tunneling, and junction leakage even when transistors are idle.
10) Factors Affecting ALU Power: ALU power depends on clock frequency, operand width, instruction mix, switching activity, and leakage in inactive units.

B. Importance of Low-Power ALUs

1) Low-power ALUs are essential to improve energy efficiency, thermal reliability, and operational cost across computing platforms.
2) Portable Devices: Low-power ALUs extend battery life, reduce heat, and eliminate the need for bulky cooling systems in portable electronics.
3) IoT Systems: Energy-efficient ALUs enable long-term operation of IoT devices using small batteries with minimal maintenance.
4) Data Centers and HPC:Low-power ALUs reduce electricity and cooling costs while supporting sustainable high-performance computing.
5) Trade-offs: Designing low-power ALUs involves balancing power with performance, chip area, and dynamic versus static power.

C. Low-Power ALU Design

Low-power ALU design focuses on reducing energy consumption while maintaining high computational performance.

1) Reasons: The need for low-power ALUs arises from increasing computational demands, thermal and battery limitations, and sustainability goals.
2) Low-Power Techniques: Techniques such as clock gating, power gating, operand isolation, DVFS, and activity-aware control
3) Environmental Importance: Low-power ALUs reduce energy usage and CO_2 emissions, supporting environmentally sustainable and green computing.

D. Power Reduction Techniques in ALU

The control unit, after the ALU, is one of the largest power consumers in a processor. To achieve energy-efficient operation, modern ALU designs employ a combination of techniques that reduce both dynamic power caused by switching activity and static power due to leakage currents. Among these, clock gating and power gating are the most effective, supported by operand isolation, voltage scaling, and circuit-level optimizations.

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Efficient ALU power reduction is achieved by combining **clock gating** for dynamic power control and **power gating** for leakage suppression, along with operand isolation, DVFS, and transistor-level optimizations. Together, these methods enable high-performance ALUs to operate within strict power and thermal constraints.

E. Optimization Approaches in ALU

A low-power ALU cannot rely on a single technique such as clock gating or power gating alone; instead, it requires a multi-level optimization strategy spanning architectural, logic, and circuit levels, along with corresponding physical-design optimizations to achieve effective energy efficiency. There various are various ALU Optimization Approaches as shown in Figure 1

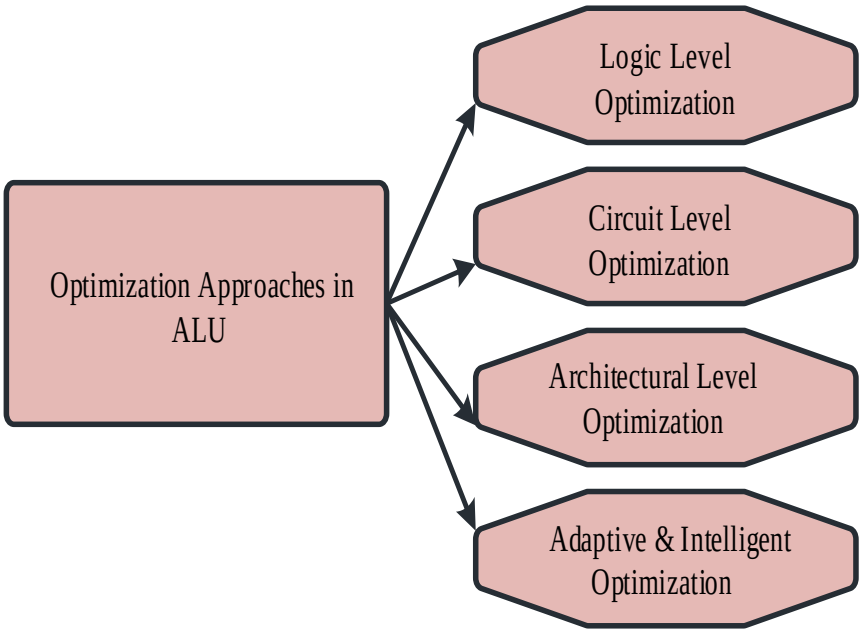


Figure 1 ALU Optimization Approaches

F. Logic-, Circuit-, and Architectural-Level Optimization in Low-Power ALUs

1) Logic-Level Optimization: At the logic level, power is reduced by simplifying Boolean expressions, sharing common gate-level structures, and minimizing glitches. Techniques such as Boolean simplification, gate-level sharing between arithmetic and logic operations, and balanced signal paths reduce redundant hardware and unnecessary switching, thereby lowering dynamic power.

2) Circuit-Level Optimization: Circuit-level techniques focus on minimizing parasitic effects and leakage through careful transistor sizing, multi-threshold CMOS (MTCMOS), and power-supply partitioning. Advanced approaches such as adiabatic and reversible logic further enhance energy efficiency by recycling charge instead of dissipating it as heat.

3) Architectural-Level Optimization: At the architectural level, power savings are achieved by selectively activating only the required functional units, isolating idle operands, and sharing hardware resources across multiple bit-width operations. Dynamic voltage and frequency scaling (DVFS) further adapts the ALU's operating conditions to the workload, ensuring optimal performance with minimum energy consumption.

II. METHODOLOGY

The design of low-power ALUs has become a central focus in modern digital systems due to the increasing demand for high performance, energy efficiency, and environmental sustainability. With the rapid growth of portable devices, embedded platforms, and high-performance computing systems, power consumption has emerged as a critical design constraint alongside speed and functionality. Consequently, techniques such as clock gating, power gating, operand isolation, and architectural restructuring are now essential for achieving efficient ALU operation across diverse computing platforms.

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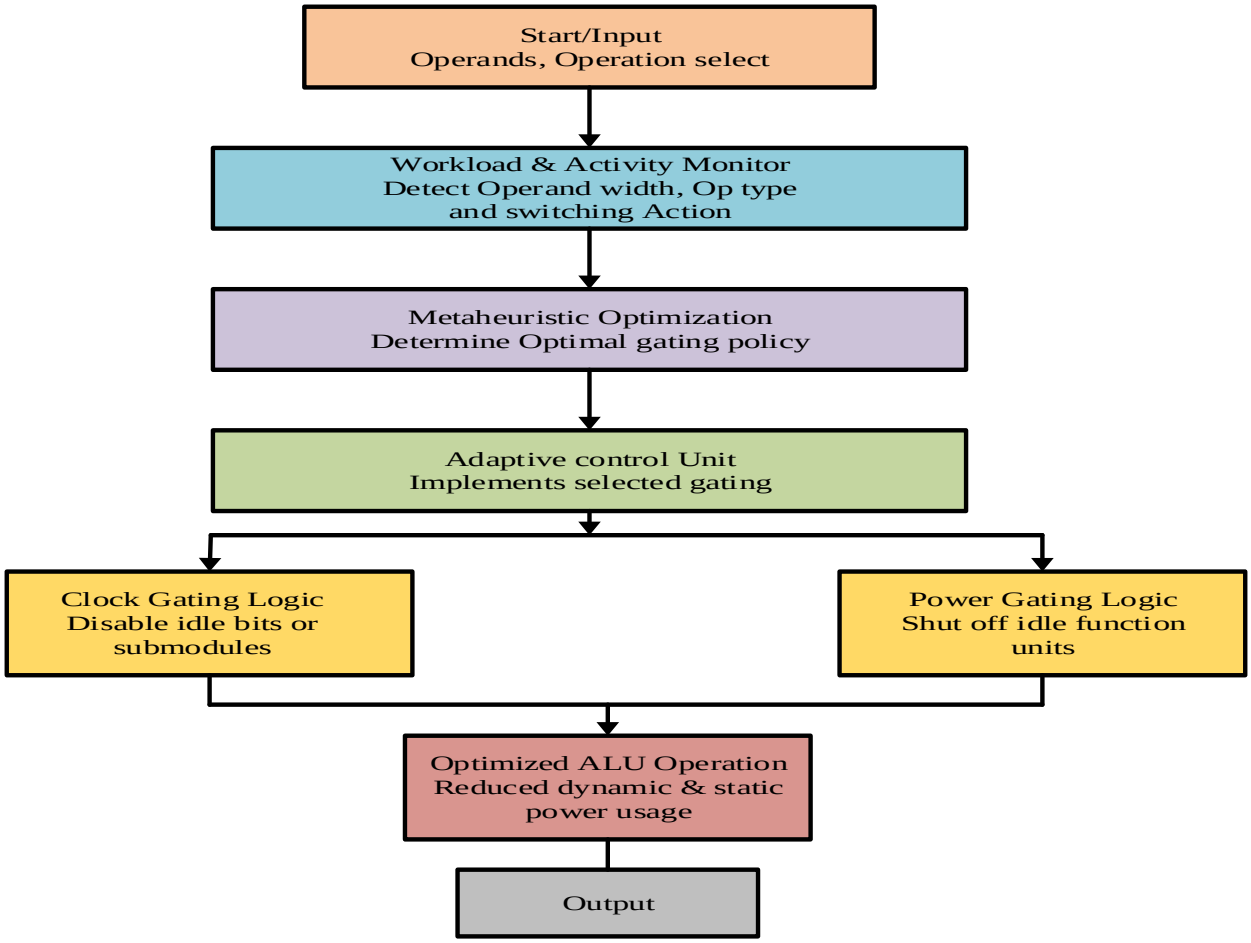


Figure 2 Proposed Methodology Flow

Low-power ALUs are especially vital for battery-powered devices such as smartphones and IoT nodes, where extended operational lifetime is required, as well as for data centers and supercomputers, where power and cooling costs dominate operational expenses. However, the adoption of these techniques introduces challenges related to design complexity, area overhead, latency, and process variability in advanced semiconductor technologies. Therefore, designers must carefully balance power reduction with performance, reliability, and manufacturing cost.

In conclusion, optimized low-power ALU architectures form the backbone of modern energy-efficient computing. By integrating clock gating, power gating, and advanced optimization strategies, these ALUs enable high-speed computation within strict energy budgets, supporting a sustainable and scalable digital ecosystem from embedded systems to exascale computing platforms. The proposed methodology flow as shown in Figure 2

The figure illustrates an optimization-based control framework for a low-power ALU in which workload and activity are monitored and processed by a metaheuristic optimizer to generate optimal clock and power gating policies. An adaptive control unit then dynamically enables or disables ALU sub-blocks, minimizing energy consumption while maintaining performance.

III. RESULTS

A. Simulation and Implementation Results

1) Clock Gating Optimization

Clock gating is employed to reduce dynamic power by disabling the clock to inactive ALU components. In this design, gating is applied at both the register level, to prevent unnecessary flip-flop switching, and at the functional unit level, where entire submodules such as adders, shifters, and logic units are turned off when idle. Instruction-dependent clock gating further improves efficiency by enabling only the functional units required for the current operation. As shown in Figure 3.

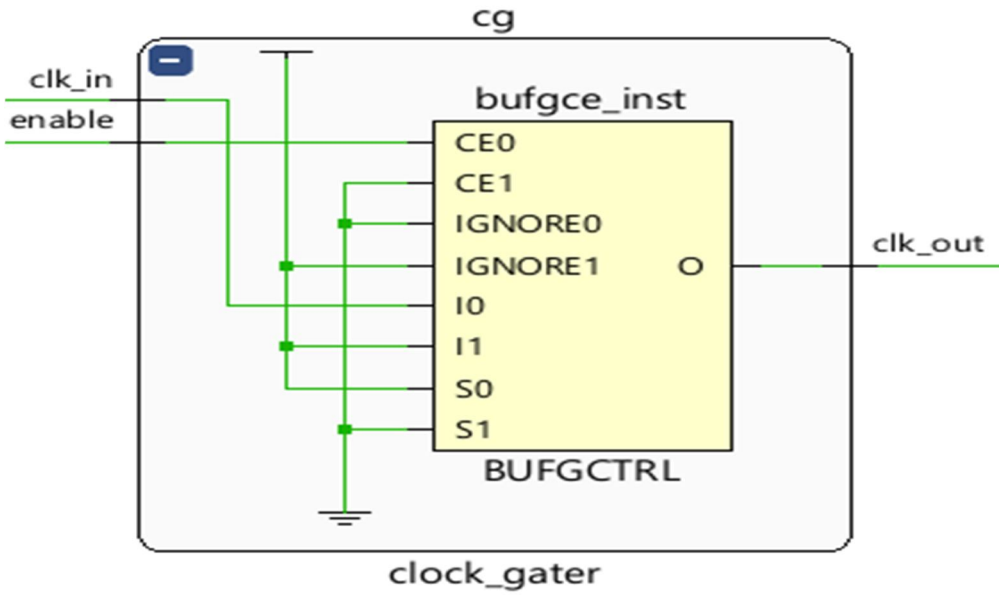


Figure 3 RTL Schematic of Clock Gate Block

2) Power Gating Optimization

Power gating, a state-of-the-art low-power design technique, disconnects idle functional units from the power source in order to completely cut off power and consequently leakage. This system uses sleep transistors to implement the power gating technique, which prevents static current leakage during the non-operating period by allowing currents to trickle through from the supply of the dormant ALU blocks. As shown in Figure 4

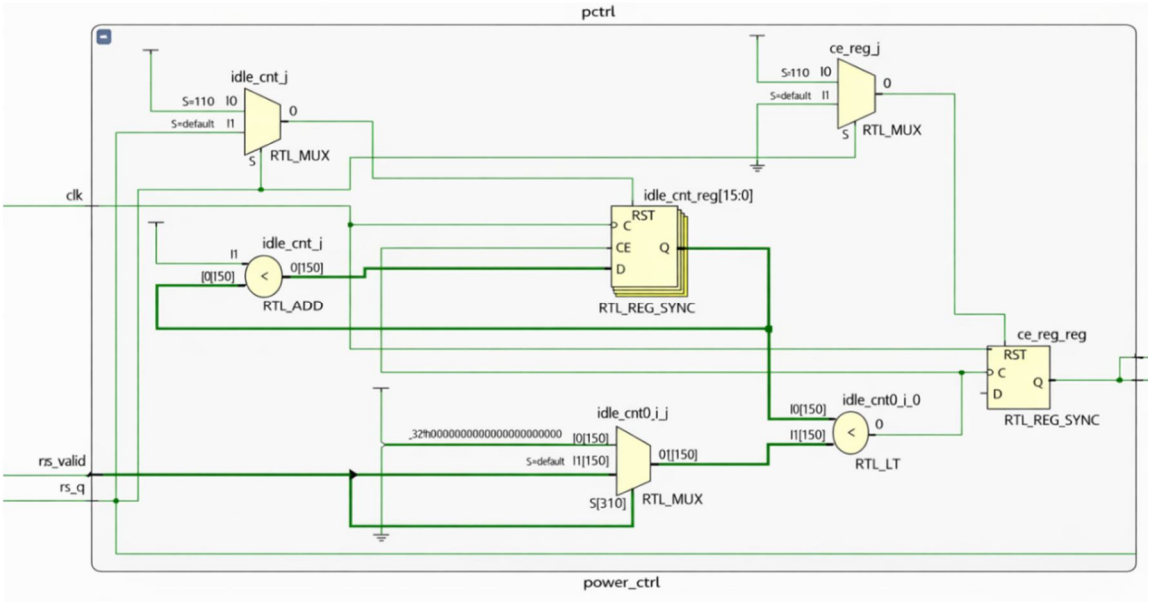


Figure 4 RTL schematic of power control Block

3) Simulation Results (VLSI)

The simulation results demonstrate that the proposed VLSI design operates reliably and efficiently under different operating conditions. Power distribution analysis obtained from Fig. 5.10 and Fig. 5.11 indicates that the DSP blocks consume 2.707 W (18%), routing resources consume 2.093 W (14%), logic resources consume 0.588 W (4%), and I/O blocks consume the highest power at 10.049 W (64%). This shows that I/O activity and DSP processing are the dominant contributors to total power consumption.

Thermal analysis further confirms safe operation of the design. The junction temperature is 54.3 °C at an ambient temperature of 25 °C, providing a thermal margin of 30.7 °C. This indicates that the system remains well below its thermal limit, ensuring reliable and stable operation without overheating.

Overall, the results verify that the proposed architecture achieves efficient power utilization while maintaining thermal safety and operational stability.

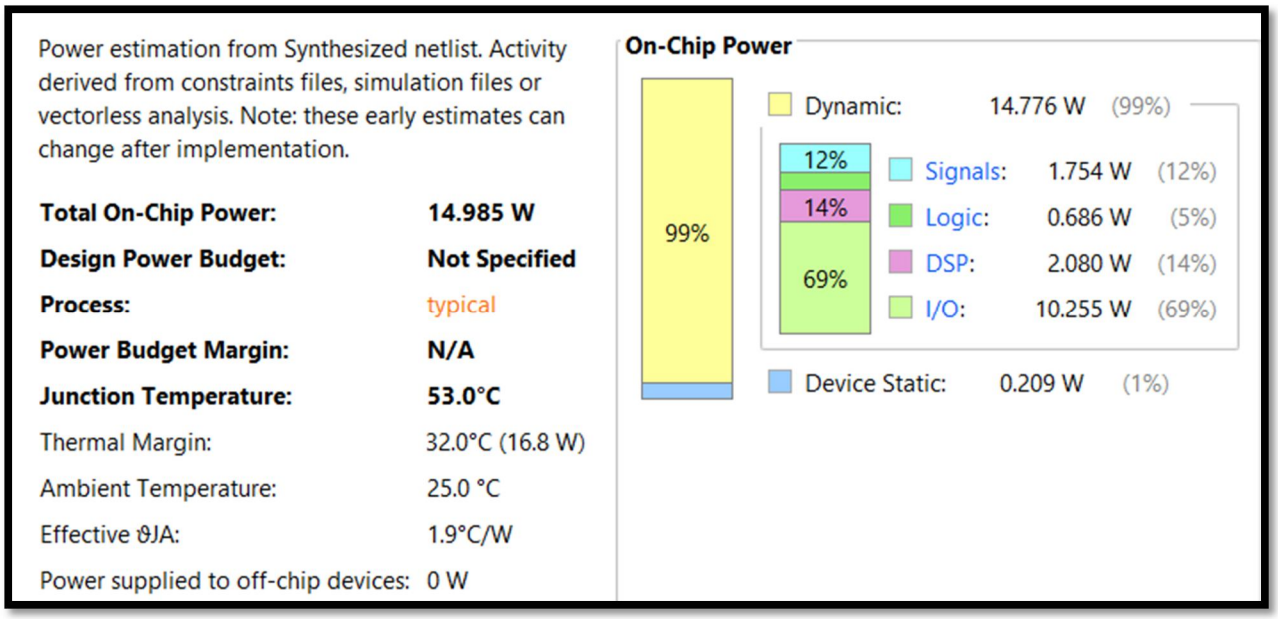


Figure 5 Synthesized Power Report

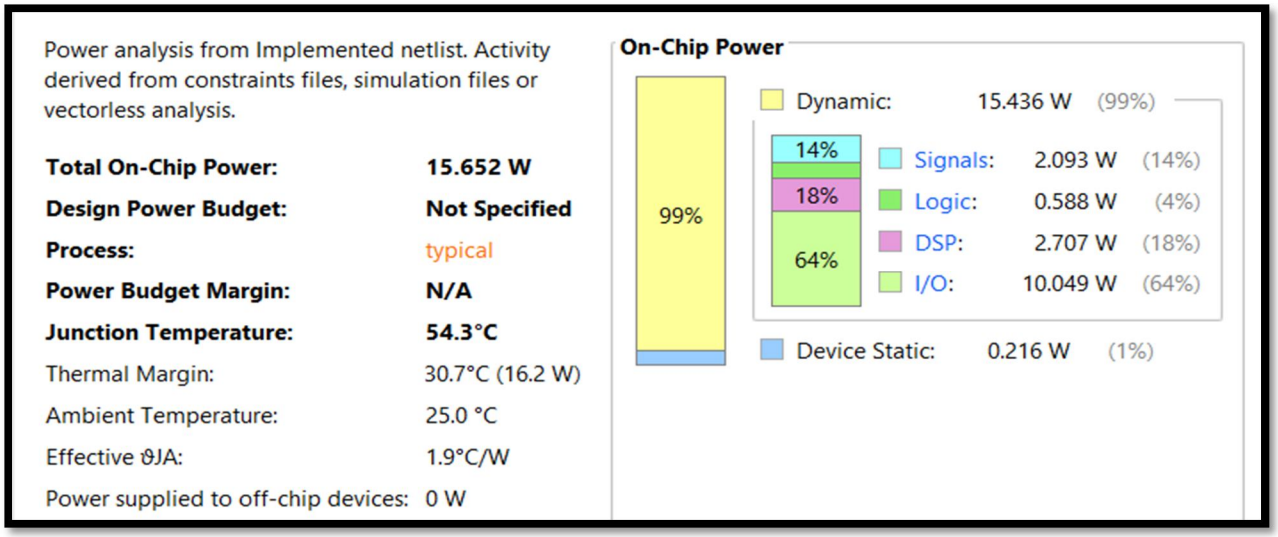


Figure 6 Implementation Power Report

IV. CONCLUSION

Here we presented a comprehensive evaluation of the proposed Optimization-Enhanced Low-Power ALU (O-ALU) through detailed analysis of hardware utilization, power consumption, and performance metrics obtained from FPGA-based implementation. The objective was to verify whether the integration of metaheuristic-guided clock gating and power gating can effectively reduce energy consumption while maintaining reliable computational performance. The results clearly demonstrate that the proposed O-ALU meets these objectives.

The resource utilization analysis shows that the O-ALU achieves an efficient and balanced use of Slice LUTs, registers, and DSP blocks. Although additional control and optimization logic is introduced to support adaptive power management, the overhead remains within acceptable limits. The modular structure of the arithmetic, control, and register units further enhances scalability and enables easy portability across different VLSI platforms and technology nodes.

Power analysis confirms a substantial reduction in both dynamic and static power compared to conventional ALU designs. Dynamic power savings are mainly achieved through activity-aware clock gating, which suppresses unnecessary switching in idle or partially active sub-modules. Static power is reduced through power gating, which disconnects inactive functional units from the power supply, thereby minimizing leakage currents. The metaheuristic optimization framework plays a key role by continuously determining the optimal gating strategy based on real-time workload characteristics.

Performance evaluation indicates that the O-ALU maintains comparable latency and throughput to traditional ALUs, despite the aggressive power-saving techniques employed. This shows that the trade-off between power efficiency and performance is effectively managed by the adaptive control framework. The design is therefore capable of supporting diverse workloads without compromising computational reliability.

Overall, the results validate the proposed O-ALU as a scalable, adaptable, and energy-efficient arithmetic unit suitable for modern power-constrained applications. Its ability to deliver high performance under strict energy budgets makes it particularly attractive for IoT devices, portable electronics, and real-time embedded systems. The findings of this chapter strongly support optimization-driven power management as a promising approach for next-generation low-power processor design.

REFERENCES

[1] Jahanirad, H. (2023). Dynamic Power-Gating for Leakage Power Reduction in FPGAs. Frontiers of Information Technology & Electronic Engineering, 24, 582–598. *https://doi.org/10.1631/FITEE.2200084*

[2] Sharma, M., Khanna, V., Tonk, A., & Ruhil, S. (2025). Implementation and Comparative Analysis of Various Low-Power FSM Synthesis Techniques. Journal of Electronics and Power Engineering, 2(1), 54–66.

[3] Agarwal, P., Garg, T. K., & Kumar, A. (2024). Low-Power Embedded System Design Applications Using FPGAs. In Embedded Devices and Internet of Things (pp. 1–20). CRC Press. *https://doi.org/10.1201/9781003510420-1*

[4] Balaji, K. V., Kannan, K. N., Balaji, V. R., Priya, V., Sivaraju, S. S., & Duraivel, A. N. (2024). ASIC Design and Implementation of 32-Bit Arithmetic and Logic Unit. EAI Endorsed Transactions on the Energy Web, 11(1). *https://doi.org/10.4108/ew.6035*

[5] Hosamani, R., Rakesh, H., Shettar, R. B., & Y. G., P. K. (2021). Realization of an 8-Bit Pipelined RISC Processor Using Verilog HDL.

[6] Duggi, N., & Rajula, S. (2021). Implementation of Low-Area ALU Using Reversible Logic Formulations. In Springer Conference Proceedings. *https://doi.org/10.1007/978-981-33-4443-3_44*

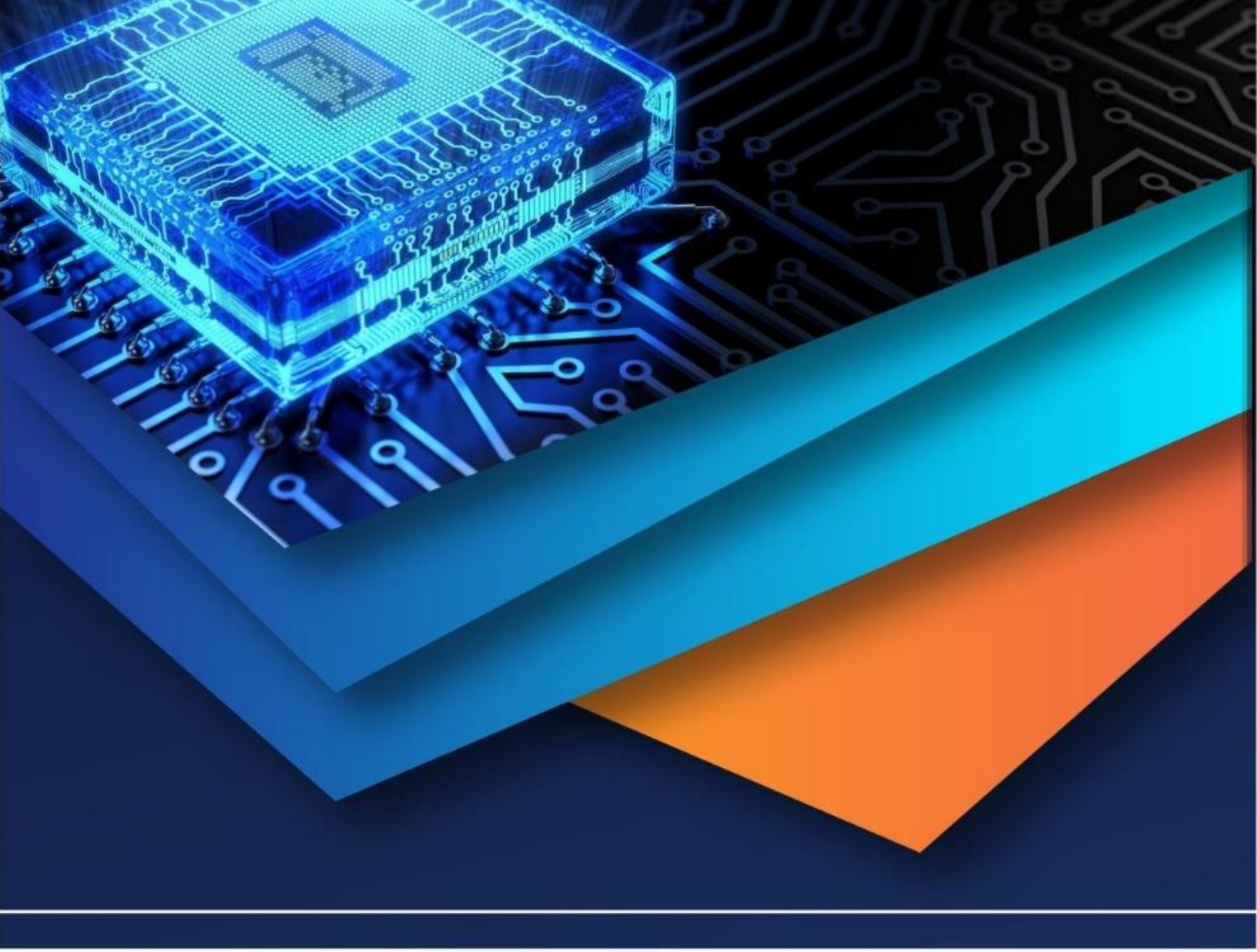
[7] Helander, J. (2024). Performance Monitoring and Power Management for RISC-V Core.

[8] Fiore, L. (2021). Design of a Fault-Tolerant RISC-V Instruction Execute Stage for Safety-Critical Applications (Doctoral dissertation, Politecnico di Torino). *http://webthesis.biblio.polito.it/id/eprint/17869*

[9] Yang, S., Shao, L., Huang, J., & Zou, W. (2023). Design and Implementation of Low-Power IoT RISC-V Processor with Hybrid Encryption Accelerator. Electronics, 12, 4222. *https://doi.org/10.3390/electronics12204222*

[10] Hossain, M. S. (2021). Power Management Techniques for Ultra-Low Voltage Integrated Circuits (Doctoral dissertation, Drexel University).

[11] Oliveira, Á. B. D. (2023). Fault Tolerance Characterization of RISC-V Processors in SRAM-Based FPGAs for Aerospace Applications. *http://hdl.handle.net/10183/264018*



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