iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 12 **Issue:** V **Month of publication:** May 2024

DOI: https://doi.org/10.22214/ijraset.2024.62995

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue V May 2024- Available at www.ijraset.com

Analysis of 1-bit Full Adders in Cadence 45nm Technology

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Abstract: ***A full adder is a digital circuit that performs the arithmetic operation of addition on three binary digits, producing a sum and a carry output. Unlike a half adder, which adds only two binary digits and produces a sum and carry, a full adder considers an additional carry input from a previous less significant bit addition. The full adder's design includes three inputs: A, B, and Cin (carry-in), and two outputs: Sum (sum) and Cout (carry-out). The sum output Sum is derived by XOR-ing the three inputs, while the carry-out Cout is obtained by considering the majority function of the inputs. This means Cout is set when any two or more of the three inputs are high (logical 1). Full adders are fundamental components in the construction of arithmetic logic units (ALUs), binary adders, and other computational circuits in digital systems, enabling the handling of multi-bit binary addition by cascading multiple full adders.***

I. INTRODUCTION

The recent applications of VLSI(Very Large Scale Integration) such as audio and video processing, microprocessors and digital signal processing etc., using arithmetic operations are becoming more important. In past times VLSI applications are mainly depends on area, reliability and cost rather than power. The power increasing demand and low delay was mainly due to latest growth of electronic products such as portable mobile phones, laptops and other devices needs high speed and low power consumption. The full adder is an important component for controller or processor design like microprocessors, digital signal processors etc. It is also used to do arithmetic and logical operations. In this paper the full adders are designed in various techniques and technologies. The project is aiming to analyse the delay ,power and gain characteristics of 10T full adders in different techniques and technologies. Finally, we conclude that which is the best design for applications.

II. LITERATURE SURVEY

1) Chandran Venkatesan, Thabsera Sulthana M, Sumithra M.G these authors presented that A 1bit full adder with various design techniques and their area, power delay are calculated using cadence 45nmtool environment with a supply voltage of 1.8V. This project finally concludes that 10T GDI technique is best in all measurements with low power. The circuit used a smaller number of transistors so area and leakage power can be reduced.

2) Manjunath K M, Abdul Lateef Haroon P S, Amarappa Pagi and Ulaganathan J. proposed that the circuits are designed in the virtuoso platform, using cadence tool with the available GPDK – 45nm kit. The Full-adder circuits with the most 28 transistors to the one with only 6 transistors are successfully designed, simulated and compared for various parameters like power consumption, speed of operation(delay) and area (transistor count), and finally concluded the best designs, that suite for the particular specifications.

3) Y. Sunil Gavaskar Reddy, V.V.G.S. Rajendra Prasad. Low-power, adiabatic logic, Full adder, CMOS, Pass transistor logic, Positive feedback adiabatic logic, Transmission. They have presented low power full adders by using the different CMOS techniques and adiabatic adder circuits are analysed in terms of power and transistor count in 0.18um technology.

III. AIM, OBJECTIVES AND ADDITIVE CIRCUIT

A. Aim

The main aim of the project is to analyse and compare the design parameters of various 10T full adders.

B. Objectives

The objectives of the project are

1) Designing and simulation of full adders in 10T various technologies in Cadence Virtuoso tool.

2) Measurement of parameters of the designed full adders in technology of FINFET.
3) Measurement of parameters of the designed full adders in technologies of GDI, SERF and CMOS.
4) Analysis and comparison of results of the measured parameters of designed and simulated full adders.

C. Additive Circuit

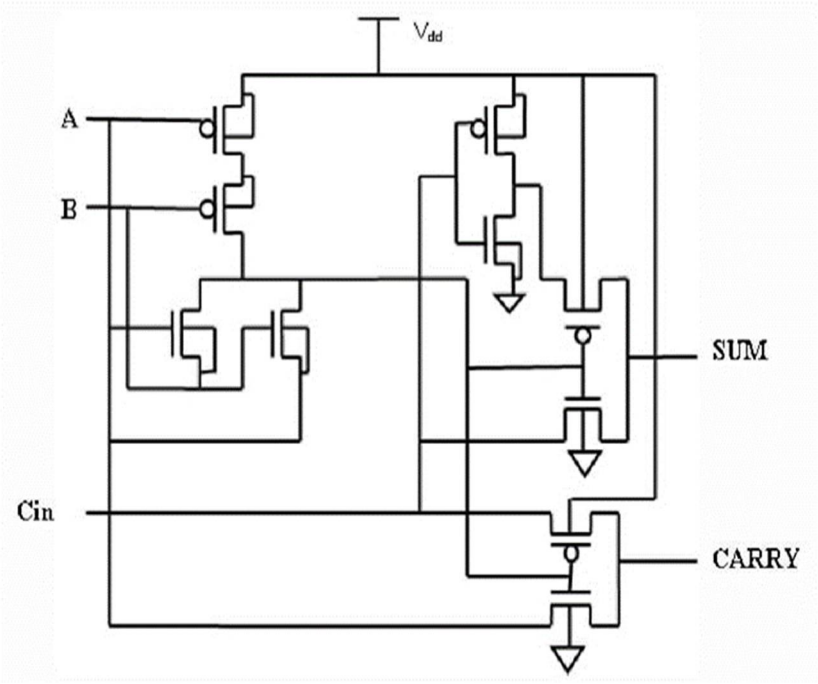
The Additive circuit that we are adding to the project is 10T FINFET full adder. FINFET stands for Fin Field-Effect Transistor which is a type of 3D Transistor used in modern semiconductor devices for improved performance and lower power consumption. FINFETs have better control over the channel, reducing short-channel effects that are common in traditional MOSFETs.

IV. SOFTWARE USED

Cadence Virtuoso is a prominent Electronic Design Automation (EDA) solutions provider, offering a comprehensive suite of tools for analog, mixed signal and integrated circuit (IC) design. It provides a suite of tools and features that enable us to process the design from initial schematic capture to final layout and verification.
The Key features of Cadence Virtuoso are Schematic Capture, Layout Editor, Simulation and Analysis, Design and Rue Checking, Physical Verification, Parametric Analysis and Custom Design.
The main Advantages of Cadence Virtuoso over other platforms are:
High precision, Comprehensive toolset and Industry Standard.

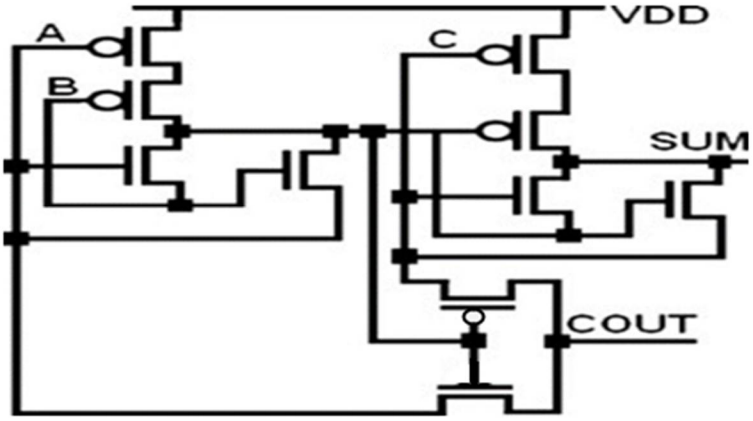
V. BLOCK DIAGRAMS

A. 10 T FINFET full adder



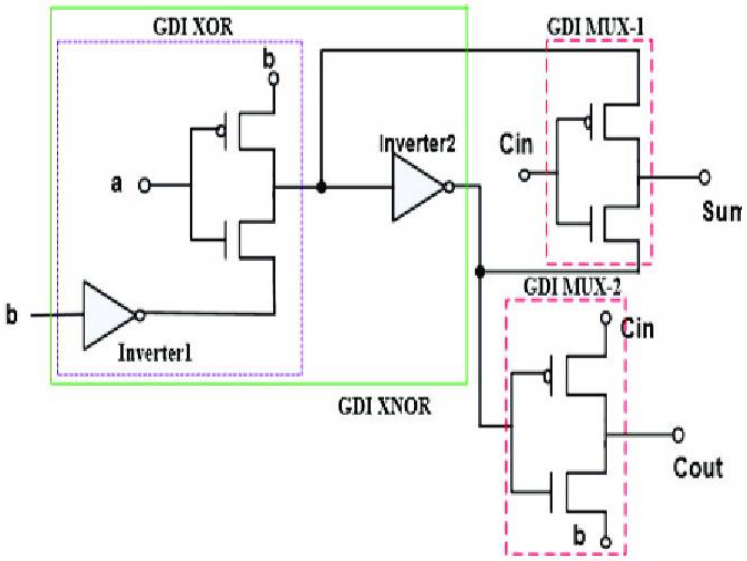
A 10-transistor (10T) full adder designed with FinFET technology at the 45nm scale offers significant improvements in performance, power efficiency, and area utilization. FinFET, known for their superior control over short-channel effects and reduced leakage current, enhance the operational efficiency of the full adder. By leveraging the three-dimensional
structure of FinFET, the 10T full adder achieves faster switching speeds and lower power consumption compared to traditional planar CMOS transistors. This design optimizes the number of transistors required for addition operations, which not only reduces the silicon footprint but also enhances the overall computational performance. Such a compact and efficient full adder is particularly advantageous in high-performance and low-power applications, including mobile devices, wearable technology, and other space-constrained VLSI systems, demonstrating the benefits of advanced FinFET technology in modern integrated circuit design.

B. 10 T CMOS full adder



A 10-transistor (10T) full adder implemented in 45nm CMOS technology is a highly efficient design for performing binary addition with minimal power consumption and area. This design utilizes only 10 transistors compared to the conventional 28-transistor full adder, achieving significant reductions in power dissipation and silicon area, which are critical in high-density VLSI circuits. The 45nm process technology enhances performance by providing faster switching speeds and lower power operation. Despite the reduced transistor count, the 10T full adder maintains reliable operation, making it suitable for low-power applications such as mobile and portable devices, where battery life is a key concern. The compact and efficient nature of the 10T full adder demonstrates the advancements in CMOS technology and design techniques aimed at optimizing digital circuits.

C. 10 T GDI full adder



A 10-transistor (10T) full adder implemented using Gate Diffusion Input (GDI) technique in 45nm CMOS technology offers significant improvements in power efficiency and area optimization. The GDI technique simplifies logic design by reducing the number of transistors required for complex operations, thus enabling the construction of a full adder with just 10 transistors. This reduction in component count directly translates to lower power consumption and reduced silicon area, which are critical for high-density and low-power applications such as mobile and IoT devices. The 45nm technology node further enhances performance by allowing for higher speed operation and lower voltage requirements. Despite the minimalist design, the 10T GDI full adder achieves reliable performance, making it an attractive solution for modern VLSI systems where efficiency and compactness are paramount.

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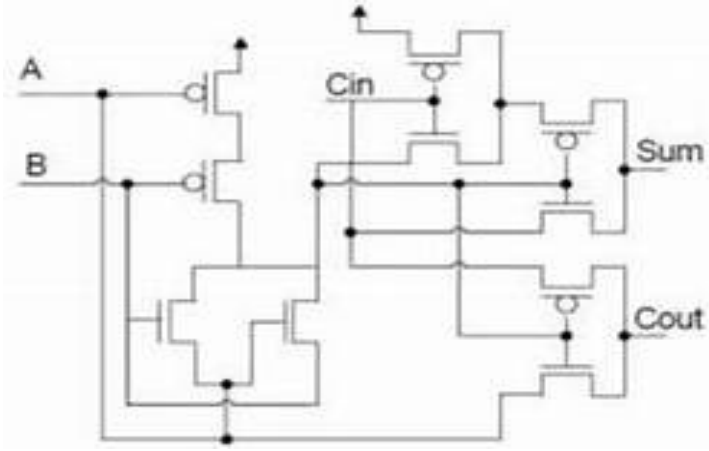
D. 10 T SERF full adder



A 10-transistor (10T) full adder using the Static Energy Recovery Full Adder(SERF) approach in 45nm CMOS technology represents a significant advancement in digital circuit design, prioritizing both power efficiency and area reduction. The SERF technique minimizes the number of transistors by effectively using pass-transistor logic to perform the full adder operation, resulting in a highly compact design. Implementing this in the 45nm process technology enhances performance characteristics, such as faster switching speeds and lower voltage operation, which are critical for power-sensitive applications like portable and battery-operated devices. The reduced transistor count not only decreases the silicon area but also lowers power dissipation, making the 10T SERF full adder an optimal choice for high-density VLSI systems where minimizing power and area is crucial without compromising on computational reliability.

VI. SCHEMATIC DESIGN AND SIMULATION RESULTS

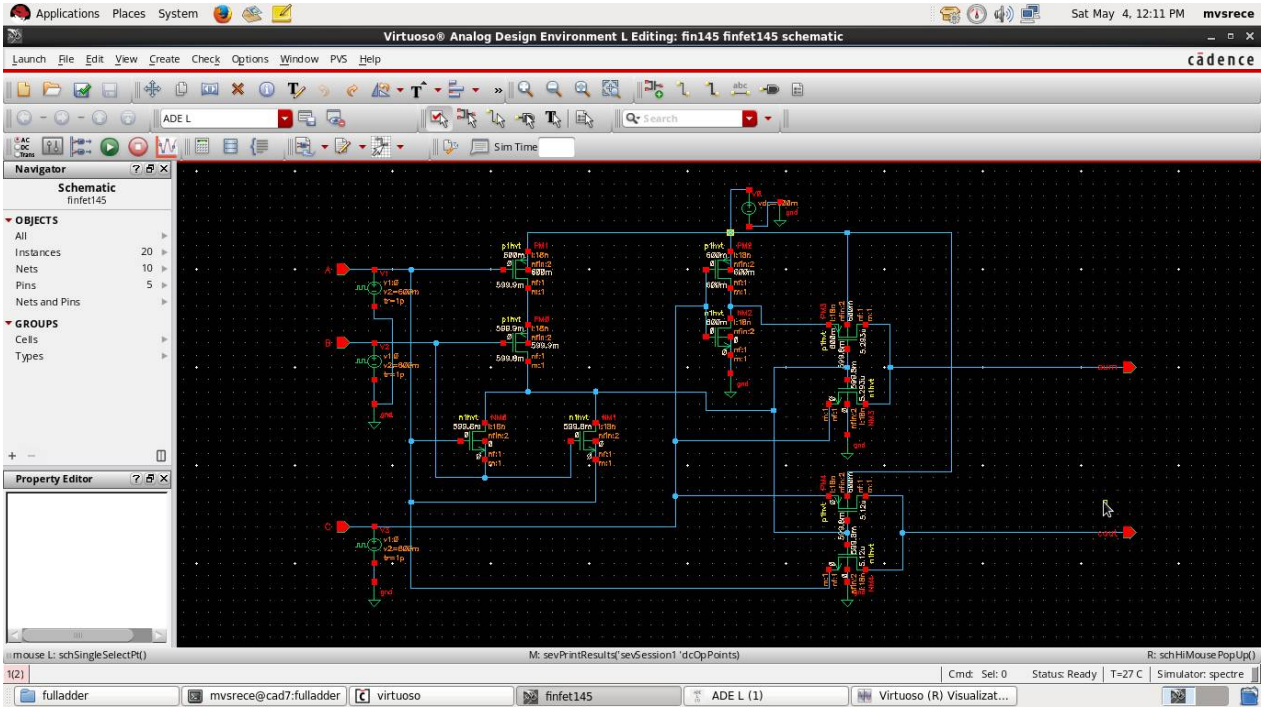


Fig. 1 Schematic of 10T FINFET full adder

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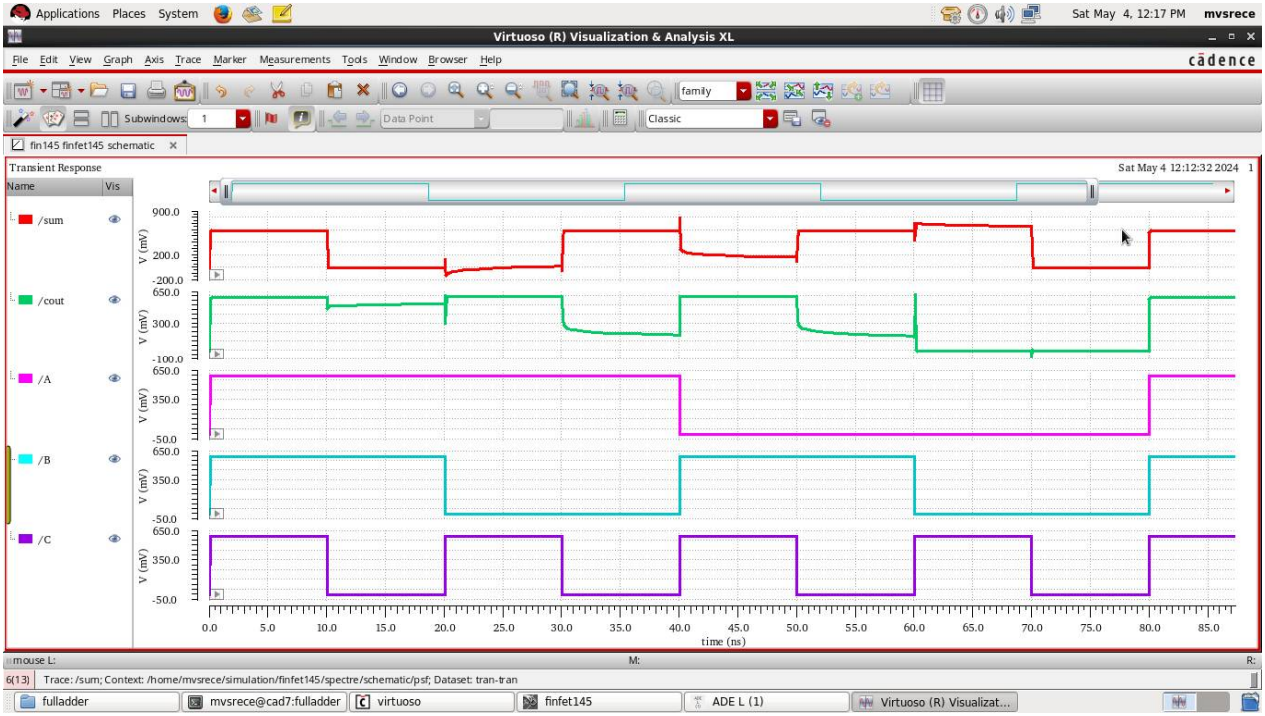

Fig. 2 Output of 10T FINFET full adder

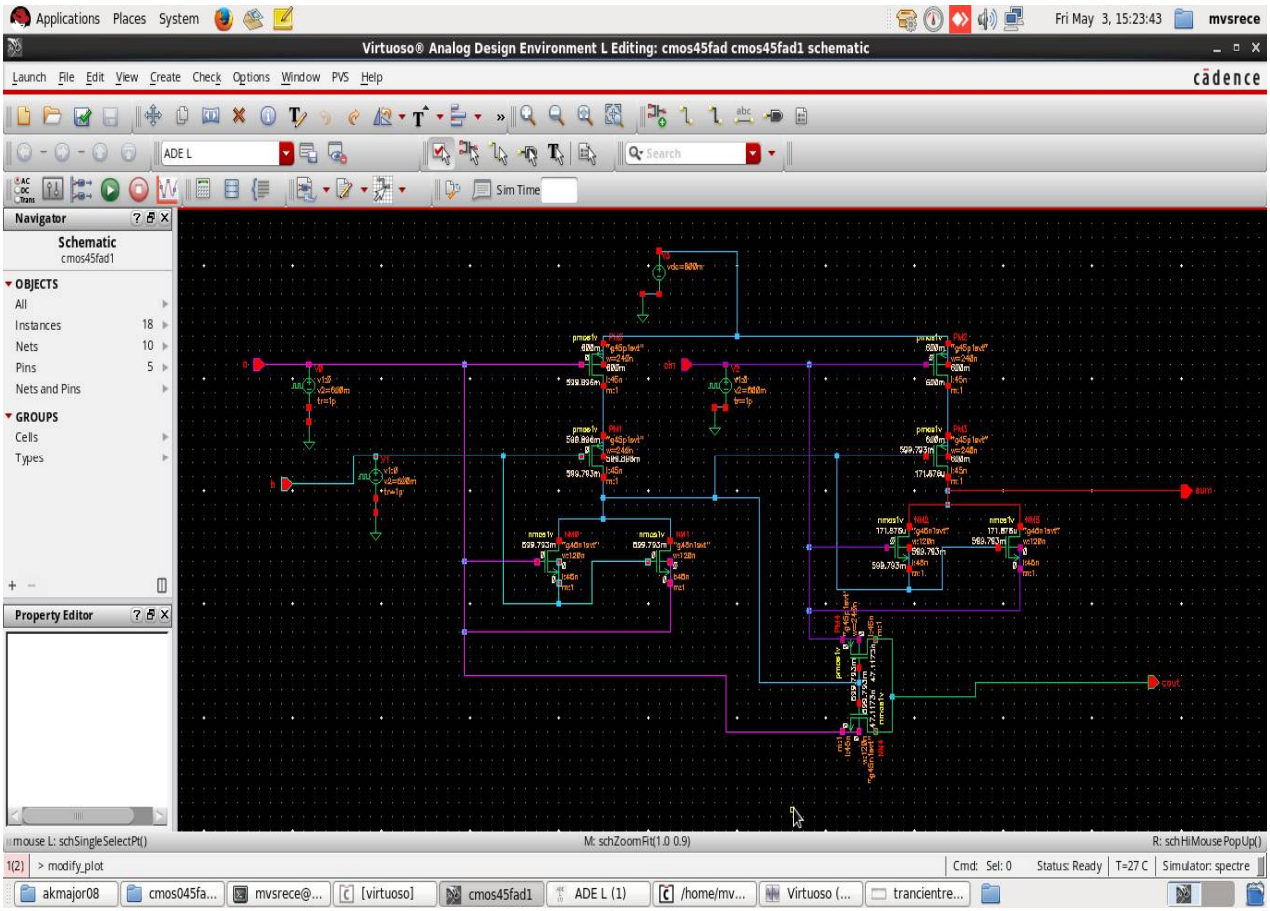

Fig. 3 Schematic of 10T CMOS full adder

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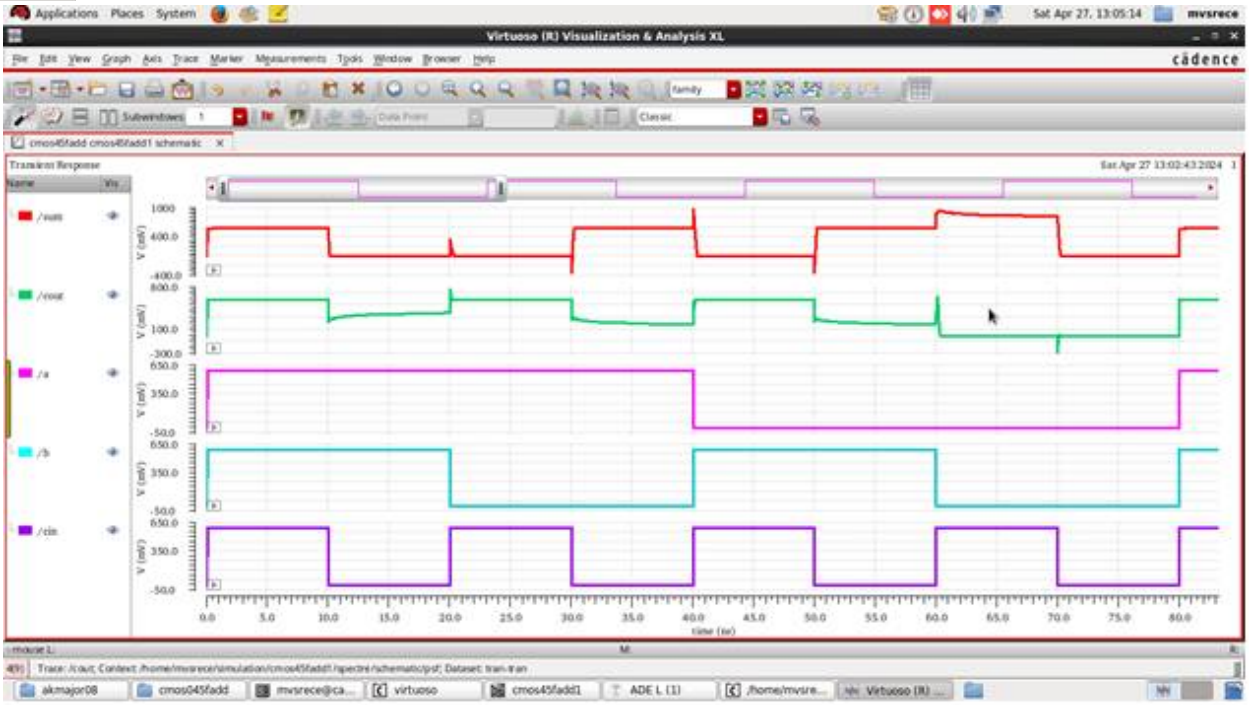

Fig. 4 Output of 10T CMOS full adder

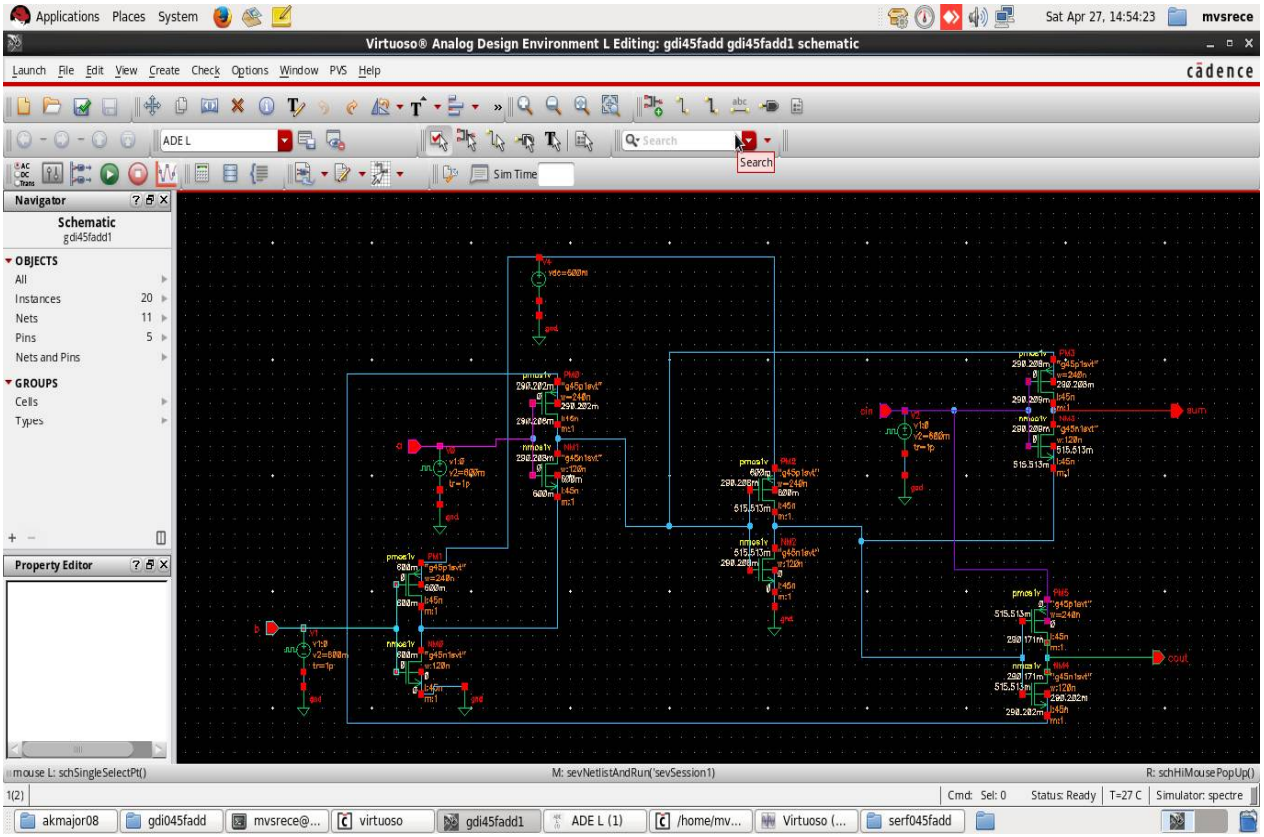

Fig. 5 Schematic of 10T GDI full adder

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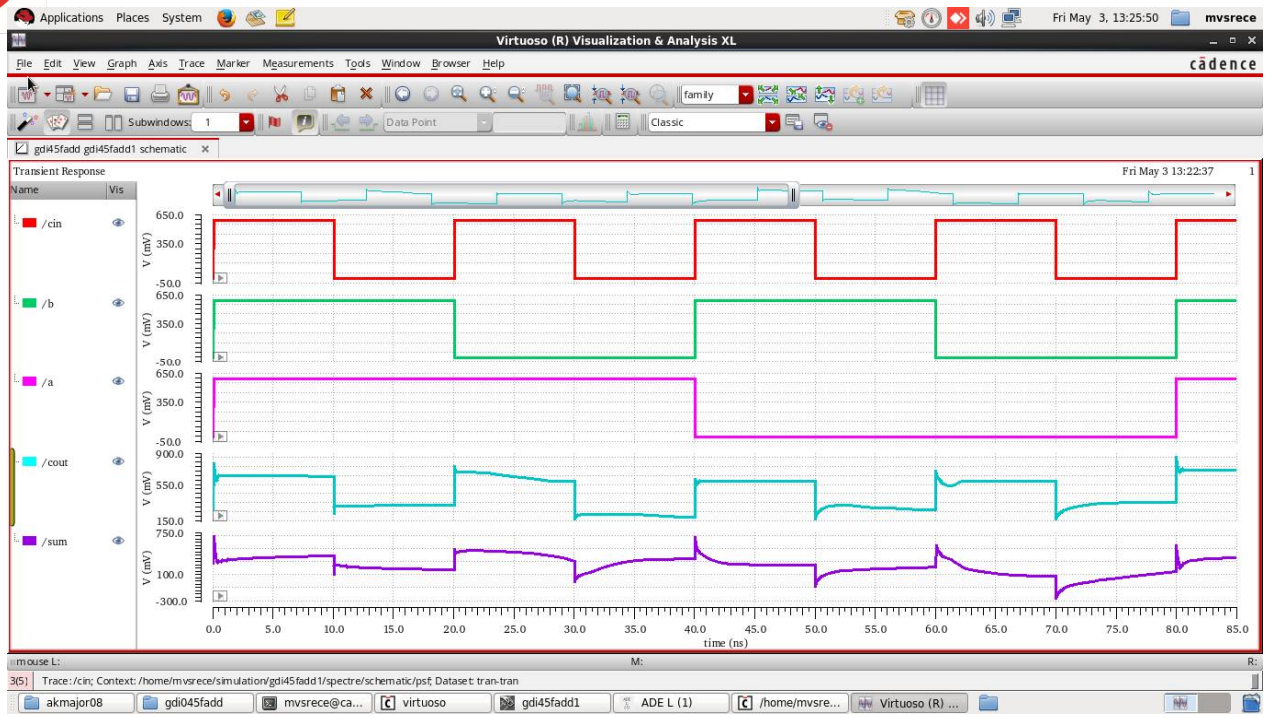


Fig. 6 Output of 10T GDI full adder

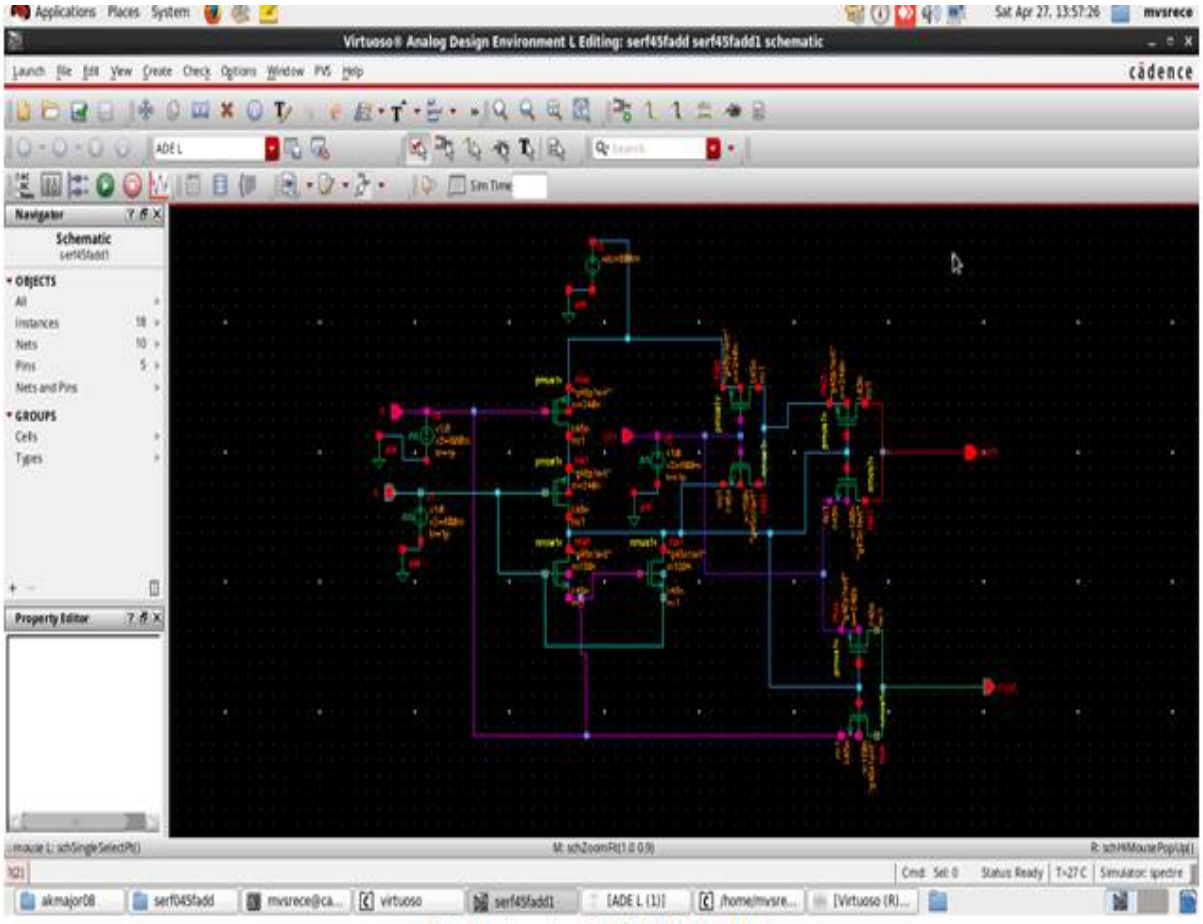


Fig. 7 Schematic of 10T SERF full adder

Fig. 8 Output of 10T SERF full adder

VII. EXPERIMENTAL RESULTS

S.no	Full adders in different techniques	POWER(W)	DELAY(S)	GAIN at 600mv
i	10T CMOS	2.86438n	102.3E-15	0.194
ii	10T GDI	4.86437n	475.9E-15	0.484
iii	10T FinFET	6.683n	398.7E-15	0.00001
iv	10T SERF	12.8942p	19.63E-15	0.0002

VIII. CONCLUSION

We can see from the experimental results the outputs of design parameters of full adders. 10T SERF full adder have low power consumption and low delay so it is used for low power applications. 10T GDI is a high gain full adder with high delay. 10T CMOS full adder is relatively stable with moderate power consumption and low delay with average gain. 10T fin FET full adder uses high power and relatively less delay than GDI.

IX. FUTURE SCOPE

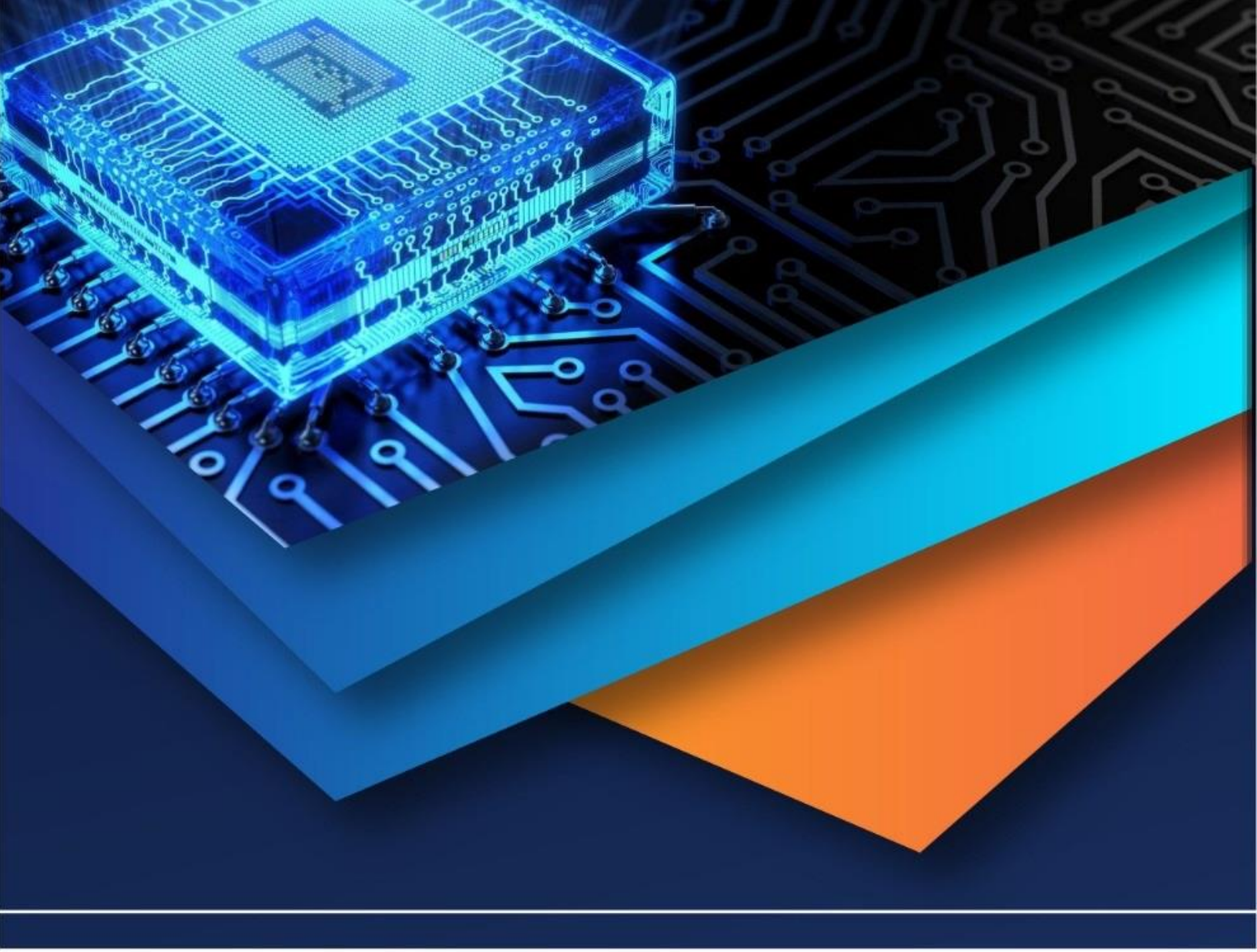
The future scope of full adders, which are fundamental components in digital electronics, is broad and influenced by several emerging technologies and trends in the field of computing and electronics. Here are some key areas where full adders are likely to see significant developments and applications:

1) Energy-efficient and Low-power Designs
2) Neuromorphic Computing
3) Nanoelectronics and Emerging Materials
4) Internet of Things (IoT)
5) Reconfigurable Computing and FPGAs

REFERENCES

[1] Chandran Venkatesan, Thabsera Sulthana Mc, Suriya M and Sumithra M.G," Analysis of 1 – bit full adder using different techniques in Cadence 45nm Technology",2019.
[2] Shrikant M Patar and Ravish Aradhya H V, "Novel low power and High speed 8T full adder," in International Journal of Scientific and Engineering Research, vol.4, Aug. 2016, pp. 1156–1160.
[3] Manjunath K M, Abdul Lateef Haroon P S, Amarappa Pagi, Ulaganathan J, "Analysis of various full-adder circuits in Cadence," International Conference on E merging Research in Electronics, Computer Science and Technology,2015, pp. 90–97.
[4] Ms. Asha K A and Mr. Kunjan, Shinde D, "Analysis, Design and Implementation of full adder for systolic array-based architectures," in IOSR Journal of VLSI and Signal Processing, vol.6, May-Jun. 2016, pp. 73–77.
[5] Dhanunjaya K, Dr. Giri Prasad MN, Dr. Padma Raju K, "Performance analysis of low power full adder cells using 45nmCMOS technology," in International Journal of Microelectronics Engineering (I J M E), vol.1, 2015, pp.35–49.
[6] 2018 4th International Conference on Computing Communication and Automation (ICCCA) ©2018 IEEE "Overview and Comparative Performance Analysis of Various Full Adder Cells in 90 nm Technology".
[7] International Journal of Scientific Research & Engineering Trends Volume 6, Sept-Oct-2020, ISSN (online): 2395-566X. "Performance Analysis of Low Power high Speed 1-Bit CMOS Full Adder Cell "M. Tech. Scholar Ayushi Katiyar, Dr. Bharti Chourasia Department of Electronics and Communication, RKDF IST SRK University, Bhopal, India.
[8] FinFET GDI full adder consists of three input pins and two output pins. Here we are using shorted gate FinFET according to the modes of operation. The supply voltage is taken as 1.2V for "FinFET GDI Adder using cadence Virtuoso tool at 180nm technology". In FinFET GDI Adder multiplexer is taken as selective input.

[9] International Research Journal of Engineering and Technology (IRJET) Volume: 10 Issue: 07 | Jul 2023 www.irjet.net © 2023, IRJET |ISO 9001:2008 Certified Journal | "Design and Analysis Of 64-Bit Adders In Cadence Using Different Logic Families "by Gadamsetty Vyshnavi, Pasupaleti Vijay Krishna.
[10] International Journal of Advanced Research Trends in Engineering and Technology (IJARTET) Issue 23, December 2017 "Design, Analysis and Implementation of various Full Adder using GDI and MGDI Technique "by Ms. Vishalatchi.S, Ms. Dhanam.B, Dr. Ramasamy, KPG Student, Assistant Professor, Principal Department of ECE, PSR Rengasamy College of Engineering for Women, Sivakasi, India.



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