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Performance Analysis of Associate Radix-2, Radix- 4 and Radix-8 based FFT using Folding Technique

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Abstract : ***In recent years, as a result of advancing VLSI technology, Orthogonal Frequency Division Multiplexing (OFDM) has received a great deal of attention and has been adopted in many new generation wideband data communication systems such as IEEE 802.11a, IEEE 802.16e, HiPerLAN/2, Digital Audio/Video Broadcasting (DAB/DVB), and for 4G Radio mobile communications. This is because of its high bandwidth efficiency as the use of orthogonal waveforms with overlapping spectra. The immunity to multipath fading channel and the capability for parallel signal processing make it a promising candidate for the next generation mobile communication systems. The modulation and demodulation of OFDM based communication systems can be efficiently implemented with an FFT and IFFT, which has made the FFT valuable for those communication systems. The complexity of an OFDM system highly depends upon the computation of Fast Fourier Transform (FFT) algorithm. With the advent of new technology in the fields of VLSI and communication, there is also an ever growing demand for high speed processing and low area design. It is also a well-known fact that the multiplier unit forms an integral part of processor design. Due to this regard, high speed multiplier architectures become the need of the day.***

I. INTRODUCTION

A. *Overview*

Mathematical transformations are applied to signals to obtain further information from that signal that is not readily available in the raw signal. Assume a time-domain signal as a raw signal, and a signal that has been "transformed" by any of the available mathematical transformations as a processed signal. There are numbers of transformations that can be applied, among which the Fourier transforms are probably by far the most popular. Fourier transform states that the periodic waveforms can be modeled as the sum of harmonically-related sine waves. The goal of the Fourier Transform is to decompose a cycle of an arbitrary waveform into its sine components. The Inverse Fourier Transform does the reverse operation of Fourier Transform. This means that it transforms a sequence of sine components into a resulting waveform.

B. *Transform*

In 19th century, the French mathematician J. Fourier showed that any periodic function can be expressed as an infinite sum of periodic complex exponential functions. Many years after he had discovered this remarkable property of (periodic) functions, his ideas were generalized to first non-periodic functions, and then periodic or non-periodic discrete time signals. It is after this generalization that it became a very suitable tool for computer calculations. In 1965, a new algorithm called fast Fourier Transform (FFT) was developed and FT became even more popular. Fourier Transform can be calculated as

$$X(f) = \int_{-\infty}^{\infty} x(t).\, e^{-2j\pi ftdt}$$

C. *Butterfly*

With regards to quick Fourier change calculations, a butterfly is a bit of the calculation that joins the consequences of littler discrete Fourier changes (DFTs) into a bigger DFT, or the other way around (separating a bigger DFT into sub changes). The name "butterfly" originates from the state of the information stream outline in the radix-2 case, as portrayed beneath. The soonest event in print of the term is thought to be in a 1969 MIT specialized report. A similar structure can likewise be found in the Viterbi calculation, utilized for finding the no doubt grouping of shrouded states. Most generally, the expression "butterfly" shows up with regards to the Cooley– Tukey FFT calculation, which recursively separates a DFT of composite size n=rm into r littler of changes of size m where r is the "radix" of the change.

D. *Multiplier*

A multiplier is one of the key hardware blocks in most digital signal processing (DSP) systems. Typical DSP applications where a multiplier plays an important role include digital filtering, digital communications and spectral analysis. Many current DSP applications are targeted at portable, battery-operated systems, so that power dissipation becomes one of the primary design constraints. Since multipliers are rather complex circuits and must typically operate at a high system clock rate, reducing the delay of a multiplier is an essential part of satisfying the overall design.

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E. Complex Multiplication

Complex multiplication is consisting of 4 multiplications, 2 adders and 1 subtraction. But in the proposed complex multiplication is consisting of 3 multiplications, 1 adder and 1 subtraction in shown in figure 1.6. The proposed multiplication is consumed delay and area compared to simple complex multiplication.

II. PROPOSED METHODOLOGY

A. Introduction

According to previous design, the use different technique used for Decimation In Time (DIT) and Decimation In Frequency Fast Fourier Transform (DIF-FFT) using pipeline and parallel technique. In proposed methodology generally concentrate on the number of slice (area), number of Look Up Table (LUT) and Maximum Combination Path Delay (MCPD) of the fast fourier transform. In this dissertation proposed folding technique based DIT FFT using reversible gate. The step of proposed design is given below:

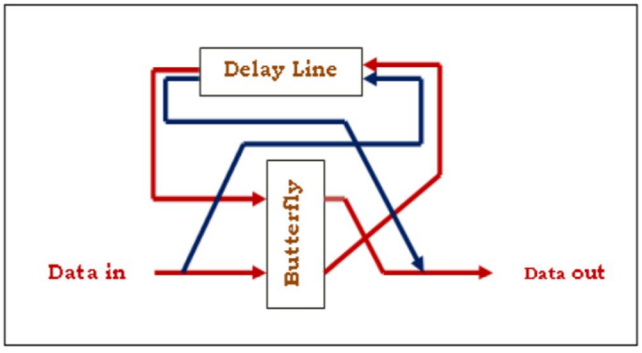
1) Design serial in serial out shift register using delay flip flop.
2) By the help of reversible half adder, full adder, half sub-tractor and full subtractor design N-bit adder and N-bit sub-tractor.
3) Design single path delay feedback pipeline structure.
4) Same block are used to different level folding technique is applied to minimize the delay and area.
5) Output is achieved with minimum delay and less area.

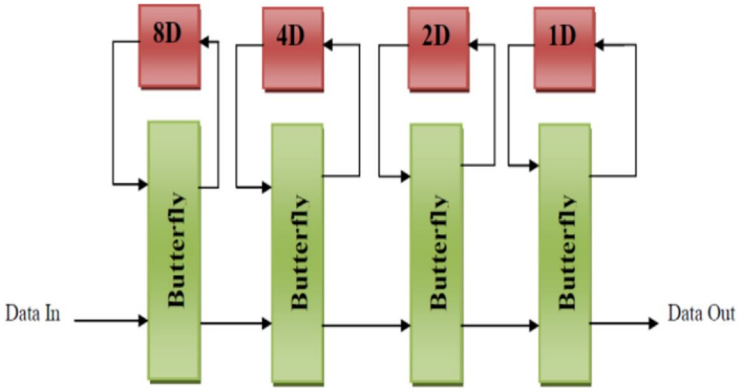
B. Proposed Methodology

The consolidated R2B, R4B & R8B based SDF FFT has been planned in this proposed work. The consolidated Radix of FFT design has a lesser measure of computational way and furthermore improves the exhibitions of FFT processor. SDF design, the info information successions are going through one single way. The butterfly preparing component plays out the calculation on the information. The expansion and deduction activity is done in butterfly components. The changed convey select viper circuit is utilized for snake activity in this engineering. This snake structure is extremely productive in this design. The structure of joined R2B, R4B & R8B FFT is appeared in Figure 4.1. The engineering of 16 point SDF FFT is appeared in Figure 4.2. Figure 4.1 shows the 16 point SDF engineering. The procedural progression of this engineering is as per the following; first and foremost the information with files 0 to 7 is put away in the move register. The R2B components work on this information and the rest of the info information with records 8 to15.

C. SDF

The information successions took care of through one single way postpone input. The butterfly-preparing component plays out the estimations on the information. The defer units are all the more productively used by having a similar stockpiling among info and yield of butterfly unit. Butterfly units and multiplier can be utilized 50% because they are bypassed half the time. SDF FFT is a pipelined based frequency transformation technique. The structure of SDF FFT is just like "stream-like" processing of block-based algorithm. The representation of sequential data flow in SDF FFT





It has single butterfly processor for performing signed addition and signed subtraction function. Single path delay elements have been used in the feedback structure.

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D. 8-Point DIT FFT Algorithm Using RADIX-2 Butterfly

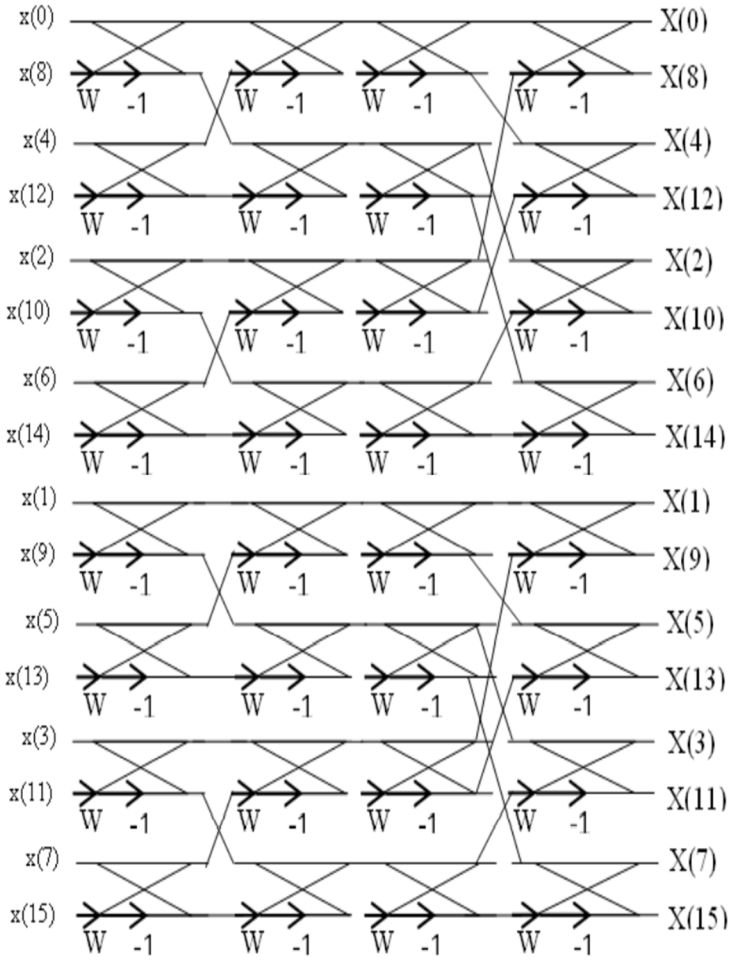
DFT is a most important transform among the transforms that are widely used. The DFT is used to perform the Fourier transform efficiently. The FFT algorithm is the most efficient and most preferred algorithm that is used in DFT computation. The FFT algorithm is preferred the most for DFT computation because of the need of less arithmetic resources when compared to that of the conventional method of DFT computation.

Among various algorithms used in the performance of computation of FFT, CooleyTukey plays a vital role. This algorithm performs its computation by decomposing the transform of size 'N' into 2 equal transforms of size N/r at each phase for a radix-2 computation. When all such small elements are combined together in order to compute FFT then it is known 34 as FFT butterfly unit of 'r' size.

E. 16-Point DIT FFT Algorithm using Radix-2 Butterfly

Figure 4.6, shows the block diagram of 16-point DIT FFT algorithm using radix-2 butterfly algorithm. In these research radix-2 cooley-tukey FFT algorithms is considered due to its divide and conquer strategy. For N-point FFT which is given as 2n-point FFT size and in order to obtain it a Cooley-Turkey algorithm is used. Equation gives a clear mathematical expression for cooley-tukey algorithm based NFFT Radix-r algorithm

Hence for computing N-point FFT using CooleyTurkey algorithm only the obtained results of two 'N/2' transforms which include separate even and odd elements. The proposed 16-point FFT is reduces complexity compared to existing algorithm.



III. IMPLEMENTATION AND SIMULATION RESULT

A. Result Analysis

Each unit presented in this dissertation is functionally verified including radix-2 unsigned 8-point, 16-point and 32-point decimation in time (DIT) algorithm, all conventional weight measurement, multiplexer and encoder and decoder. It has been found that number of slices, number of LUTs and maximum combinational path delay is less compare to conventional algorithm.

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B. Theoretical Result

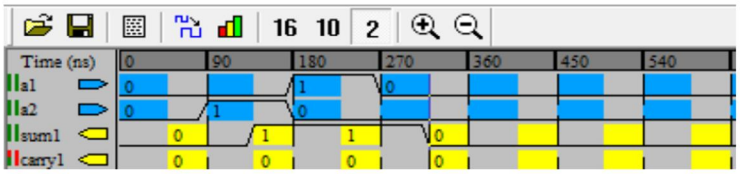
The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter (AOI), each having delay equal to 1 unit and area equal to 1 unit.

Adder Block	Delay	Area
XOR	3	5
2:1 MUX	3	4
Half Adder	3	6
Full Adder	6	13

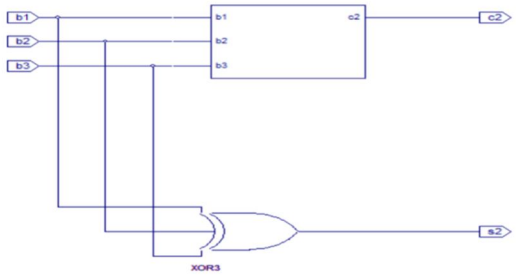
To add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block.

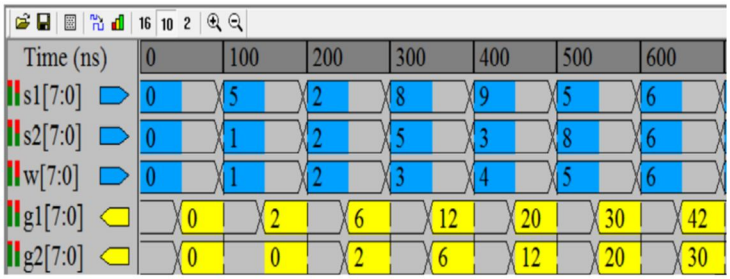
C. Synthesize Result

Half adder is a combinational logic circuit with two inputs (a1, b1) and two outputs (s1, c1). It is a basic building block for addition of two single bit numbers. The addition of three bits is not possible to perform by using a half adder circuit. Therefore, practically we cannot use a half adder. Figure 6.1 and figure 6.2 shows the resistor transfer level (RTL) using half adder and output waveform of half adder respectively.

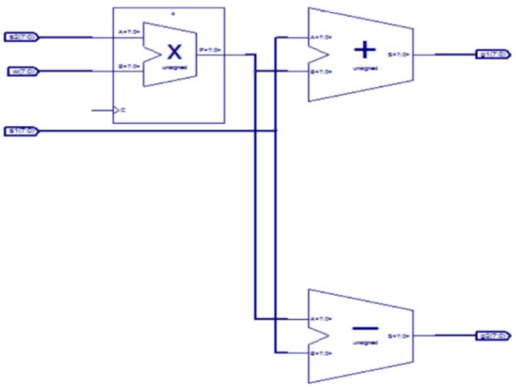


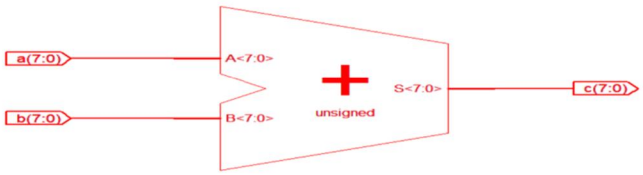
To overcome the drawback of a half adder circuit, 3 single bit adder circuit is developed called full adder. Basically, a full adder is a three input (a2, b2, c2) and two outputs (s2, car) combinational circuits. Figure 6.3 and figure 6.4 shows the resistor transfer level (RTL) using half adder and output waveform of half adder respectively.





Adding unsigned number in binary is quite easy. Recall that with 8-bit number we can represent number from 0 to 255. Addition is done exactly like adding decimal numbers, except that you have only two digits (0 and 1). The number facts to remember are that 0 + 0 = 0, with no carry 1 + 0 = 0, with no carry 0 + 1 = 0, with no carry





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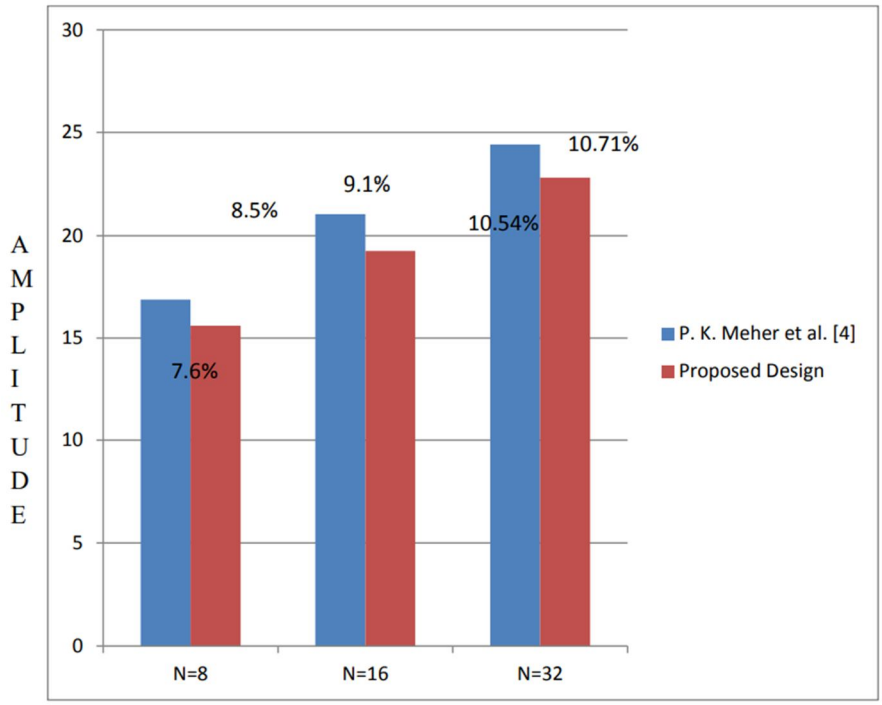
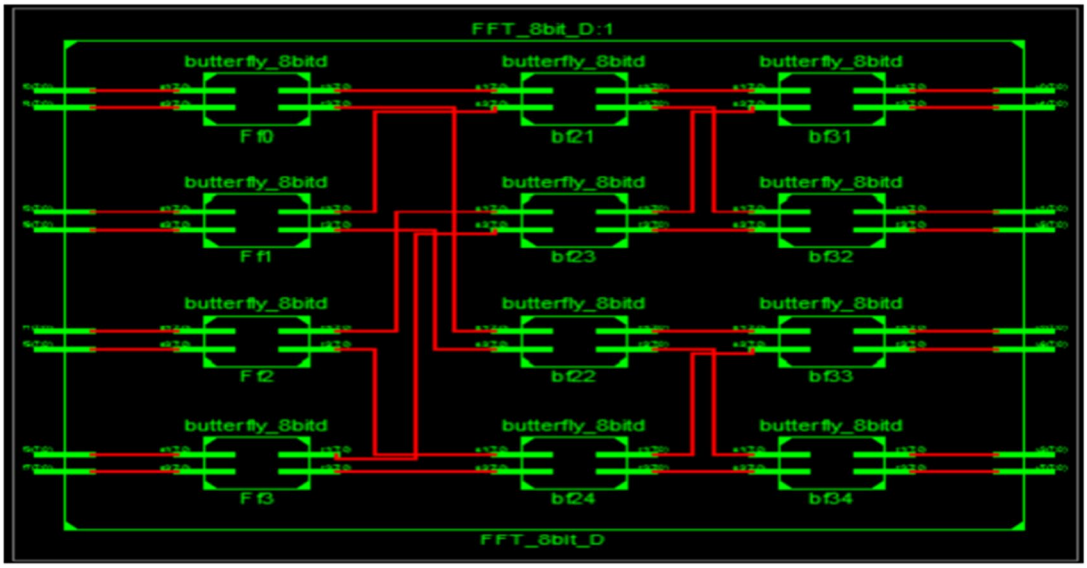
D. Comparision Result

Comparative results of using multiplier add operation (TMA), add multiplier operation (TAM), radix-2 DIT FFT algorithm using eight point, sixteen point, thirty two point, sixty four point and one hundred twenty eight point in terms of area occupied (Number of Slices), delay involved (Maximum Combinational Path Delay), LUT has been shown in table 5.2-5.4 respectively.



E. Combined R2B, R4B & R8B SDF FFT

Table 5.4 shows the results of proposed radix-2 DIT FFT algorithm in different point that can be implemented in the Xilinx 6.2i in term of number of slice, number of look up table (LUT) and maximum combinational path delay (MCPD). The reproduction results for different FFT calculations have been tried basically by executing in the Vertex-4 Xilinx programming. Additionally these product yields can be confirmed with reproduction results got utilizing MODELSIM. A portion of the previews of results in the Xilinx programming and reenactment are as per the following



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Design	N	Slices	LUTs	MCPD (ns)
R_2B SDF FFT	8	145	252	11.378
	16	371	648	12.396
	32	897	1568	13.754
Combined R_2B, R_4B and R_8B based SDF FFT	8	187	336	10.111
	16	514	923	11.425
	32	1158	2069	13.416

Design	N	Q.C for I[st] Stage	Q.C	Power
R_2B SDF FFT	8	P= 208 TR = 208	1248	128.943 mW
	16	P = 416 TR = 416	2496	257.88 mW
	32	P = 832 TR = 832	4992	515.773 mW
Combined R_2B, R_4B and R_8B based SDF FFT	8	D =192	576	59.512 mW
	16	D = 384	1152	119.024 mW
	32	D =768	2304	238.049 mW

IV. CONCLUSION AND FUTURE SCOPE

Implementation of a minimum delay and low area efficient radix-2 DIT FFT algorithm using folding technique are consumed 8.46% computational delay of multadd (DIT) operation,10.46% computation delay of add-mult (DIF) operation for N=16 and consumed 7.95% computation delay of mult-add operation, 6.487% computational delay of add-mult operation. Improved Percentage for base paper is

- 47.91 % power consumption for N=8
- 40.15 % computational delay for N=8

A. Future Scope

The following are the suggestions sorted out for the scope of future study

1) The FFT processor can be extended to have radix-3 and radix-4 algorithm and to improve the requirements of high throughput, consumption of low power and low area.

2) Higher Mixed Radix number or Iterative Radix 2 can be employed to improve the percentage of utilization of hardware.

3) The integration of commutator and feedback architectures can be implemented with the FFT processor for optimum results.

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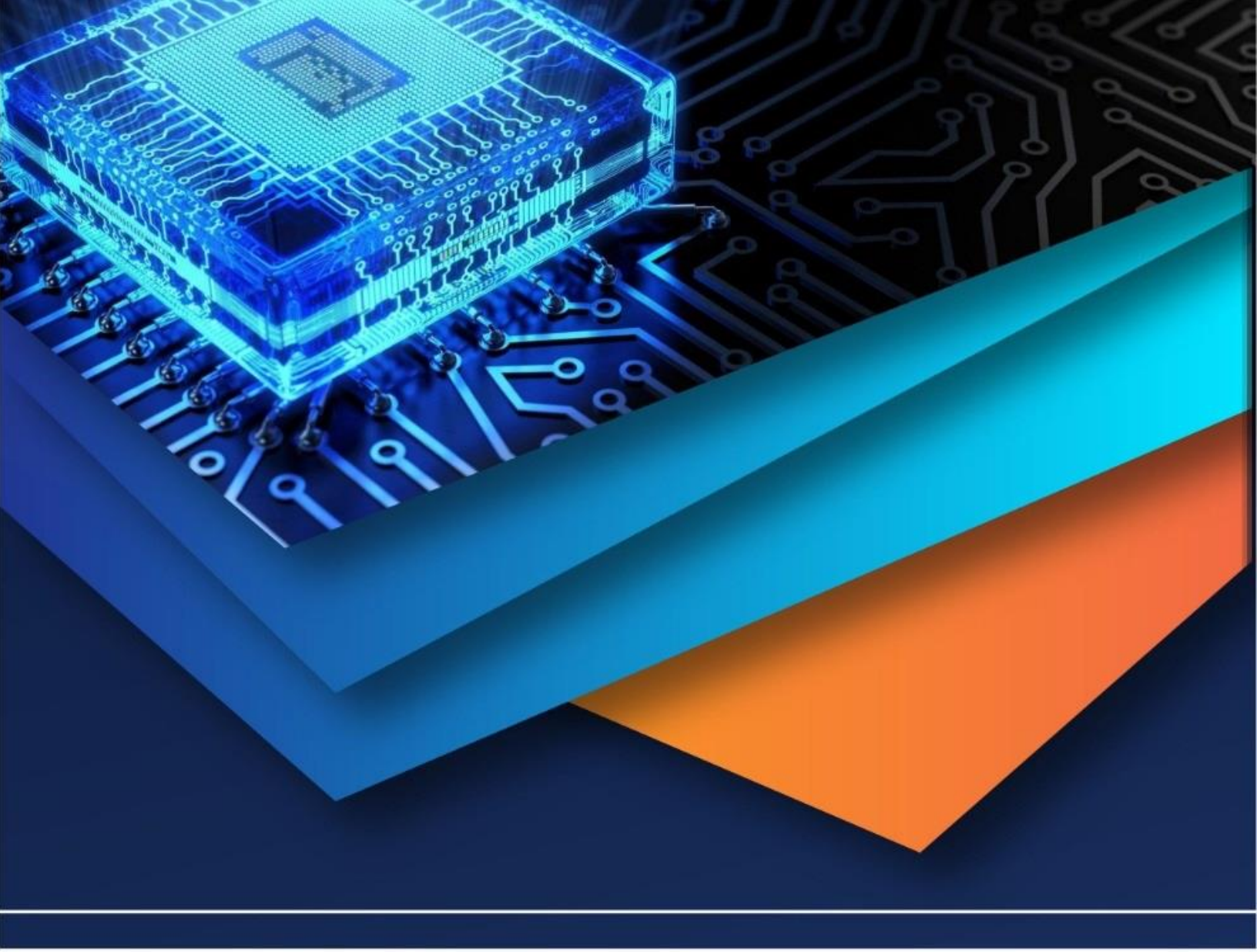

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