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Analysis of Parallel Prefix Adders

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Abstract: ***Parallel prefix adders are essential components of contemporary digital arithmetic circuits and are found in many different devices, including digital signal processors and microprocessors. In order to improve the effectiveness and performance of parallel prefix adders, this research investigates their design and optimization. This paper analyses in detail the state of the parallel prefix adder architectures and provide new designs that minimize power consumption and critical path delays. The speed and area efficiency benefits of the parallel prefix designs with thorough simulations and comparisons is reviewed. This research have ramifications for high-performance computing systems and point to interesting avenues to further the state of the art in parallel prefix adder design.***

Keywords: ***prefix adders, comparison, performance, and delay and power consumption.***

I. INTRODUCTION

The majority of contemporary digital control systems and DSP circuits depend heavily on the fundamental operation of binary addition. Adders come in different varieties, and each has a distinct function and significance [1]. The choice of adder type is contingent upon the intended application [2]. In order to achieve high accuracy and minimal space consumption, adders must be able to compute more quickly. In a digital system, binary adders are among the most important logic components. These impact the design's performance. Aside from Arithmetic Logic Units (ALU), binary adders are also useful in memory addressing units, multipliers, dividers, and other units [3]. Any enhancement to binary addition can boost the performance of any computing device, which in turn enhances the system as a whole. The carry chain is the main disadvantage of binary addition.[2] [3]. The carry chain's length grows in tandem with the width of the input operands. Accelerating the carry chain, but not completely eliminating it, can help the carry-propagate adders perform better. Because they often set the critical path for most computations, most digital designers end up building faster adders by optimizing computer architecture [1]. The primary goal of this paper is to identify an improved adder with respect to cell usage, device utilization, and delay constraints [1] [2].

II. METHODOLOGY

With the rising processing demands of the present generation, DSP is essential. A variety of procedures are carried out in order to create an effective architecture. One of the key components that aid in creating an effective architecture is the adder [4]. The way an architecture is implemented determines how effective it is. In this work, Verilog coding is used for the implementation and analysis of adders [5]. Targeting the Spartan 6 FPGA family, analysis, synthesis, and pre-simulation compilation were carried out using the Xilinx ISE design tool. Fig. 1 displays the block diagram of the high-speed architecture utilizing serial adders and parallel prefix [6]. This picture illustrates the several processes that must be taken in order to calculate assessment parameters like area and delay [8].

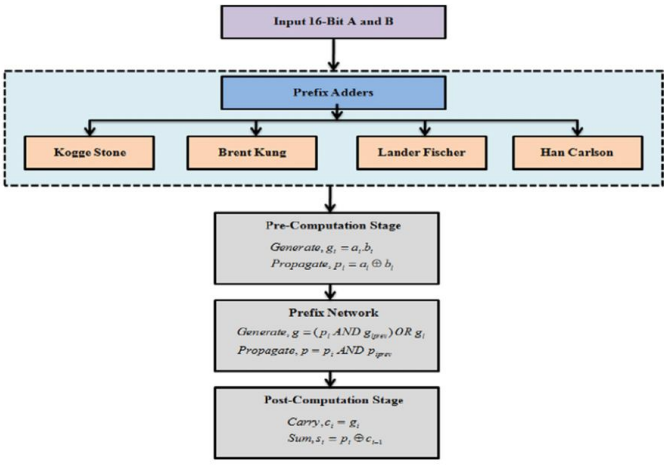


Fig. 1 Block Diagram of Parallel Prefix Adders.[3]

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III. PARALLEL PREFIX ADDERS

These adders determine carriers for several bits at once using a variety of methods, such as the prefix calculation. By anticipating whether a carry will be formed or propagated from each bit addition, the carry lookahead logic lessens the need to compute the current carry by relying on the prior one [4]. Different designs of parallel prefix adders exist, including the Brent-Kung adder, the Kogge-Stone adder, and others. Each has a distinct method for computing the carry signals in parallel with the goal of maximizing performance and minimizing latency in multi-bit addition operations [1][7][2].

A. Stages of Parallel Prefix Adders

The purpose of parallel prefix adders is to calculate the prefix sum of a group of binary values. Usually, they are divided into many stages:

1) *Generation Stage:* In this stage, partial prefix sums are calculated without taking the carry bits into account [4].
2) *Stage of Propagation:* Manages the carry propagation via the adder. The carry bits that must be conveyed to higher order bits are calculated by it [4].
3) *Reduction Stage:* To get the final total, the carry bits are effectively reduced or processed in this last stage [4]. Together, these steps allow for the prefix sum to be computed efficiently, which lowers the critical path time when adding several bits in parallel. Prefix adders come in different designs, such as the Kogge-Stone, Brent-Kung, and Han-Carlson adders, and each one implements these phases in a different method for quicker results [5][6].

B. Types of Parallel Prefix Adders

1) Kogge Stone Adders

Kogge and Stone created KSA, a parallel prefix form of CLA, in 1973[7]. It is often referred to as the faster adder and is used in industries for higher performance arithmetic circuits because it generates a carry in O (logn) time. In the Kingdom of Saudi Arabia, carry is produced more quickly by calculating it concurrently at the risk of an expanded area [10]. Because of its uniform structure, KSA can be readily integrated with current electronic technologies. KSA's minimum fan-out or minimum logic depth is another advantage. KSA consequently developed into a larger but faster adder[11]. The number of stages for the "o" operator, or log2n, is the delay of KSA. The KSA has an area of (n*log2n)-n+1, where n is the number of "o" operators [12][13]. The features of the kogge-Stone adder are:

- Low depth
- High node count (suggests greater area).
- Each node has a minimum fan-out of 1, which suggests faster performance [14][15].

Calculating the propagation and carry generation, there are three phases to it:

- Pre-Processing stage: P = A xor B; G = A and B
- Generation of carry: CP = P(previous) and P; CG= G or (P and G(previous))
- Final processing stage: S = P xor C; C = CG (previous)[16][17].

It is claimed to be a good substitute for high performance applications and is the fastest adder that concentrates on design time. Low propagation delay is frequently the outcome of the Kogge-Stone adder's parallel structure. For applications like high-performance computing, where quick arithmetic operations are crucial, this feature is indispensable.

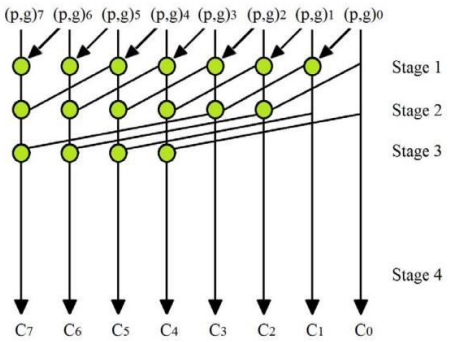


Fig. 2 Kogge Stone Adder Architecture [18].

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2) Brent Kung Adders

A particular kind of parallel prefix adder that is frequently used in digital circuit design for quick binary addition is the Brent-Kung adder [18]. It was first introduced by Tim S. Kung and C. L. Brent in 1982, and it effectively reduces calculation time and critical path latency to overcome the drawbacks of conventional adders. Multiple additions can occur simultaneously because the adder has a tree-like structure in which input bits are separated into groups and carry values are computed in parallel [19]. Because of its ability to provide quicker addition operations, this parallelism is appropriate for highspeed arithmetic applications such as GPUs and CPUs [20]. It is widely utilized in digital circuit design for speedy binary addition. It effectively overcomes the limitations of traditional adders by reducing critical path latency and computation time [21][22].
The extreme boundary case of the following applies to the

Brent-Kung parallel prefix adder:

- Maximum logic depth in PP adders (implies longer calculation time).
- Minimum area implied by minimum number of nodes [23][24].

Three steps make up the computation of carry generation and propagation:

- Preprocessing stage :P=A xor B; G=A and B
- Generation of carry: CP=P and p(previous); CG= G and P and p(previous)
- Final processing stage: Sum=CP; Carry=CG [25].

The Brent Kung Adder is best for area and power performance [26].

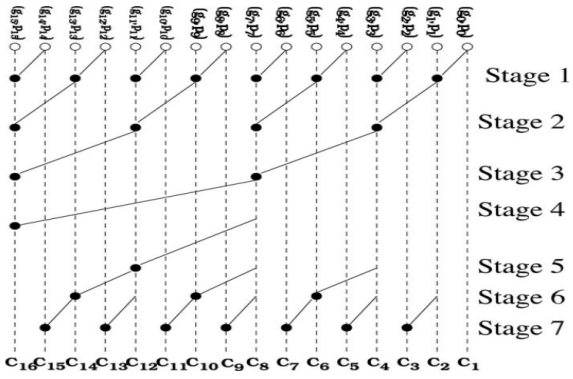


Fig. 3 Brent Kung Adder Architecture [25]

3) Ladner Fischer Adder

The Ladner-Fischer (LFA) trees comprise a family of networks that spans from Brent-Kung to Sklansky. calculates the prefixes for the odd-numbered bits and then ripples into the even positions one more time. Ladner and Fischer (1980) [28] suggest a general technique to build a prefix network with a marginally deeper depth when compared to Sklansky topology [29]. By using this technique, the critical path's maximum fan-out for computation nodes is decreased. Here is the number of computational nodes: [n 2 (log2(n))] [30]. The LFA has carry operator nodes with less logic depth and high fan-out.

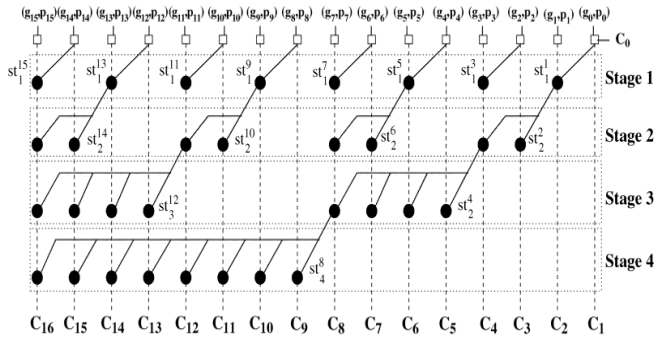


Fig. 3 Ladner Fischer Adder Architecture [31].

4) Skalnsky Adder

Another name for the Sklansky adder is the "divide-and-conquer tree." Sklansky (1960) proposed conditional sum addition logic for prefix addition, which provides a minimum depth prefix network at the expense of increased fan-out for some computation nodes[32]. The nodes connected to $n/2$ other nodes are served by the longest lateral fanning wires[33]. Large amounts of latency are caused by the Sklansky's adder's fan-out, which increases dramatically from inputs to outputs along the critical path. When the adder's bit count rises, this causes the structure to perform less well[34]. Compared to certain alternative adder architectures, Sklansky adders can be made to be more area-efficient. This is significant for integrated circuits since, in many cases, minimizing physical area is an essential design factor.

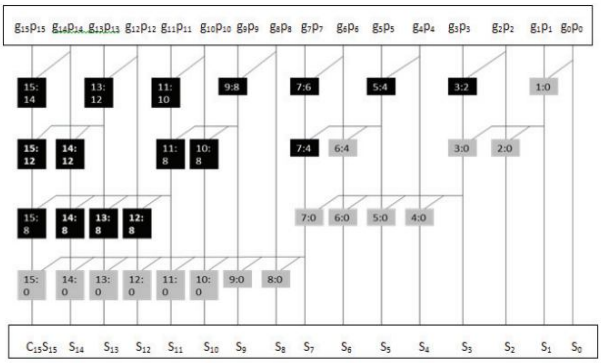


Fig 4. Sklansky Adder Architecture [10].

IV. APPLICATIONS

Parallel prefix adders, often referred to as carry-select adders or prefix adders, are vital parts of digital circuit design and are used in a wide range of industries [35]. These adders are especially helpful in situations requiring high-speed arithmetic operations as they are made to efficiently complete binary addition operations. Digital circuit design uses parallel prefix adders, often referred to as carry-lookahead adders, extensively [36].

Both speed and efficiency are major benefits of these specialized adders. They are mostly used in the core of processors, where they improve the efficiency of the arithmetic units of digital signal processors and microprocessors [37]. These processors' high-speed addition operations—which are necessary for a variety of arithmetic and logic operations—are dependent on parallel prefix adders. Furthermore, they are essential to digital signal processing because they enable faster addition and multiplication operations for real-time signal processing, including the processing of audio and images [38]. Additionally, cryptographic systems make use of their quick modular arithmetic skills to provide strong data security. Parallel prefix adders are utilized by network switches and routers. Parallel prefix adders are also used in error correction codes in memory systems to ensure data integrity, and they are also used in network routers and switches for quick packet routing and switching [39]. They are an essential part of many applications needing high-speed arithmetic operations, and their effect can be seen in digital filters, graphics processing units, high-performance computing, image and video compression, and even FPGA and ASIC designs [40][41]. The core of contemporary digital systems is parallel prefix adders, which maximize performance in a variety of application [42].

V. CONCLUSION

Due to their logarithmic delay, parallel-prefix structures have been found to be appealing for adders. The path for Adders Design's quicker development has been cleared by this project analysis. Our only goal was to identify which of the many binary and PPA types previously discussed was the fastest adder. The results demonstrated that, when the lower bits are considered, there is almost no difference in delays; however, when the number of bits is increased, there is a noticeable difference in delays. Once more, the area used will increase with the number of LUTs used. The findings imply that no one architecture type is optimal for all bit values; rather, they provide sufficient information to determine which kind of adders is most effective for a given bit value. Bold fonts are used to highlight the comparison view's best numbers. In terms of the future, we can go into more detail about other crucial design factors like area, power, energy, and comparability. In order to optimize tree-based adder designs for place and routing, it would be beneficial for future FPG A designs to incorporate an optimized carry path.

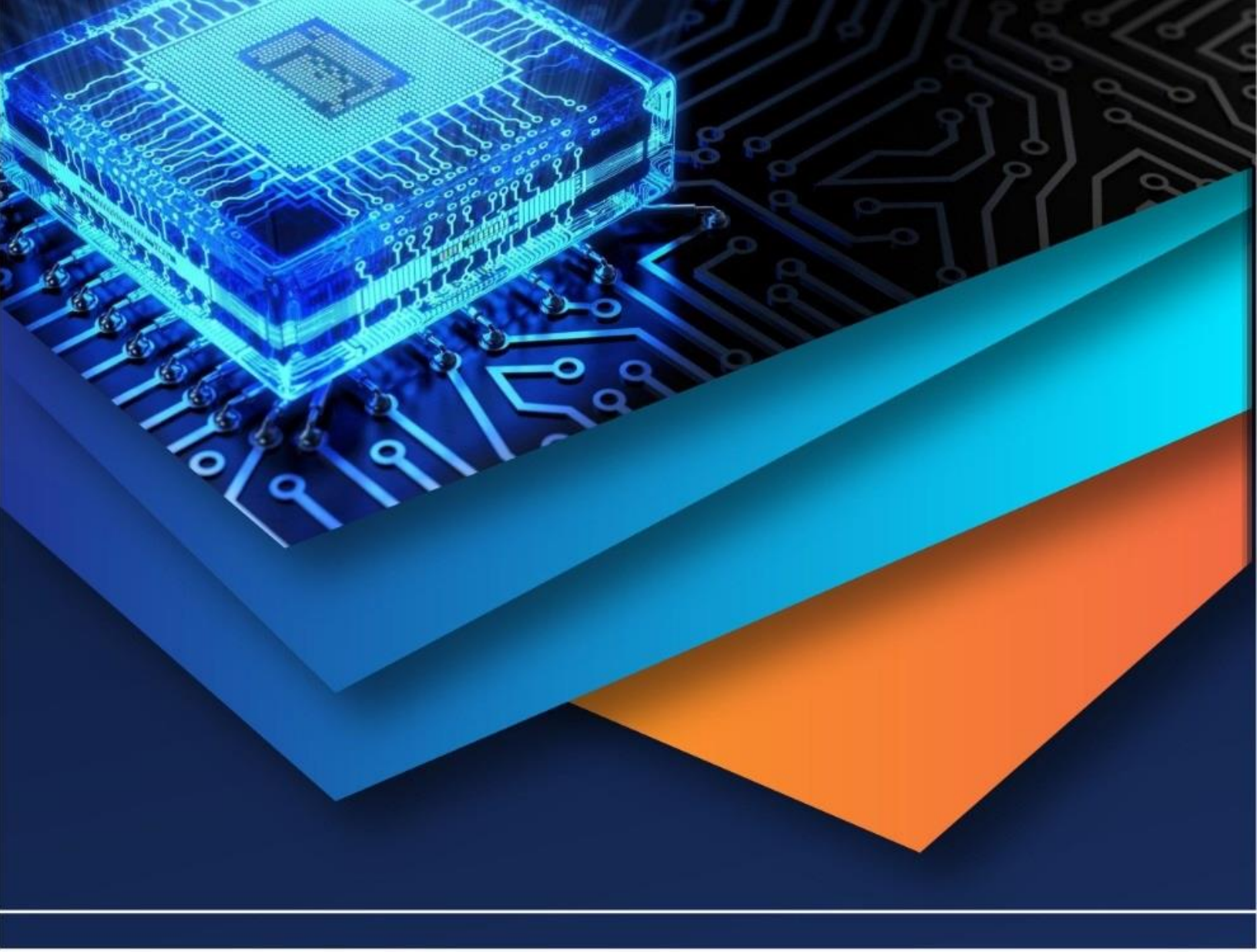
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