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ASIC Design and Implementation of Automated Coffee and Tea Brewing System with FPGA Validation

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Abstract: This paper presents a pioneering approach to enhance the efficiency of automated coffee and tea brewing systems through the integration of an ASIC-GDSII and FPGA validation. Leveraging the power of 45nm CMOS Technology, the design achieves substantial reductions in area, power consumption, and delay. The Verilog HDL code undergoes meticulous verification using Cadence tools like Genus and Innovus, ensuring optimal design performance. Innovus validates timing constraints, ensuring adherence to acceptable delay parameters. The resulting compact design not only minimizes power consumption but also effectively addresses leakage issues. These comprehensive optimizations meet stringent performance, area, and power requirements, elevating the operational efficiency of automated brewing systems. Furthermore, the control algorithm is synthesized and implemented using Xilinx's ISE Design Suite, followed by validation on SPARTAN 6 FPGA, providing invaluable insights for future synthesis and implementation endeavors. Keywords: ASIC, FPGA, CMOS Technology, GDS II, Verilog HDL.

I. INTRODUCTION

The passage provided outlines the significance of automated machines, particularly focusing on coffee machines, in revolutionizing daily life through time-saving, convenience-enhancing, and quality-improving features. It highlights the necessity for coffee machines to adapt to evolving preferences, necessitating upgrades in their functionality and capabilities.

Recent advancements in programmable logic, specifically FPGA (Field-Programmable Gate Array) and CPLD (Complex Programmable Logic Device), are acknowledged for their role in streamlining device development processes. These programmable matrices offer rapid customization options, optimizing both the development and implementation phases. They allow for flexibility in design and troubleshooting while reducing complexity and time requirements[I][III].

Moreover, the introduction of ASIC (Application-Specific Integrated Circuit) level chips is noted for their contribution to enhancing efficiency in automated machines. ASICs have significantly reduced area, power consumption, and delay parameters, thereby improving overall system performance.

The paper proposes the development of a control algorithm for automated coffee machines, utilizing Verilog HDL (Hardware Description Language) within CADENCE Tool Suite and Xilinx's ISE Design Suite. This approach is chosen for its simplicity, cost-effectiveness, and effectiveness in managing synthesis processes. By implementing the control algorithm in Verilog HDL, the coffee machine's functionality can be seamlessly upgraded to meet changing customer demands [II][IV].

The current development plan suggests the incorporation of six modes for each beverage using parallel control. This strategy ensures enhanced functionality and versatility in the automated coffee machine, allowing users to select from a variety of options to suit their preferences[V][VI][X].

The aims of this paper are as follows: designing the operational features of an Automatic Coffee machine utilizing Verilog HDL programming language, validating its functionality via NC Launch ISIM Simulator with the Cadence tool, assessing the Pre-Synthesis and Post-Synthesis stages of the design using the Genus Tool within Cadence, transforming the RTL (Register Transfer Level) code into GDS (Graphic Data System) format through the INNOVUS Tool within Cadence, optimizing the design's Area, Power, and Delay, and finally, validating the design on Spartan 6 FPGA.

Thus, the paper's main goal is to introduce a strong control method for automatic coffee machines. It uses new technology in computer chips to make a coffee machine that's both affordable and can adapt to what customers want.



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II. METHODOLOGY

The block diagram illustrates the menu selection of an automated coffee and Tea Brewing system, as depicted in Figure 1. This system offers six modes of operation, each catering to different preferences:

- Milk.
- Espresso.
- Cappuccino.
- Americano.
- Tea.
- Lemon Tea.

Each mode triggers a specific sequence of processes based on the selected program. These operation involved in preparing the various menu options in the automated coffee dispenser:

- 1) Milk:
- Cup: Place a Cup.
- Milk: Dispenses Milk into the cup.
- Sugar: Adds sugar.
- Stirrer: Mixes the contents thoroughly.
- Finish: Ready to serve.
- 2) Espresso:
 - Cup: Place a Cup.
 - Coffee: Dispenses Coffee Powder.
 - Water: Adds water.
 - Sugar: Adds sugar.
 - Stirrer: Mixes the contents thoroughly.
 - Finish: Ready to serve.

3) Cappuccino:

- Cup: Place a Cup
- Coffee: Dispense Coffee Powder into the cup.
- Milk: Adds milk.
- Sugar: Adds Sugar.
- Stir: Mixes the ingredients.
- Finish: Ready to serve.
- 4) Americano:
 - Cup: Place a cup.
 - Coffee: Dispense coffee into the cup.
 - Water: Dispense hot water twice.
 - Sugar: Adds sugar.
 - Stirrer: Mixes the contents thoroughly.
 - Finish: Ready to serve.
- 5) Tea:
 - Cup: Place a cup.
 - Tea Leaves & Spices: Dispense tea ingredients.
 - Water: Adds water.
 - Sugar: Adds sugar.
 - Stirrer: Mixes the contents thoroughly.
 - Finish: Ready to serve.



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- 6) Lemon Tea:
 - Cup: Place a cup.
 - Tea Leaves: Dispense tea leaves.
 - Lemon Syrup: Add lemon syrup.
 - Water: Add water.
 - Sugar: Add sugar.
 - Stir: Mixes the contents thoroughly.
 - Finish: Ready to serve.

Each operation is essential in preparing the desired beverage, ensuring accurate ingredient dispensing, mixing, and customization according to user preference



Fig. 1. Block Diagram of the Automated Coffee and Tea Brewing system.

III. IMPLEMENTATION

Each individual process activates a corresponding timer, which is considered in the development of the control program. Importantly, each program operates independently from others, and if a program is not needed, it can be removed from the selection. In this paper, we have several parameters to consider. The Input Parameters are: rst, clk and mode select. The Output Parameters are: Milk, Espresso, Cappuccino, Americano, Tea and Lemon Tea.

The implementation of an automated coffee and tea brewing system using FPGA involves a meticulous series of steps. First, we use Verilog HDL to encode the core functionality of the coffee machine. Through comprehensive simulation using the NC Launch ISIM Simulator with the Cadence tool, we rigorously validate the behavior of the system.

Moving forward, the design undergoes scrutiny in both the Pre-Synthesis and Post-Synthesis stages using the Genus Tool within Cadence. This ensures that the RTL code is refined and optimized for subsequent stages. The transformation of the RTL code into GDS format is achieved through the INNOVUS Tool, ensuring compatibility and readiness for FPGA deployment.

During this transformation, we focus on optimizing key metrics such as Area, Power, and Delay to enhance overall efficiency and performance. Finally, we port the design onto a Spartan 6 FPGA for real-world validation, ensuring seamless integration and functionality within the physical hardware environment. Through this comprehensive process, the automated coffee and tea brewing system is meticulously crafted and validated for optimal performance and reliability.

For example, for "cappuccino" there are 6 states:



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Fig. 2. FSM of the Cappuccino Menu.

- S0 Initial State
- S1 Placing cup
- S2 Adding coffee powder
- S3 Adding milk
- S4 Adding sugar
- S5 Stirring
- S6 Finish

The paper work incorporates a Finite State Machine (FSM) for one menu i.e., Cappuccino Menu where 'S0' serves as the initial state, common to all other states. This state acts as the starting point for all modes of flavors. As the system progresses through different states based on user selections, it ultimately reaches a final state. Upon reaching this final state, the system transitions back to the initial state ('S0'), where it awaits the next user selection. This cyclic behavior ensures the readiness of the system to accept and process subsequent requests, maintaining a seamless and efficient operation of the automated coffee and tea brewing system.

After selecting the menu option 'S0,' which is the same for all menu options, the FSM will first place the cup, then pour milk. Since it is cappuccino with sugar, sugar is also added. After that, in state 4, stirring happens. Finally, in state 5, the process is finished, and the FSM returns to the initial state.



Fig.3. Simulation Waveform on Cadence NC Launch Sim Tool.

The Automated Coffee and Tea Brewing System was created using Verilog. This design code was subsequently synthesized and simulated using NC Launch Simulator Tool in Cadence to generate waveforms, as shown in Fig. 3. The waveforms clearly demonstrate that each state transitions in accordance with the designed Finite State Machine (FSM) and adheres to precise timing definition.



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Generated by:	Genus(TM) Synthesis Solution 17.22-s017_1						
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Module:	coffee_making						
Technology libraries:	slow						
Operating conditions:	slow (balanced_tree)						
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(D) = wireload is default in technology library

Fig. 4. Genus Tool Area Report Analysis.

The coffee_making module, generated by Genus Synthesis Solution in Fig. 4., has a total area of 2826.265 square units.

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The coffee_making module, generated by Genus Synthesis Solution in Fig. 5., has a total Power of 2.09mW.

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Fig6. Genus Tool Timing REport Analysis.

The coffee_making module, generated by Genus Synthesis Solution in Fig. 5., has a slack of -453ns, input delay of 700ns, data path of 613ns and required time of 860ns.

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The coffee_making module, generated by Innovus Tool in Fig. 6., has a total area of 1013.57 square units.

Total Power						
Total Internal Power: Total Switching Power: Total Leakage Power: Total Power:		.60552531 .12037416 .00004550 .72594496	83 16 0	83,4120% 16,5817% 0.0063%		
Group		Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential Macro IO Combinational Clock (Combinational) Clock (Sequential)		0.4714 0 0.1341 0 0	0.03203 0 0.08835 0 0	1.613e-05 0 2.937e-05 0 0	0.5034 0 0.2225 0 0	69.35 0 30.65 0
Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
VDD	1.08	0.6055	0.1204	4.55e-05	0.7259	100

Fig. 7. INNOVUS Tool Area Report Analysis.

The coffee_making module, generated by Innovus Tool in Fig. 7., has a Total Power of 0.729W, Leakage Power of 4.55*10^5 W.

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# 0S:	Linux x86	64(Host	ID cad08)				
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Path 1: VIOLATED	Recovery Check	with Pin	coffee_	reg/CK				
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Beginpoint: rst	(v) t	riggered	by lead:	ing edge of	f 'clk'			
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Other End Arrival	Time	0.000						
 Recovery 		0.671						
+ Phase Shift		1.000						
= Required Time		0.329						
 Arrival Time 		1.773						
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Clock Rise E	dge		0.000					
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9/656		TNVXL	1.003	1.703	0.319			
Corree_reg		DFFRAZ	0.010	1.773	0.329			

Fig. 8. INNOVUS Tool Timing Report Analysis.

The coffee_making module, generated by Innovus Tool in Fig. 8., has a slack of -1.433ns and required time of 0.329ns.







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From Fig.9. The RTL schematic we've obtained from the Cadence Genus tool for our automated coffee and tea brewing system is a critical component of our project's development. This schematic serves as the blueprint for the system's digital logic, outlining the sequence of operations and control flow required to automate the brewing process. Through the Genus tool, we've meticulously designed and optimized the RTL (Register Transfer Level) representation, ensuring that it accurately captures the functionality and behavior of our brewing system. This RTL schematic lays the foundation for further design and implementation stages, guiding the development of our system towards efficient and reliable operation. Overall, it represents a significant milestone in our journey towards realizing a fully automated and efficient coffee and tea brewing solution

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Fig. 10. GDS II File of the Automated Coffee and Tea Brewing system.

From Fig. 10. The ASIC design layout we've obtained from the Cadence Innovus tool for our automated coffee and tea brewing system marks a crucial milestone in our project. This layout essentially represents the physical blueprint of our system's integrated circuits, meticulously crafted to ensure efficiency, performance, and reliability. Through careful optimization processes, we've managed to condense the layout while maximizing its functionality, allowing us to meet stringent requirements within limited space. Extensive testing and validation have been conducted to ensure that the layout aligns with our system's functional needs and industry standards, guaranteeing its reliability during operation. Overall, this ASIC design layout signifies a significant step forward in bringing our vision of an advanced and efficient brewing system to life.



Fig. 11. Physical Design of the Automated Coffee and Tea Brewing system.

From Fig. 11. The GDS II file we've obtained from the Cadence Innovus tool for our automated coffee and tea brewing system is a crucial step forward in our project's progress. This file represents the final layout of our system's integrated circuits, translated into a format compatible with manufacturing processes. Through meticulous design and optimization within Innovus, we've ensured that the layout meets stringent requirements for efficiency, performance, and reliability. The GDS II file encapsulates the intricate placement and routing of transistors, capacitors, and other components, optimizing their arrangement to maximize functionality within limited space. This milestone signifies a significant achievement in our journey towards realizing a fully functional and efficient brewing system, bringing us one step closer to delivering an innovative solution for automated coffee and tea preparation.



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Fig. 12. Validation Using Sparten-6 FPGA Board.

V. CONCLUSION AND FUTURE SCOPE.

The Coffee and Tea Brewing System has been effectively crafted, synthesized, and realized using CADENCE Tool, marking a significant achievement in its development. Validation of this system has been successfully conducted using XILINX ISE 14.7 on a SPARTAN-6 FPGA kit, allowing for comprehensive observation of parameters from both technologies. The ASIC design showcases remarkable efficiency, boasting minimal power consumption of 0.7259mW Watts and impressively low delay time of 1.733us and Area of 1013.57um^2.

Consequently, this solution presents the opportunity for integration with Embedded Systems, paving the way for the creation of a marketable smart Maker with enhanced capabilities.

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