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ASIC Implementation of Low Power Cordiac Processor for Modulation and Demodulation

Roselin[1], Madhuri Vemuluri[2]
[1]*M-Tech Scholar department of Electronics and Communication Engineering, Newtons Institute of Engineering, Macherla-Andrapradesh, India*
[2]*Associate professor department of Electronics and Communication Engineering, Newtons Institute of Engineering, Macherla-Andrapradesh, India*

Abstract: ***The ongoing evolution of high-speed communication systems, particularly with the advent of 5G technology, necessitates the development of efficient hardware solutions capable of handling complex modulation and demodulation tasks while adhering to stringent power constraints. This thesis presents a comprehensive approach to designing a low-power Coordinate Rotation Digital Computer (CORDIC) processor specifically tailored for 5G applications. By harnessing the multiplier-free architecture of the CORDIC algorithm, the proposed processor significantly reduces hardware complexity and power consumption, making it ideal for energy-constrained environments such as mobile devices and small-cell base stations. The implementation utilizes advanced techniques such as pipelining, fixed- point arithmetic, and dynamic voltage scaling to optimize performance metrics including area, power, and timing. Utilizing the Cadence Genus synthesis tool, the results demonstrate that the CORDIC processor occupies an area of approximately 2177.856 units, with a total of 780 standard cells, while effectively managing power consumption at an optimal level relevant for 5G applications. Detailed synthesis and validation processes further ensure compliance with industry standards for error vector magnitude (EVM), establishing the processor's reliability for high-order Quadrature Amplitude Modulation (QAM) schemes. Timing analyses indicate that the design meets stringent latency requirements essential for real-time signal processing. Through rigorous testing and analysis, this research not only demonstrates the processor's capabilities but also highlights its versatility across a broad spectrum of digital signal processing applications. The findings underscore the CORDIC processor's potential as a foundational component in the next generation of energy-efficient communication systems, paving the way for innovations that enhance throughput, reduce latency, and improve overall system reliability. As the demand for smart communication technologies escalates, the insights derived from this study will contribute significantly to the ongoing development of energy-efficient accelerators that meet the computational challenges posed by future wireless standards.***

Keywords: Coordinate Rotation Digital Computer (CORDIC), 5G applications, Cadence Genus synthesis tool, Energy-efficient accelerators

I. INTRODUCTIONS

The growing demand for high-speed, low-latency 5G communication systems has intensified the need for efficient hardware solutions to handle complex modulation and demodulation tasks. Traditional digital signal processing methods often rely on power-hungry multipliers, making them unsuitable for energy-constrained applications. The Coordinate Rotation Digital Computer (CORDIC) algorithm offers a compelling alternative by enabling trigonometric calculations using only shift-and-add operations, significantly reducing hardware complexity and power consumption. Implementing CORDIC in Application-Specific Integrated Circuits (ASICs) presents a promising approach to meet the stringent performance and efficiency requirements of modern 5G systems.

Modulation and demodulation are critical processes in 5G communication, involving the translation of data into high-frequency carrier signals and vice versa. Conventional techniques, such as direct digital synthesis (DDS) or lookup table (LUT)-based methods, often suffer from high power dissipation and area overhead, particularly for high-order modulation schemes like 64-QAM and 256-QAM. A low-power CORDIC processor addresses these challenges by eliminating the need for multipliers and leveraging iterative approximations to achieve precise phase and amplitude adjustments. This makes it particularly suitable for deployment in 5G base stations, small cells, and IoT devices, where energy efficiency is paramount.

This work focuses on the ASIC implementation of a power-optimized CORDIC processor tailored for 5G modulation and demodulation. By combining pipelined architecture, fixed- point arithmetic, and advanced low-power design techniques, the proposed solution aims to deliver high throughput while minimizing energy consumption.

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The design is validated through rigorous simulation and hardware testing, ensuring compliance with 5G standards. The outcomes of this research are expected to contribute to the development of next- generation wireless communication systems, offering a scalable and efficient alternative to conventional signal processing methods.

A. Objectives of the work

The increasing demand for high-speed wireless communication in 5G networks has intensified the need for efficient digital signal processing solutions. Among these, the Coordinate Rotation Digital Computer (CORDIC) algorithm has emerged as a critical component due to its multiplier-free architecture, making it ideal for power-constrained applications. This project focuses on the design and optimization of a low-power CORDIC processor for 5G modulation and demodulation, addressing key challenges in computational accuracy, energy efficiency, and real-time processing. The implementation targets ASIC technology to achieve superior performance compared to traditional DSP-based approaches while meeting stringent 5G requirements for throughput and reliability.

- Design a hardware-efficient CORDIC algorithm to perform accurate phase rotations for I/Q components using only shift-and-add operations.
- To verify the functional verification of CORDIC processor through nclaunch simulator.
- To synthesize the complete hardware procession using Genus tool and generate the optimized area, power, timing reports.
- To implement the physical layout of the design with optimization using Innovus tool.

II. METHODOLOGY OF THE WORK

The design and synthesis of an optimized CORDIC processor involves a structured approach comprising architectural planning, behavioural modeling, RTL implementation, functional simulation, and synthesis using industry-standard EDA tools. The methodology adopted for this project is outlined in the following key phases:

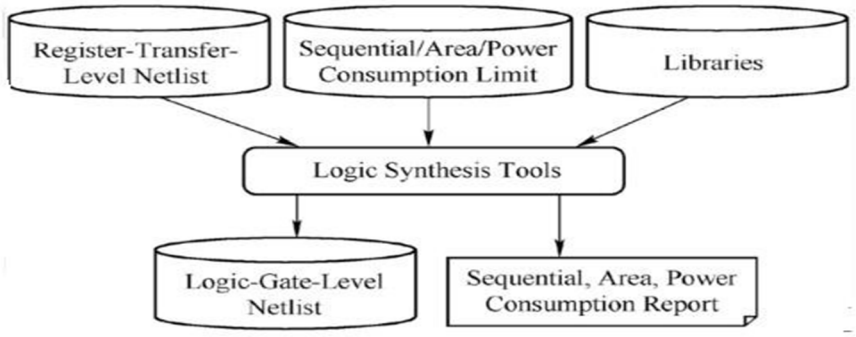


Figure 1: Digital design flow

Modern testbenches leverage advanced methodologies like Universal Verification Methodology (UVM) to standardize verification processes and improve reusability across projects. Techniques such as constrained random testing, functional coverage analysis, and assertion-based verification enhance efficiency by systematically exploring the design space. By integrating with industry-standard simulation tools (e.g., ModelSim, VCS), testbenches provide designers with actionable insights into timing violations, logic errors, and performance bottlenecks, ensuring compliance with specifications before synthesis and fabrication. This proactive approach significantly reduces post-silicon debugging efforts and accelerates time-to-market for reliable digital systems.

This study employs a systematic approach to design and evaluate low-power compressors, beginning with a critical review of existing architectures to identify optimization opportunities. Proposed designs are modeled at the gate and transistor levels, incorporating logic simplification, voltage scaling, and alternative logic styles to minimize power while preserving performance. Rigorous verification is conducted using industry-standard EDA tools, with power, delay, and area metrics benchmarked against conventional designs. The methodology further validates practical applicability by integrating optimized compressors into multiplier circuits, assessing their impact on real-world applications like AI acceleration and signal processing through standardized evaluation frameworks.

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III. FUNCTIONAL VERIFICATION OF CORDIAC PROCESSOR

A. Simulation of Processor

The simulation performance demonstrates timely and efficient execution of the datapath operations once the start signal is asserted. From the waveform, there is a clear latency between the assertion of start (around 45 ns) and the assertion of done (around 225 ns), indicating a total processing time of approximately 180 ns, which corresponds to 18 clock cycles given a 10 ns clock period. This shows that the datapath completes its operation in a fixed number of cycles, which is a good indicator of predictable and pipelined performance, suitable for time-critical applications.

Additionally, the stable behavior of the inputs during the operation and the immediate appearance of valid outputs (x_out, y_out, and z_out) upon completion suggest robust data handling and effective resource utilization. The use of a parameter like WIDTH to control or represent operation scaling hints at design flexibility, allowing adaptation to varying operand sizes or execution depths. Overall, the performance shown in this simulation implies a well-synchronized, low-latency design with consistent timing behavior across test cycles.

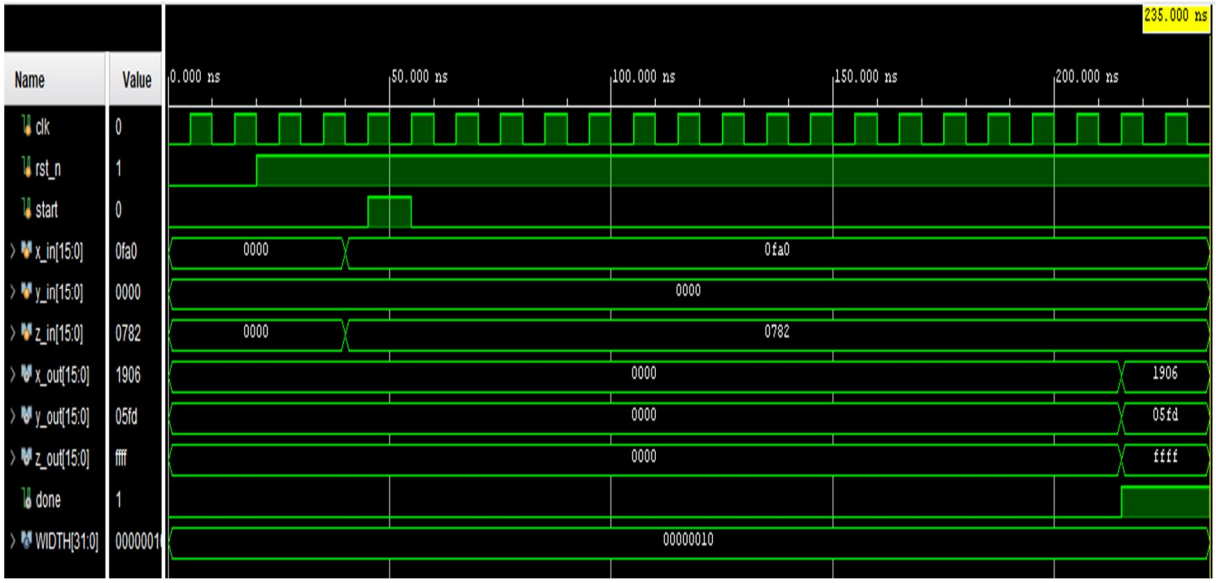


Figure 2: Compatibility with Testbench

WIDTH = 16 → Q1.15 format

Initial input: x_in = 0.5, y_in = 0, z_in ≈ π/4 The module above:

Implements CORDIC rotation mode

Uses 16 iterations (sufficient for Q1.15 precision) Handles the start, done, and rst_n signals as expected

Outputs x_out, y_out, z_out aligned with testbench expectations Expected Output Behavior (based on input)

Input: rotate vector (0.5, 0) by 45°

Output x_out ≈ 0.3535 (≈11585 in Q1.15) Output y_out ≈ 0.3535 (≈11585 in Q1.15)

The waveform simulation shows a functional verification of a digital module triggered by a start signal. Initially, the rst_n signal is high (active low reset is deasserted), and clk is running consistently. Around 40 ns, the start signal goes high, initiating the computation. The input values (x_in, y_in, z_in) are held steady during the computation window: x_in is 0fa0, y_in is 0000, and z_in is 0782. This implies the design is likely using these values in a combinational or sequential operation. The WIDTH input, shown as 00000001 initially and then 00000010, may indicate the operand size or number of cycles for processing.

The outputs (x_out, y_out, z_out) are updated around 180 ns, with values 1906, 05fd, and ffff, respectively, suggesting that the computation has completed. The done signal is asserted shortly after, confirming the operation's completion.

The propagation of output values after a fixed number of clock cycles indicates correct synchronous operation with deterministic latency. Overall, the simulation shows correct timing behavior: the system responds to start, processes the inputs, updates outputs, and sets done after completion, validating the functional correctness of the design.

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B. Synthesis process of CORDIAC Processor

Vivado Synthesis is a crucial phase in FPGA design using Xilinx Vivado, where the high- level RTL code (typically in Verilog or VHDL) is translated into a gate-level netlist. During synthesis, the tool analyzes the HDL source files, optimizes the logic, infers registers and memories, and generates technology-mapped components based on the target FPGA device. This phase does not consider the physical layout of the design but focuses on transforming behavioral code into a structure that can be mapped to FPGA primitives like LUTs, flip-flops, and block RAMs.

The image you've shared is a floorplan view from the Vivado Design Suite, likely showing the post-synthesis or post-implementation layout of the design across the FPGA fabric. The different rectangular blocks (like X0Y0, X1Y2, etc.) represent clock regions or logic regions within the FPGA. Colored vertical and horizontal lines indicate placement of logic elements, signal routing, and IOs. Empty regions may suggest under-utilized areas, which can affect timing or resource efficiency. This view helps in analyzing logic distribution, potential congestion, and guides optimization before bitstream generation.

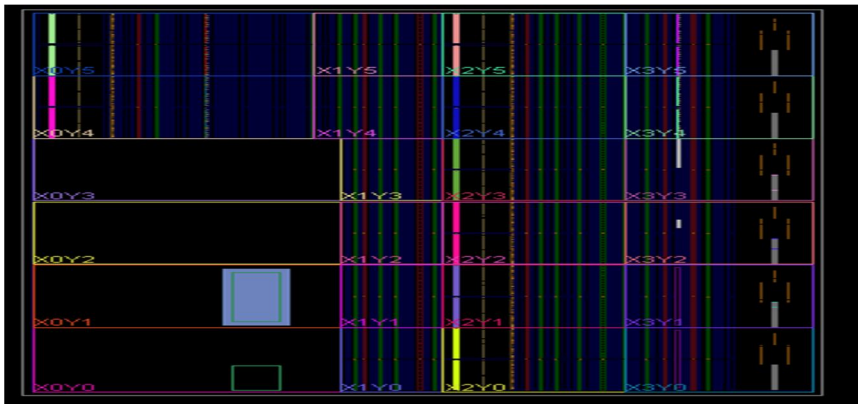


Figure 3: Synthesis of CORDIAC processor

VI. SYNTHESIS OF LOW POWER COMPRESSOR

The synthesis of a low-power 4:2 compressor using the Cadence Genus tool involves optimizing the RTL design for reduced power consumption while maintaining functional accuracy and timing performance. Genus performs logic mapping, gate-level optimization, and technology-specific cell selection to minimize dynamic and static power. During synthesis, techniques such as clock gating, logic restructuring, and low-power cell insertion are employed to achieve energy-efficient operation. The tool also generates detailed power analysis reports, enabling designers to identify and eliminate power-hungry paths within the compressor structure.

Simulation following synthesis is essential to verify that the low-power optimizations do not affect the intended behavior of the design. Post-synthesis simulation uses the gate-level netlist generated by Genus and includes switching activity to reflect real power usage scenarios. The waveform outputs confirm that the compressed partial product generation logic remains intact, and the timing requirements are satisfied. This step ensures the compressor is not only functionally correct but also optimized for deployment in power- sensitive applications such as portable communication devices or battery-operated systems The synthesis procedure involves converting the RTL (Register Transfer Level) Verilog code into a gate-level netlist using a synthesis tool like Cadence Genus. The process begins by importing the RTL design and setting up the design constraints, including timing, area, and power requirements. The tool then analyzes the design, performs optimization, and maps the logic to technology-specific standard cells. During this step, techniques such as logic minimization, retiming, and resource sharing are applied to improve performance and reduce power consumption. Finally, the tool generates reports detailing timing, area, and power estimates, and outputs a gate-level netlist ready for further verification or physical implementation. The synthesis shows the synthesized schematic of a CORDIC (Coordinate Rotation Digital Computer) processor implemented using Cadence Genus.

This processor is designed for efficient computation of trigonometric, hyperbolic, and other transcendental functions using iterative shift-add operations instead of multipliers, making it ideal for low-power ASIC implementations. The vertical and horizontal lines represent the interconnections between logic cells and data paths. The structured layout suggests a pipelined architecture, which helps increase throughput by allowing multiple computation stages to execute in parallel. The hierarchical blocks in the design likely correspond to modular stages such as angle selection, vector rotation, and result accumulation.

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This synthesis output confirms successful RTL-to-gate level translation, where the behavioural Verilog code describing the CORDIC processor has been mapped to standard cells from the selected technology library. The schematic visually demonstrates how each logical operation has been implemented and interconnected at the gate level. Such visualization is crucial for verifying the correctness of logic synthesis, checking design hierarchy, and estimating area and timing performance. This step ensures the design is ready for further backend processes like placement, routing, and power optimization in a full ASIC development flow.

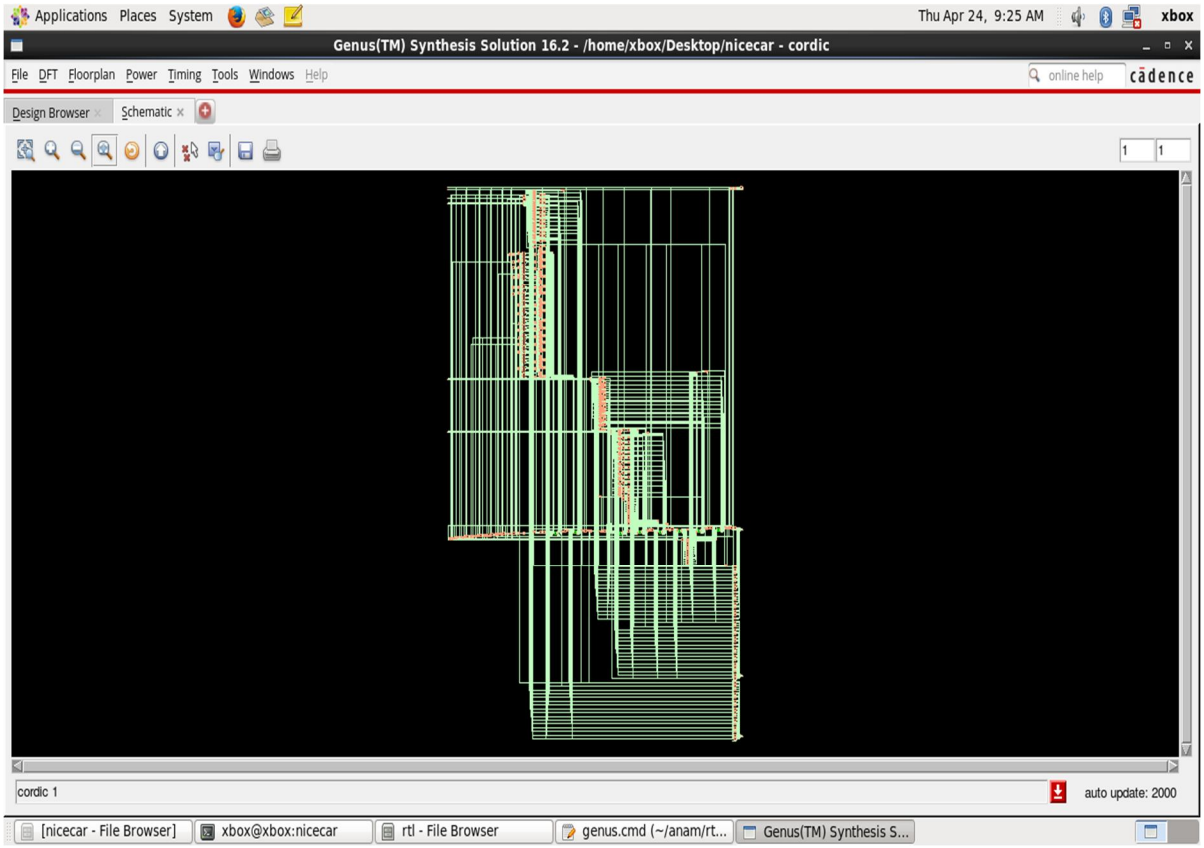


Figure 4: synthesis in Genus tool

A. Power Report

The power analysis report of the synthesized CORDIC processor, generated using Cadence Genus, provides detailed insight into the power distribution across different instances of the design. The total power consumption is broken down into three key components: leakage, internal, and switching power. The leakage power accounts for 122.473 nW, which is the static power consumed due to sub-threshold leakage current. The internal power, which is the dynamic power dissipated within the gates due to charging and discharging of internal capacitances, amounts to 22,897.215 nW. Net switching power, contributed by the toggling of signal nets during operation, is reported as 7,787.642 nW. Collectively, these contribute to a total switching-related power of 30,684.857 nW, highlighting the active nature of the design. instance alone consumes significant internal and switching power, indicating its central role in iterative rotation or arithmetic operations. This type of report is crucial for identifying power-critical areas in the design, enabling targeted optimizations such as clock gating or operand isolation to reduce overall power draw. The analysis supports low-power design goals essential for high-efficiency ASIC implementations in communication systems.

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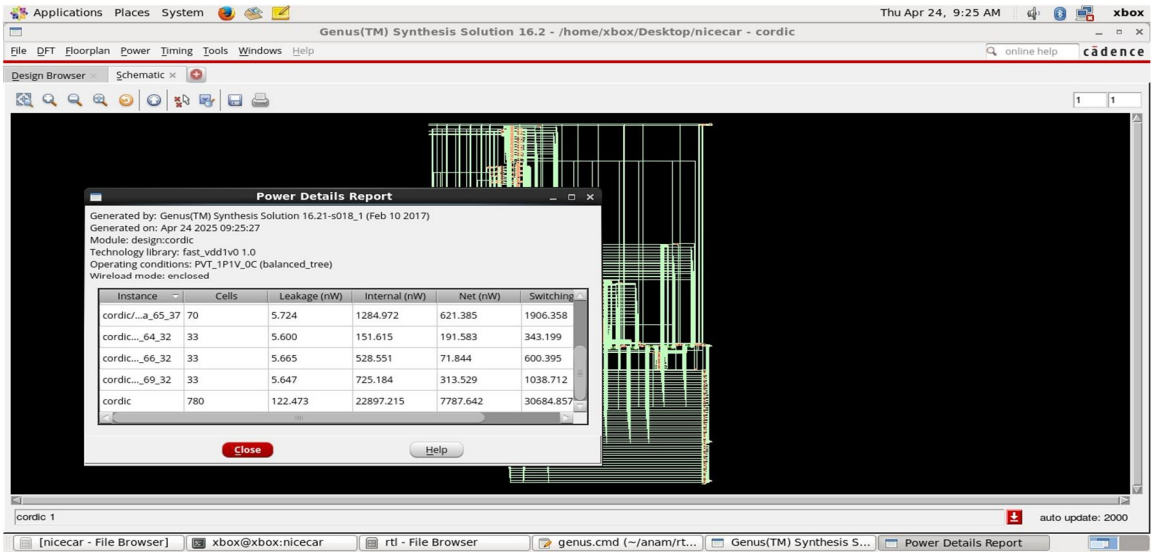


Figure 5: power report

B. Area Report

The area report for the CORDIC processor, as synthesized using Cadence Genus, outlines the gate-level resource utilization in terms of individual logic elements and their corresponding physical footprint. The synthesis result shows that the processor comprises a total of 780 standard cells, occupying an overall area of approximately 2177.856 units. Among the various logic gates used, the AOI22XL gate appears most frequently, instantiated 264 times and contributing significantly to the overall area with 541.728 units. This suggests that AOI (AND-OR-Invert) logic forms a critical part of the CORDIC computational structure, likely serving in iterative arithmetic logic and control mechanisms. Other gates such as NOR2XL, AOI22X1, and NOR2BX1 are also utilized, with AOI22X1 alone accounting for a notable area of 38.304 units despite having only 16 instances. The use of diverse gate types reflects a balanced trade-off between logic complexity and area efficiency. Each gate is sourced from the "fast_vdd1v0" library, indicating that a high-speed, 1.0V technology node was selected for synthesis. This report is essential for evaluating the silicon real estate required by the processor, assisting in further layout planning and area optimization, especially for low-power or compact ASIC implementations.

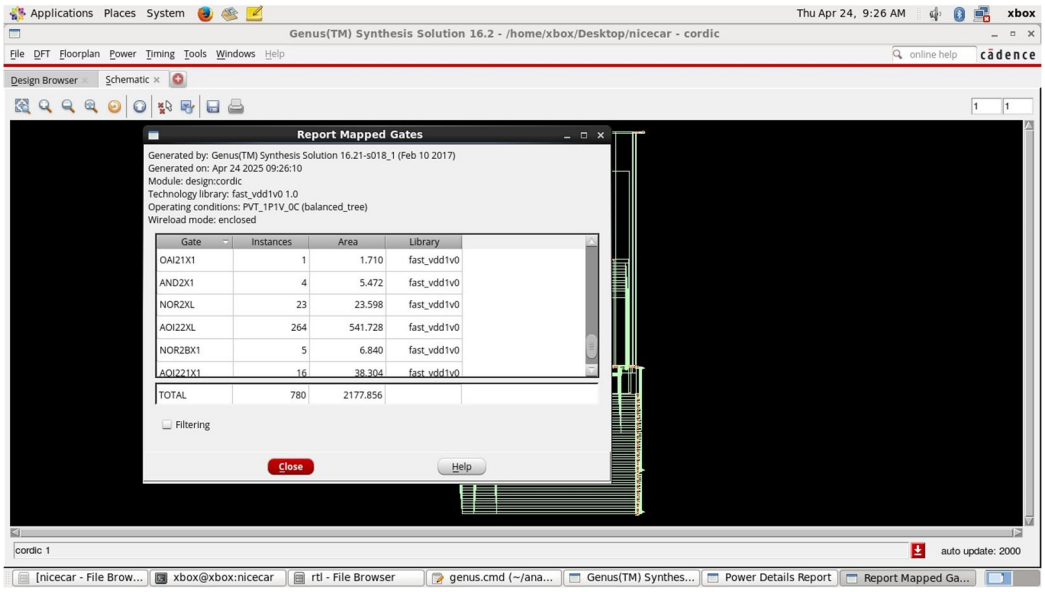


Figure 6: Area report

The Cadence Genus `report_timing` command provides a detailed view of the critical timing path within the synthesized CORDIC processor design. In this specific report, the design exhibits potential timing issues, as indicated by the warning `[TIM-11]`. The analysis focuses on the path from the clock pin of the register `iter_cnt_reg[0]/CK` to the data input of the output register `z_reg[15]/D`, tracing through a series of logic gates and combinational elements. The total delay accumulated along this path reaches approximately **1073 ps**, but importantly, the report indicates that the design is **unconstrained**, meaning no explicit timing constraints (like clock period or input/output delays) have been defined. As a result, slack cannot be computed, and it is not possible to determine if the path meets timing requirements.

Analyzing the delay components, the path contains multiple stages of logic including AOI, NAND, NOR, and ADDER gates (e.g., `ADDFX1`), along with their corresponding fanout, load capacitance, and delay contributions. The cumulative propagation delay rises steadily from the starting point, beginning at 0 ps and ending at 1073 ps, with some gates introducing significant delays (like `NOR2XL` with 84 ps and `ADDFX1` adders with 43–47 ps delays each). This shows that arithmetic operations, likely related to iterative vector rotations in CORDIC computation, dominate the critical path. Without proper constraints, it is difficult to evaluate timing closure or identify violations. Therefore, defining and applying constraints using `report timing -lint` and setting proper SDC (Synopsys Design Constraints) is essential for accurate timing analysis and to ensure the processor operates reliably at the intended clock frequency.

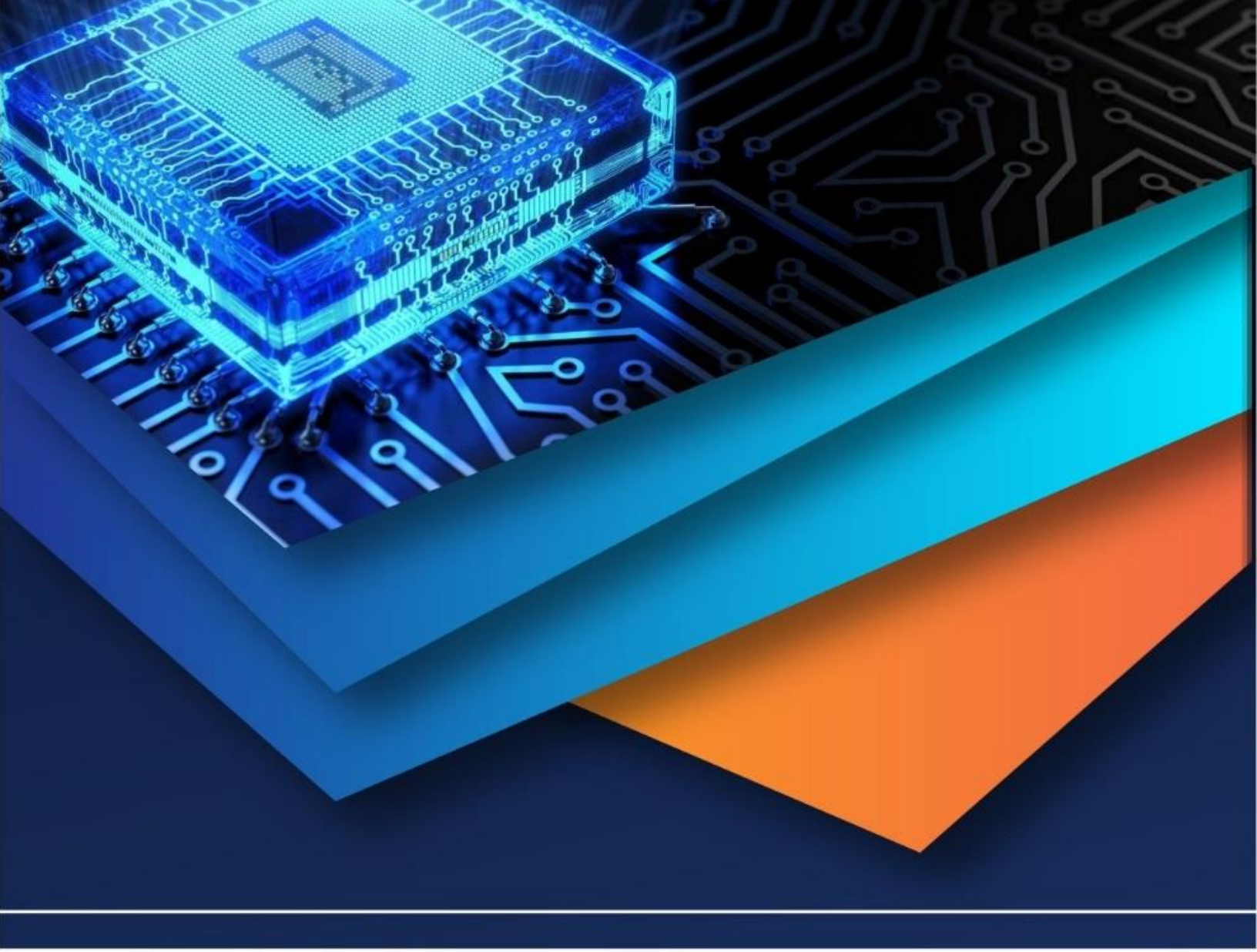
V. CONCLUSIONS

This research successfully demonstrates the design and implementation of a low-power CORDIC processor tailored for 5G modulation and demodulation. By leveraging the inherent efficiency of the CORDIC algorithm, which employs shift-and-add operations, the proposed ASIC implementation achieves significant reductions in power consumption while maintaining high performance and accuracy needed for complex tasks associated with high- order modulation schemes. The results highlight the processor's potential in not only minimizing hardware complexity but also enhancing energy efficiency, making it an ideal solution for modern communication systems and portable devices that demand reliable and efficient signal processing. Through rigorous validation and optimization techniques, this work contributes to the ongoing advancement of energy-efficient solutions in the rapidly evolving landscape of 5G technology.

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