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Comparative Analysis of Conventional and Fault-Tolerant Five-Level NPC Inverters

B. Anil Kumar[1], B.Rohith[2], P. Karthikeya[3], N. Rahul[4], T. Murali Krishna[5]
Department of EEE, Chaitanya Bharathi Institute of Technology, Hyderabad

Abstract: ***This paper presents a comparative analysis of fault behaviour in conventional and fault-tolerant five-level Neutral-Point Clamped (NPC) inverters. While conventional multilevel inverter architectures are known for their ability to lower Total Harmonic Distortion (THD) and reduce the need for bulky filters, they often encounter reliability concerns due to a higher component count and challenges in maintaining capacitor voltage balance. In contrast, fault-tolerant inverter designs are developed to improve system dependability by minimizing the impact of faults in power sources or switching devices, often through optimized switching strategies that require minimal circuit modifications. Moreover, decreasing the number of active switching devices not only improves overall system efficiency but also enhances its ability to withstand faults, making the setup more robust and reliable.This work investigates the fault performance of both conventional and fault-tolerant five-level NPC inverters under varied operational scenarios. The analysis is performed using MATLAB/Simulink simulations, with the outcomes validating the improved reliability offered by fault-tolerant configurations.***
Keywords: Multilevel inverters, five-level NPC inverter, fault analysis, fault-tolerant inverter, THD.

I. INTRODUCTION

Multi-LevelInverters (MLIs) have become essential components in modern power electronics thanks to their ability to produce voltage waveforms with excellent quality and significantly reduced harmonic distortion [1–2]. Among the different MLI configurations, the Neutral Point Clamped (NPC) topology stands out as a popular choice, particularly in industrial motor drives and grid-tied renewable energy systems, because of its high efficiency and enhanced power quality [3–4]. The five-level NPC inverter offers a notable improvement over the traditional three-level version by providing more voltage levels, which helps reduce switching stress, lower Total Harmonic Distortion (THD), and achieve smoother output waveforms [5–6].

Despite these advantages, NPC inverters remain susceptible to faults, particularly Open-Circuit (OC) and Short-Circuit (SC) faults in switching elements such as the Insulated-Gate Bipolar Transistors(IGBTs) and MOSFETs [7-8]. These faults can lead to voltage imbalance, increased harmonics, and overall system instability, potentially resulting in performance degradation or system shutdown [9-10]. Therefore, implementing effective fault detection and mitigation strategies is essential for ensuring continuous and reliable operation in NPC-based systems [11-12].

To address these challenges, fault-tolerant inverter topologies have been developed, incorporating features such as redundant switch arrangements, fault bypass paths, and adaptive control strategies capable of reconfiguring the inverter's operation during fault conditions [13-14]. These enhancements allow the inverter to maintain functionality even under fault scenarios, thereby improving system resilience and operational reliability [15].

II. LITERATURE SURVEY

A. Traditional Five-Level NPC Inverter

The traditional five-level NPC inverter is constructed using multiple power switches, clamping diodes, and DC-link capacitors to produce five distinct output voltage levels [15]. This configuration is well-regarded for its ability to reduce THD, minimize voltage stress on each switching device, and maintain high efficiency in medium- to high-power applications [16]. Despite these advantages, the design has certain limitations, such as voltage imbalance across the DC-link capacitors, structural complexity due to the numerous components involved, and a higher risk of failures in semiconductor devices like IGBTs and MOSFETs [17-18].

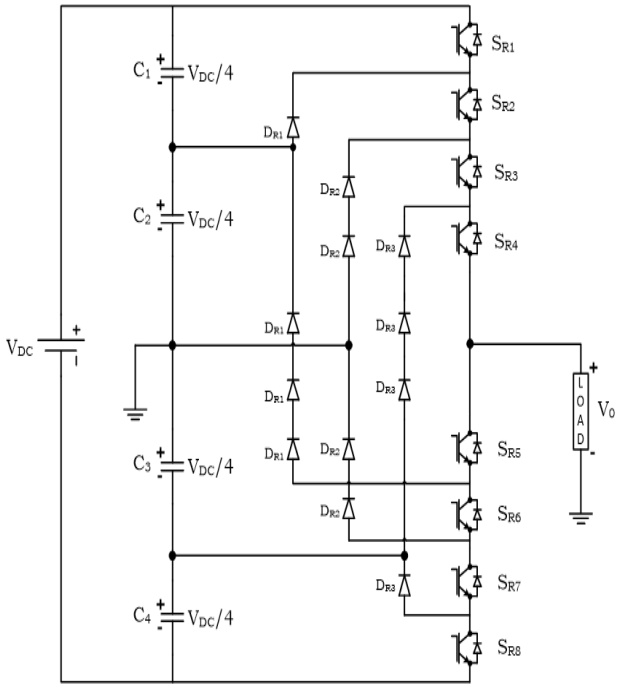


Fig. 1. Diode Clamped Five Level Inverter

TABLE I
SWITCHING STATES OF THE CONVENTIONAL
FIVE-LEVEL INVERTER

Voltage Level	S1	S2	S3	S4	S5	S6	S7	S8
$+V_{dc}/2$	1	1	1	1	0	0	0	0
$+V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

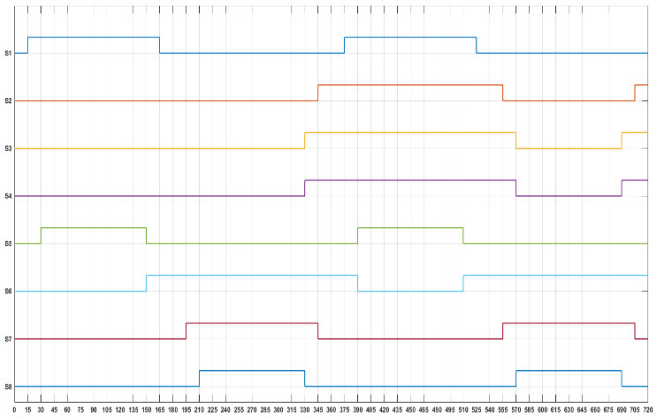


Fig. 2. Control signals for conventional NPC topology

In a traditional NPC inverter, the output voltage is generated in discrete steps of $+V_{dc}/2$, $+V_{dc}/4$, 0, $-V_{dc}/4$, and $-V_{dc}/2$. These voltage levels are achieved by appropriately controlling the conduction sequences of appropriate switches along with the clamping diodesin each phase [19].

B. Fault-Tolerant Five-Level NPC Inverter

Fault-tolerant NPC inverters improve reliability by incorporating redundancy methods that ensure continued operation during switch or diode failures [17]. These strategies effectively minimize disruptions and maintain stable voltage levels [18]. Common solutions involve dynamic reconfiguration of switching sequences and adding backup components [19], though they lead to increased design complexity and higher costs [20]. A fault-tolerant inverter with two DC sources, diodes, and unidirectional switches to generate switching pulses. When a fault occurs, the systemshifts from five-level to three-level operation, which leads to a decrease in output voltage magnitude. To offset this drop, a transformer is introduced to restore the voltage to the desired level. Additionally, the system manages energy flow between sources to maintain balance and avoid uneven battery charging.

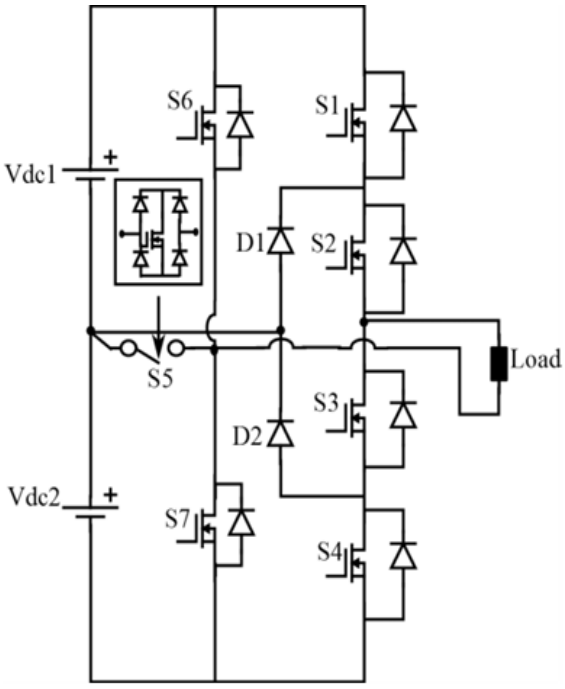


Fig. 3. Fault Tolerant Five Level Inverter

TABLE II
SWITCHING STATES OF THE FAULT TOLERANT FIVE-LEVELINVERTER

Voltage Level	S1	S2	S3	S4	S5	S6	S7
$+V_{dc}/2$	1	1	0	0	0	0	1
$+V_{dc}/4$	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0
$-V_{dc}/4$	0	1	1	0	0	1	0
$-V_{dc}/2$	0	0	1	1	0	1	0

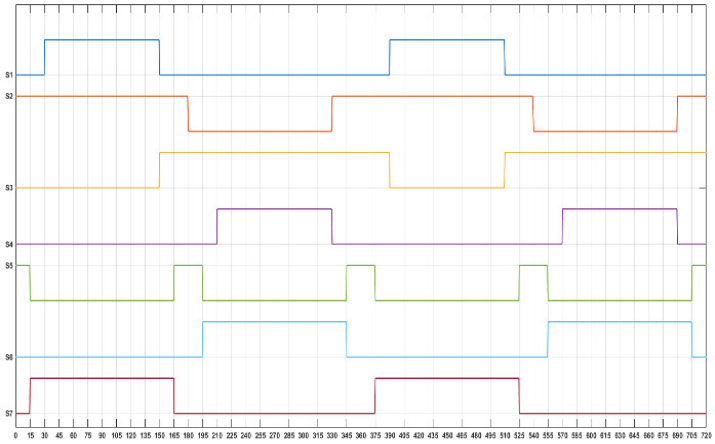


Fig. 4. Control signals for fault toleranttopology

The fault-tolerant inverter adjusts its switching strategy to bypass the malfunctioning component, ensuring uninterrupted operation [18]. For instance, in the case of an OC fault in an IGBT, the control system modifies the gate pulse patterns to redistribute the voltage levels, maintaining balanced output performance [19-20]. During such faults, the inverter typically operates at three voltage levels instead of the usual five, effectively reducing the number of voltage steps while still delivering a stable and functional output. During fault conditions, the conventional five-level NPC inverter exhibits increased THD due to imbalance in output voltage levels. The lack of fault-tolerant features leads to waveform distortion and degraded power quality. Neutral point voltage becomes unstable, affecting system reliability. Additionally, fault detection and isolation remain complex challenges.

III. SIMULATION RESULTS

The simulation was carried out using MATLAB, and the corresponding results are presented below.

A. Traditional Five Level NPC Inverter

1) Without fault

The traditional five-level NPC inverter circuit is shown in Figure 5.

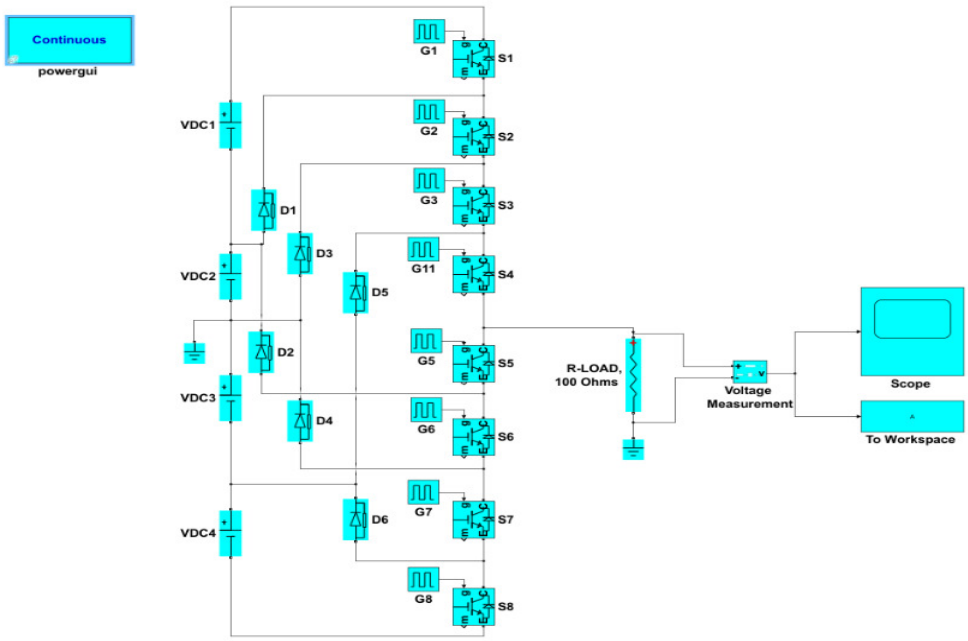


Fig. 5. Simulink model for conventional five level NPC inverter

The output voltage waveform as a function of time under normal operating conditions is presented in Figure 6.

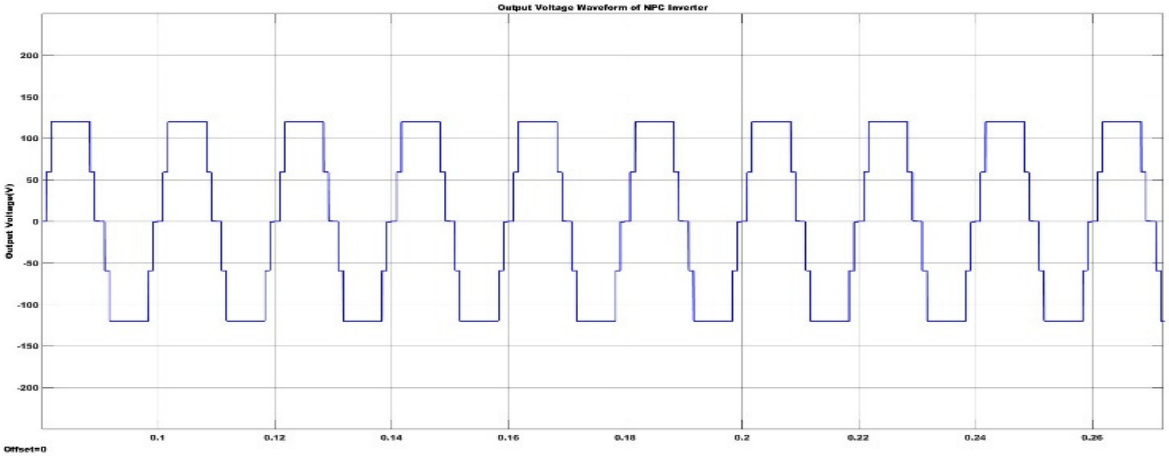


Fig. 6. Output Voltage waveform under no fault condition

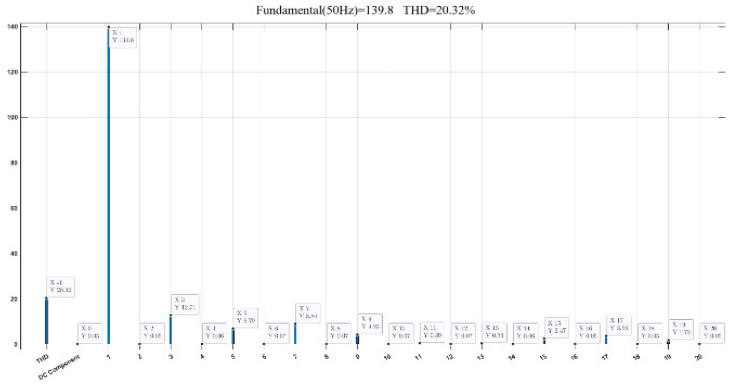


Fig. 7. FFT analysis under no fault condition

The harmonic spectrum under no fault conditions is presented in Fig. 7, indicating a THD of 20.32%.

2) With fault

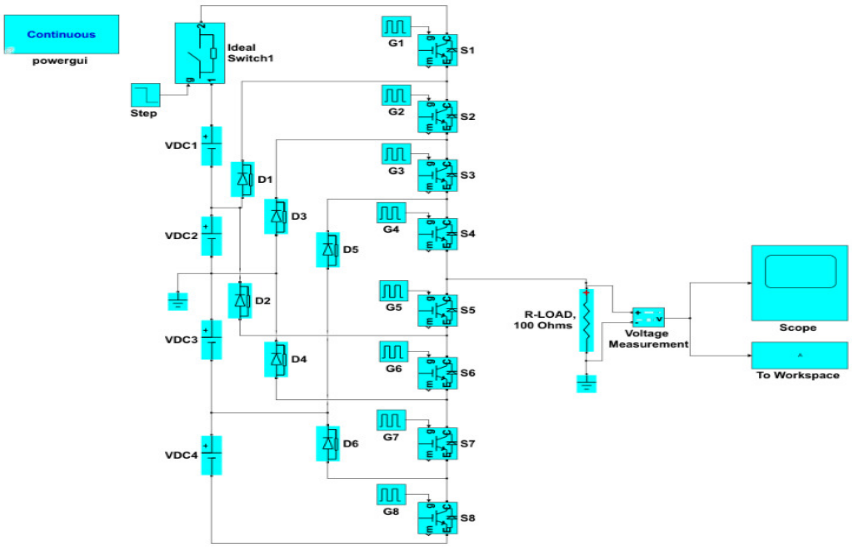


Fig. 8. Simulink model of conventional five level NPCwith IGBT1 open switch fault

The output voltage waveform of conventional five level NPC in the presence of a fault are shown in Fig. 9.

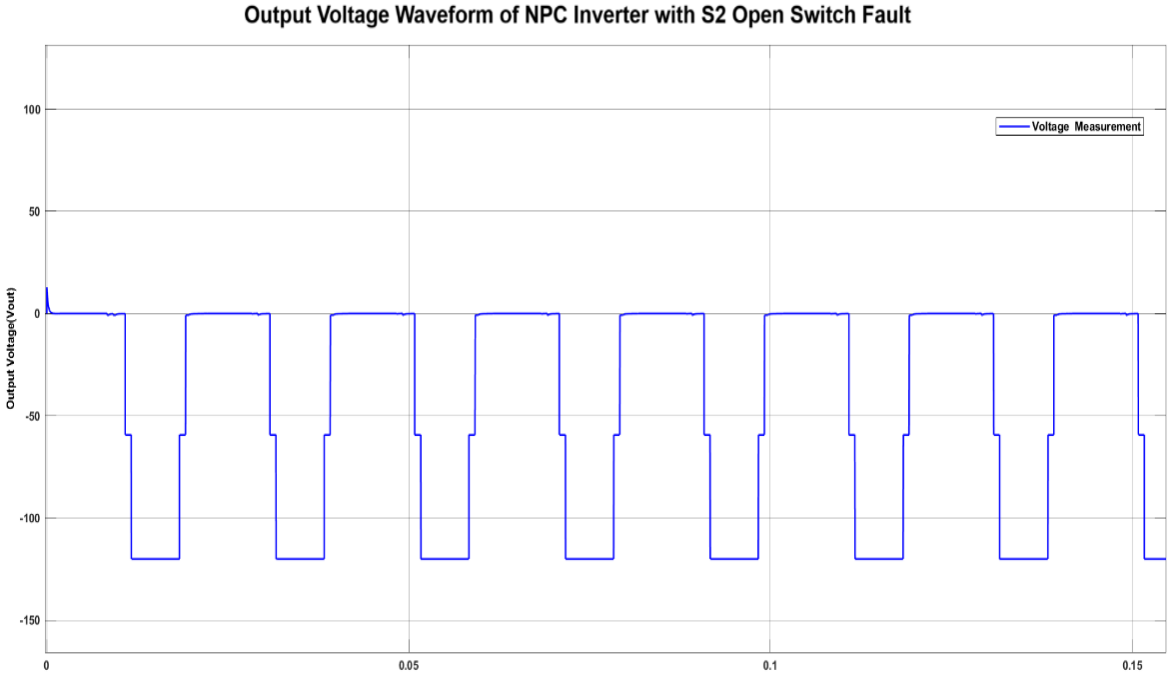


Fig. 9. Output Voltage waveforms in the presence of a fault

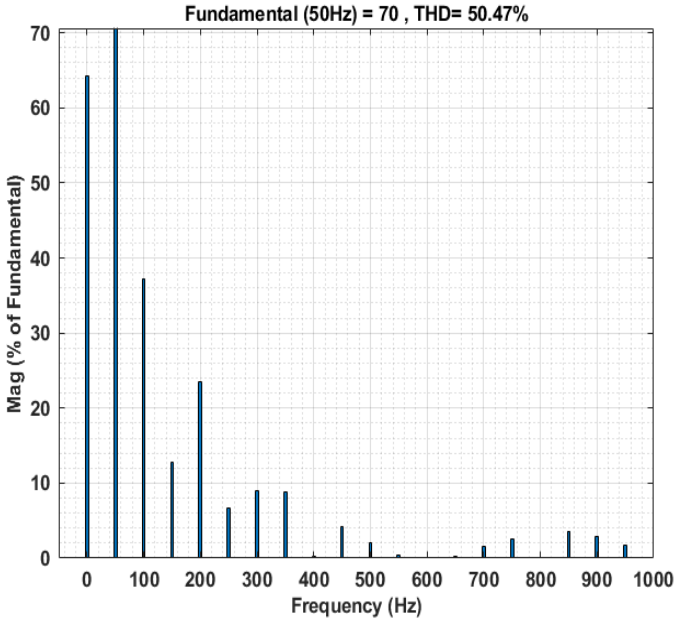


Fig. 10. FFT analysis in the presence of a fault

The harmonic spectrum under fault conditions is presented in Fig. 10, indicating a THD of 36.87%.

B. Fault Tolerant Five Level NPC inverter

1) Without fault

The traditional five-level NPC inverter circuit is shown in Fig. 11.

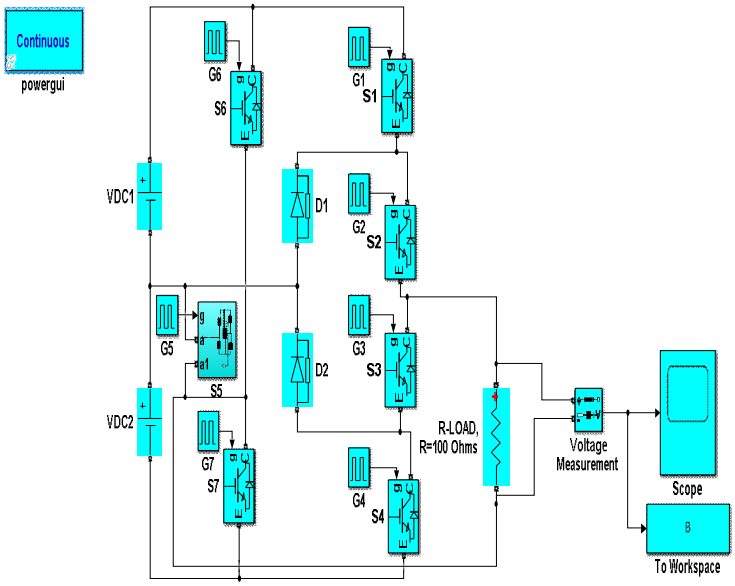


Fig. 11. Simulink model for Fault Tolerant Five Level NPC inverter

The waveforms of output voltage under no fault scenario are displayed in Fig. 10.

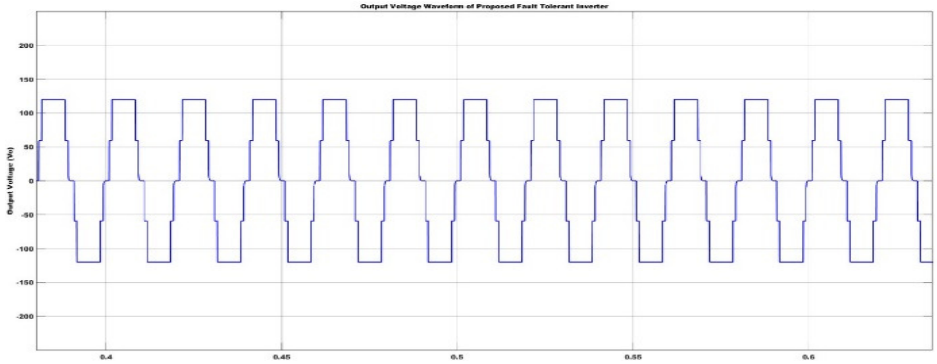


Fig. 12. Output waveforms under no fault condition

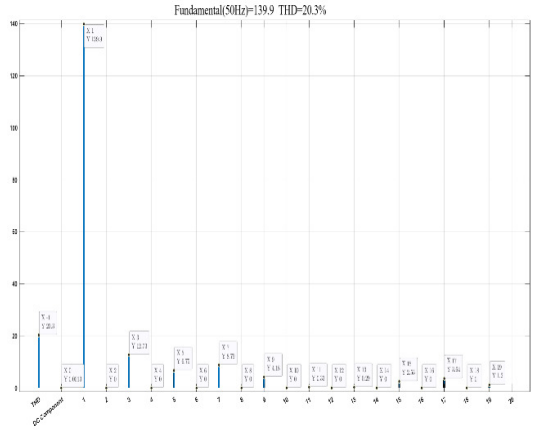


Fig. 13. FFT analysis under no fault condition

The harmonic spectrum under no fault conditions is presented in Fig.13, indicating a THD of 20.3%.

2) With fault

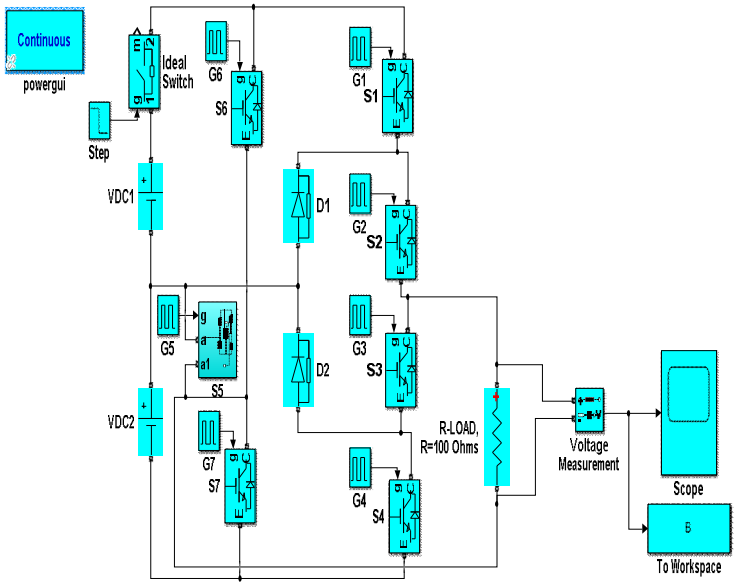


Fig14. Simulink model Fault Tolerant Five Level NPC inverter with dc1 source failure

The waveform of output voltage under fault condition are shown in Fig. 15.

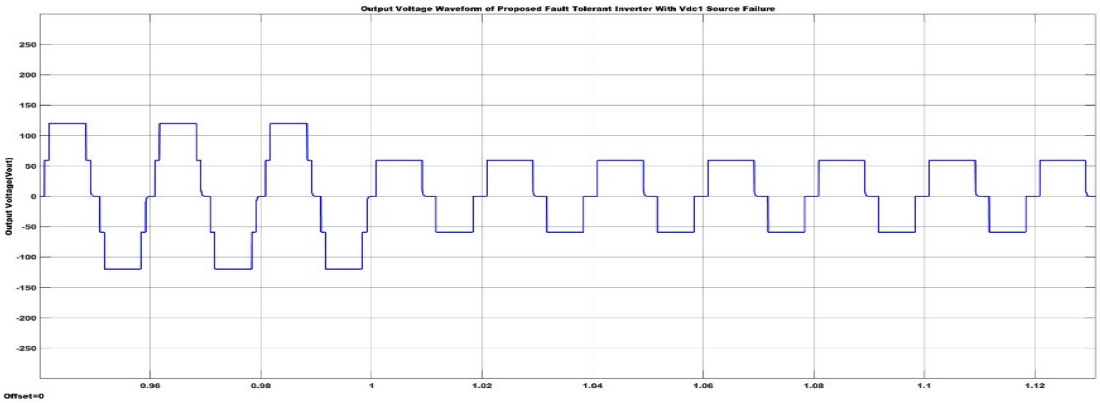


Fig. 15. Output waveform in the presence of a fault

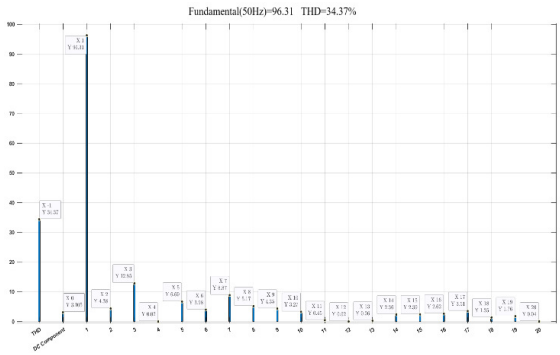


Fig. 16. FFT analysis in the presence of a fault

The harmonic spectrum under fault conditions is presented in Fig. 16, indicating a THD of 34.37%.

TABLE III
SUMMARY OF FFT ANALYSIS

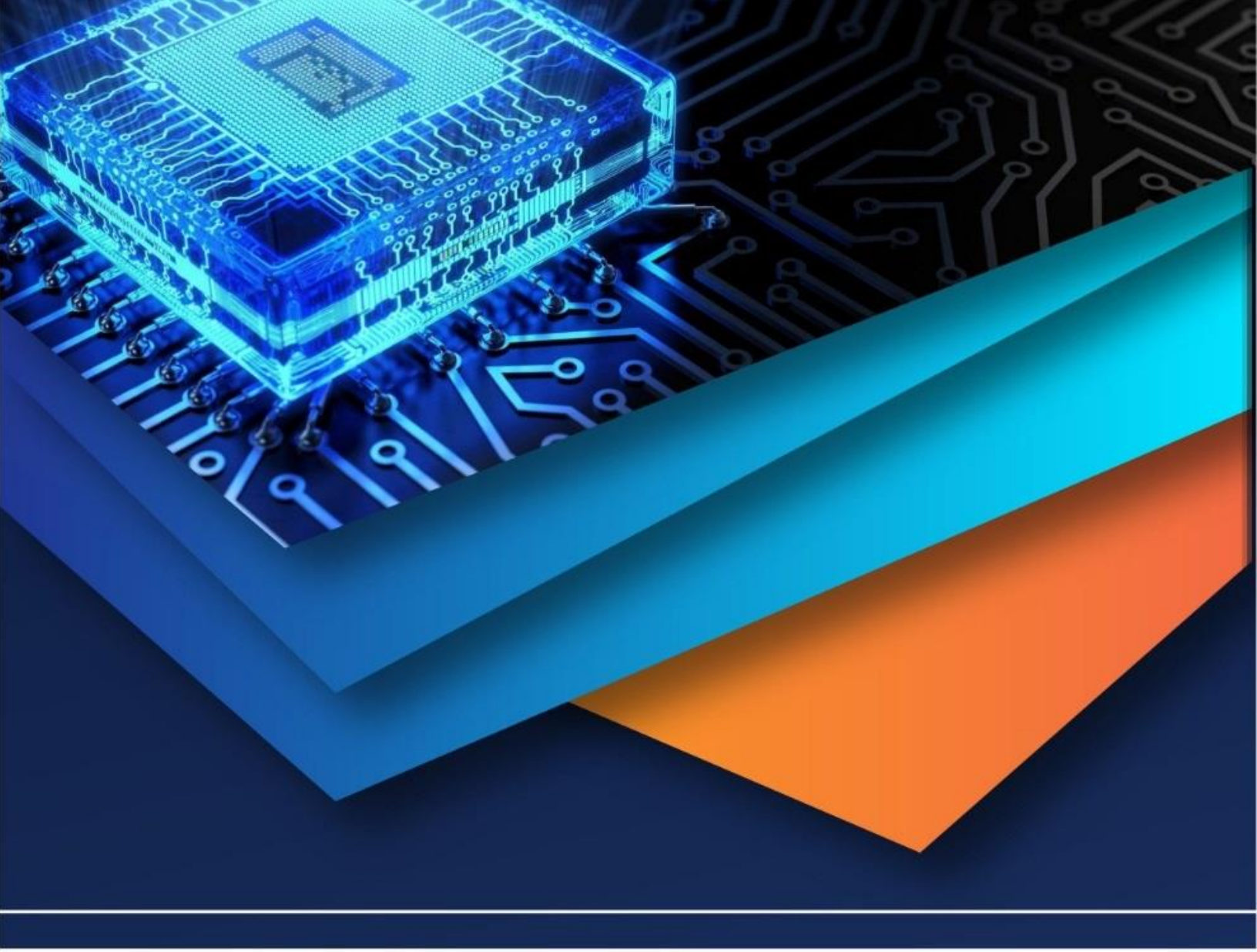
	Conventional Five Level NPC inverter		Fault Tolerant Five Level Inverter	
	Normal	During switch open	Normal	During switch open
Fundamental Component	139.8	70	139.9	96.31
% THD	20.32	50.47	20.3	34.37

IV. CONCLUSIONS

The results indicate that while conventional NPC inverters suffer from significant performance degradation in the presence of faults, the proposed fault-tolerant topology effectively mitigates these issues by redistributing voltage levels and maintaining operational stabilityBoth simulation and experimental studies show that the fault-tolerant NPC inverter offers better reliability, lowerTHD, and stronger performance in the presence of a faults. These improvements make it a promising option for demanding applications like renewable energy systems and industrial motor drives, where consistent and reliable operation is crucial.

REFERENCES

[1] S. Ahmadi, P. Poure, S. Saadate, and D. A. Khaburi, "Fault tolerance analysis of five-level neutral-point-clamped inverters under clamping diode open-circuit failure," Electronics, vol. 11, no. 9, p. 1461, 2022.
[2] P. Ba, K. Suresh, and E. Parimalasundar, "Fault analysis in the 5-level multilevel NCA DC–AC converter," Automatika, vol. 64, no. 3, pp. 606–612, 2023.
[3] M. Jalhotra, L. K. Sahu, S. P. Gautam, and S. Gupta, "Reliability and energy sharing analysis of a fault-tolerant multilevel inverter topology," IET Power Electronics, vol. 12, no. 4, pp. 819–828, 2019.
[4] N. K. Dewangan, T. K. Tailor, R. Agrawal, and P. Bhatnagar, "A multilevel inverter structure with open circuit fault-tolerant capability," Electrical Engineering, vol. 103, pp. 1613–1628, 2021.
[5] Y. Shen, Y. Zhang, and X. Wang, "Fault-tolerant control strategy for neutral-point-clamped three-level inverter," Journal of Control Science and Engineering, vol. 2018, Article ID 5126404, 2018.(2002) The IEEE website. [Online]. Available: http://www.ieee.org/
[6] D. Kumar, R. K. Nema, and S. Gupta, "Development of fault-tolerant reduced device version with switched-capacitor based multilevel inverter topologies," International Transactions on Electrical Energy Systems, vol. 31, no. 7, e12893, 2021.
[7] S. Sivapriya and R. Kumar, "Enhancing reliability in multilevel inverter: A fault-tolerant approach with reduced switch count," International Journal of Circuit Theory and Applications, vol. 49, no. 7, pp. 1735–1750, 2021.
[8] K. S. Kumar, "A fault-tolerant single-phase five-level inverter for grid-independent PV systems," RAE, 2015.
[9] D. Maharjan, S. Rana, and N. Paudel, "A review on multilevel inverters and their applications," IEEE Trans. Power Electron., vol. 36, no. 5, pp. 1242–1256, 2021.
[10] J. Rodríguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 882–892, 2002.
[11] E. Babaei, M. Alilu, and S. Laali, "A new general topology for cascaded multilevel inverters with reduced number of components," IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 3932–3941, 2019.
[12] P. Choudhary and B. Singh, "Model-based fault diagnosis and mitigation in multilevel inverters," IEEE J. Emerg. Sel. Topics Power Electron., vol. 8, no. 3, pp. 1124–1135, 2020.
[13] A. Kumar and S. Jain, "Fault-tolerant control of neutral-point-clamped inverters," IEEE Trans. Power Electron., vol. 32, no. 9, pp. 7234–7243, 2017.
[14] K. Al-Haddad, H. Kanaan, and M. Ghribi, "Voltage balancing techniques for diode-clamped multilevel inverters under fault conditions," IEEE Trans. Power Electron., vol. 36, no. 10, pp. 15547–15558, 2021.
[15] X. Li, P. Wang, and Y. Zhao, "Artificial intelligence-based fault-tolerant control strategies for multilevel inverters," IEEE Trans. Ind. Electron., vol. 65, no. 11, pp. 8884–8893, 201



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