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Comparison of Performance Fault-Tolerant Five Level Inverter with and without PWM Technique Multilevel Inverter

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Abstract: ***Five-level Neutral Point Clamped (NPC) inverters are widely utilized in high-power and industrial systems due to their ability to generate high-quality output waveforms, minimize Total Harmonic Distortion (THD), and evenly distribute voltage stress across semiconductor switches. Despite these advantages, their intricate topology makes them vulnerable to faults such as open-circuit switches, diode failures, and imbalanced capacitor voltages. Such faults can severely impact output performance, cause waveform distortion, and potentially lead to complete system failure, particularly in precision-demanding environments like motor drives and industrial controls. This paper investigates the fault behaviour of conventional five-level NPC inverters and contrasts their performance with a Pulse Width Modulation (PWM)-based fault-tolerant inverter design. Traditional fault mitigation approaches often rely on additional hardware or redundancy, increasing both complexity and cost. In contrast, the proposed method employs a control-centric strategy using PWM to dynamically adapt switching states in the presence of faults, ensuring balanced voltage output and reduced harmonic distortion without requiring extra components. Comprehensive simulations were carried out under several fault scenarios, including single-switch failures, clamping diode defects, and imbalanced DC-link conditions. The analysis focuses on key performance indicators such as output voltage quality, THD levels, and system recovery response. The results reveal that the PWM-controlled fault-tolerant inverter consistently outperforms its conventional counterpart in maintaining waveform stability and overall reliability under fault conditions. This study emphasizes the effectiveness of PWM-based control strategies in enhancing the fault resilience and operational efficiency of five-level NPC inverter systems.***

Keywords: Five-Level NPC Inverter, Fault Tolerance, PWM Control, Total Harmonic Distortion, Multilevel Converter, Inverter Reliability, Power Electronics, Fault Diagnosis.

I. INTRODUCTION

Multilevel inverters (MLIs) are now a primary solution in high-performance power conversion systems because they can produce output voltages with close-to-sinusoidal waveform shapes, lower harmonic content, and reduced voltage stress on power devices [1], [4], [5]. Of the various multilevel topologies, the Neutral Point Clamped (NPC) inverter has been particularly useful for medium and high-power applications, owing to its diode-clamping technique that facilitates efficient voltage division over the DC bus [7]. In particular, five-level inverter (NPC) inverters enhance the waveform resolution in comparison to three-level ones with more elevated Total Harmonic Distortion (THD), superior power quality, and reduced filter needs [1], [10], [5]. Despite the advantages, the complexity level of the circuit increases significantly with an increase in the number of components in the guise of clamping diodes, gate drivers, and semiconductor switches. All these increase the hardware failure susceptibility of the system, such as IGBTs open-circuits, diode short circuits, or capacitor voltage mismatches. Conventional five-level NPC inverters usually do not possess the capability to react to faults in real-time. During failures—like a faulty switch or unstable neutral point voltage imbalance and waveform distortion can occur, which may harm the attached load and lower system reliability [15].

This highlights the need for sophisticated inverter designs that can function properly even under partial hardware failure. Fault-tolerant structures overcome this challenge through the use of intelligent switching strategies and redundant channels that allow the inverter to maintain operational continuity as a fault is being sensed [17], [18]. If there is a fault in a driver or a switch, for instance, the system can present itself to provide functionality in a degraded mode usually reducing the five-level functionality to a three-level mode. Although this reduces the amplitude of the output voltage, countermeasures such as transformer compensation and energy redistribution provide acceptable voltage levels and system stability [19], [20]. The inclusion of Pulse Width Modulation (PWM) in the fault-tolerant control system enhances the flexibility and precision of the inverter.

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PWM methods allow the system to switch gate signals dynamically based on the faulty component such that faulty components are excluded and output is highly balanced. The technique not only promotes efficient real-time response but also reduces the need for additional hardware components, making it cost-efficient as well as effective fault-handling. This paper analyses performance variations in traditional five-level NPC inverters and a considered PWM-based fault-tolerant approach. Particular fault states such as switch failure, diode fault, and capacitor unbalance are analysed and compared with simulation. This study is focused on aspects such as the topology of the output voltage waveform, THD, and system tolerance to faults. The comparison indicates the effectiveness of PWM-based fault tolerance in maintaining inverter functionality and integrity upon faults.

II. LITERATURE SURVEY

A. Conventional Fault Tolerant Five Level NPC inverter

Fault-tolerant NPC inverters enhance system reliability through redundancy techniques that allow for continuous operation in the event of switch or diode faults [17]. Fault-handling capabilities reduce levels of operation disruption and allow for stable voltage provision during fault [18]. Typical fault-tolerant systems include real-time switching sequence adjustment and inclusion of spare devices [19]. But these benefits come at the cost of a penalty in terms of increased circuit complexity and higher implementation costs [20]. In most fault-tolerant implementations, two separate DC sources, besides diodes and one-way switches, are utilized in handling gate signal generation. The inverter lowers the output voltage upon occurrence of a fault by switching from five-level to a simpler three-level operation. To compensate for this voltage drop, a transformer is employed to increase the voltage to the required level. The system also monitors so that energy is controlled between the two sources in a manner that it stays balanced and does not have uneven battery utilization

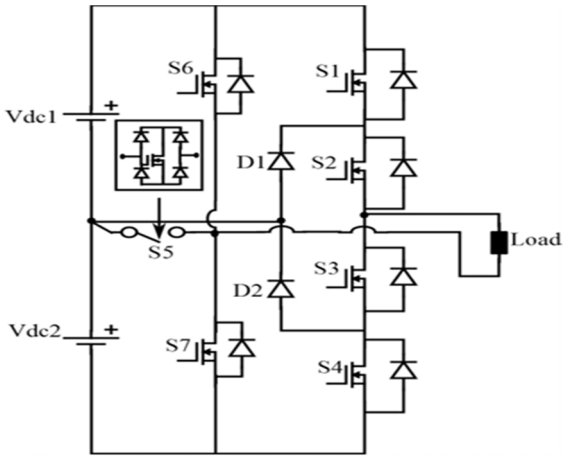


Fig. 1. Conventional Fault Tolerant Five Level Inverter

TABLE II
SWITCHING STATES OF THE FAULT TOLERANT FIVE-LEVEL INVERTER

Voltage Level	S1	S2	S3	S4	S5	S6	S7
$+V_{dc}/2$	1	1	0	0	0	0	1
$+V_{dc}/4$	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0
$-V_{dc}/4$	0	1	1	0	0	1	0
$-V_{dc}/2$	0	0	1	1	0	1	0

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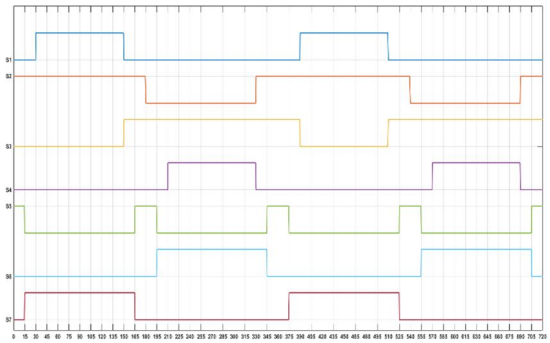


Fig. 2. Control signals for fault tolerant topology

The fault-tolerant NPC inverter adjusts its switching pattern to bypass and isolate faulty components so that the system can continue operating uninterrupted [18]. For instance, when there is an open-circuit (OC) fault in an IGBT, the control logic reallocates gate signals to redistribute voltage levels among the active switches left, thus maintaining balanced output features [19], [20]. With such conditions, the inverter tends to drop back from its conventional five-level to a lowered three-level operation. Although this mode reduces the level of voltage steps available, output is still functioning and stable to some extent.

On the other hand, traditional five-level NPC inverters do not have inherent fault-handling capabilities, and hence, the performance of these inverters degrades during faults. The component failure can cause voltage level imbalances, which have a major impact on Total Harmonic Distortion (THD) in the output. Not only does it reduce the quality of the waveform, but also leads to unstable neutral point voltage, thus weakening the overall system reliability. Further, fault detection and isolation in the inverters is a difficult task because of the complexity of the system and lack of adaptive control.

B. Fault-Tolerant Five-Level NPC Inverter with PWM Technique

The five-level Neutral Point Clamped (NPC) inverter is widely used in advanced power systems due to its capability to generate stepped voltage waveforms with improved harmonic performance and efficiency [1], [3]. However, under fault conditions especially in power semiconductor switches or clamping diodes traditional NPC inverters suffer from voltage imbalance, waveform distortion, and increased Total Harmonic Distortion (THD) [13], [15]. For improved fault robustness, enhanced NPC topologies employ redundancy strategies and smart control strategies. When a device is faulty, the inverter reconfigures its switching profile automatically to bypass the faulty device and switch to three-level operating mode to continue power flow [17],[20]. While this results in a decrease in the output voltage, employing a voltage-boosting transformer serves to compensate for the dip and ensure the voltage remains within the specified range.

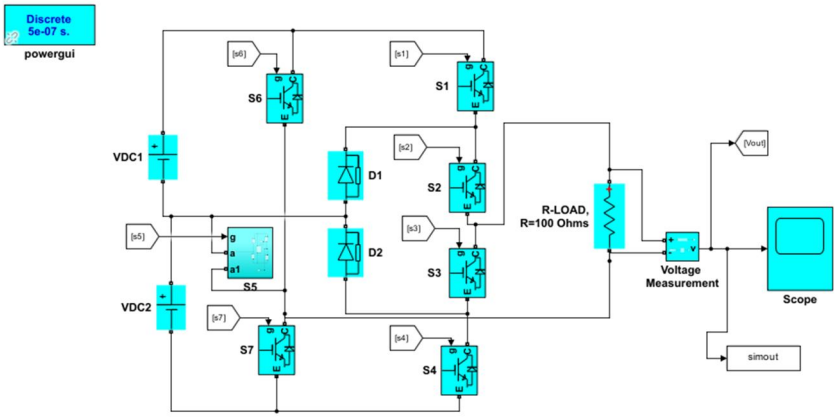


Fig.3. Fault Tolerant Five Level Inverter with PWM Technique

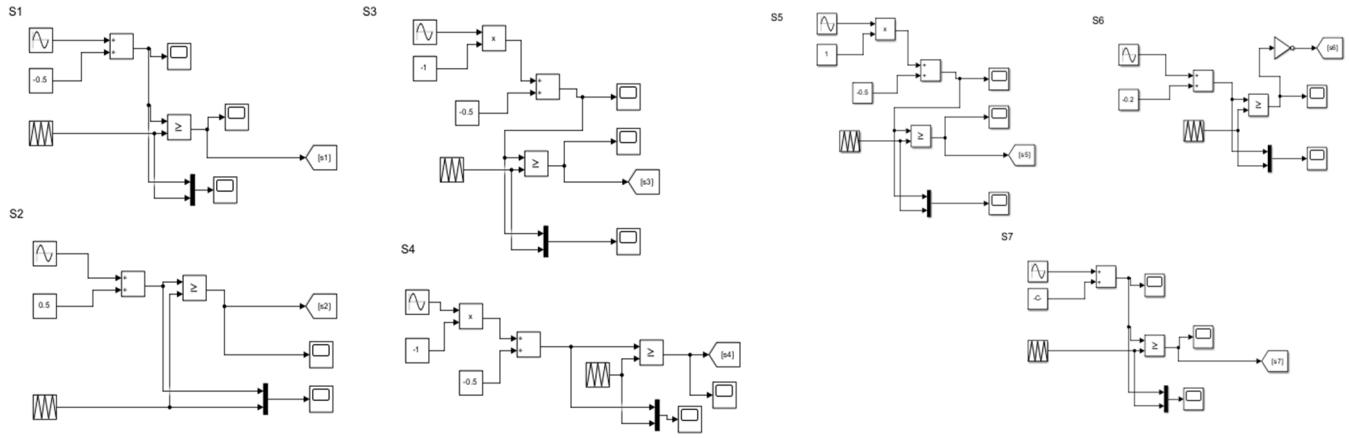


Fig.4.Gate Driver Circuits

III.SIMULATION RESULTS

The simulation was performed on MATLAB, and the results are given below.

A. Conventional Fault Tolerant Five Level NPC inverter

1) Without fault

The traditional five-level NPC inverter circuit is shown in Fig. 11.

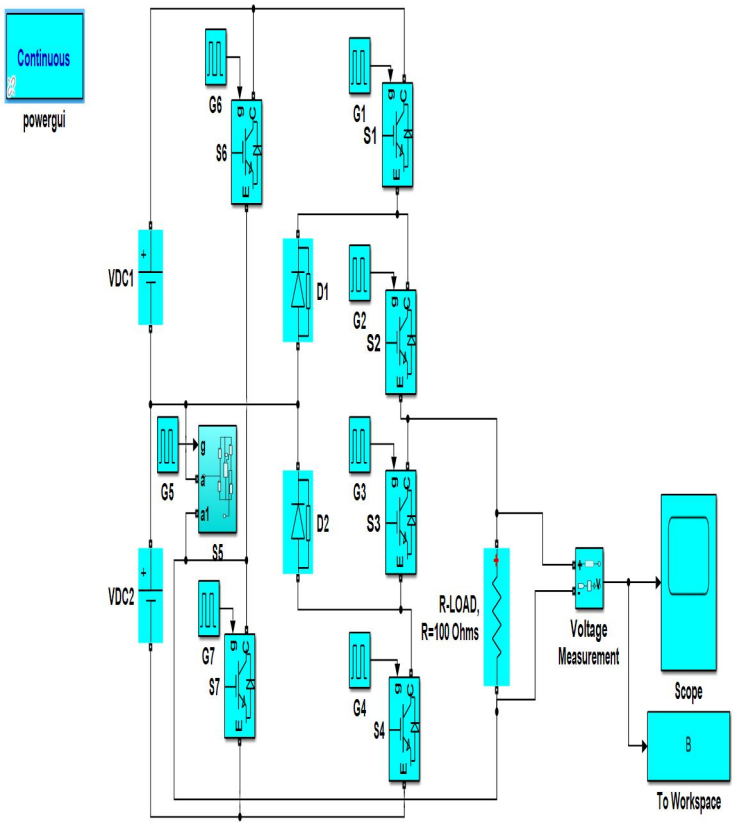


Fig. 5. Simulink model for Conventional Fault Tolerant Five Level NPC inverter

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The waveforms of output voltage under no fault scenario are displayed in Fig. 6.

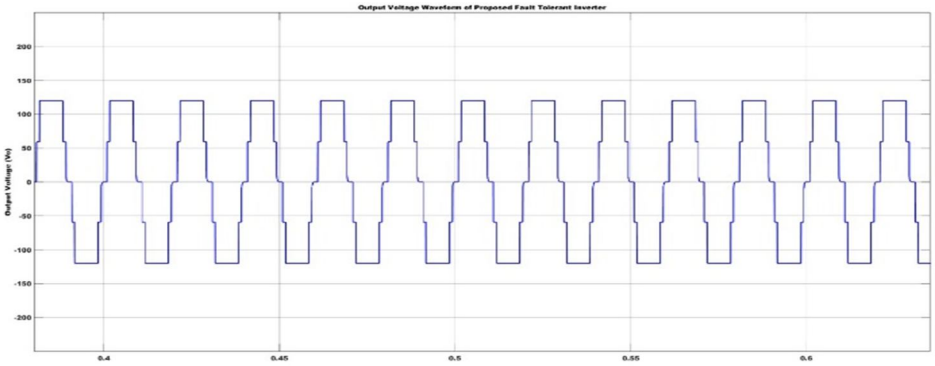


Fig. 6. Output waveforms under no fault condition

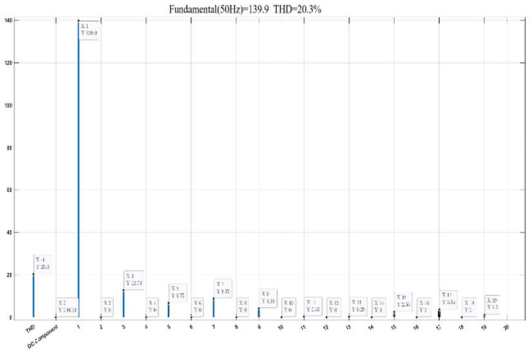


Fig. 7. FFT analysis under no fault condition

The harmonic spectrum under no fault conditions is presented in Fig.7, indicating a THD of 20.3%.

2) With fault

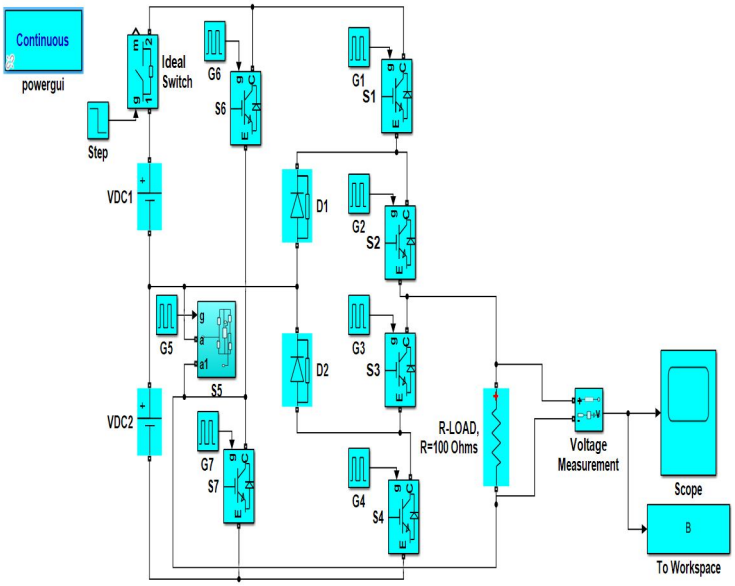


Fig.8. Simulink model Conventional Fault Tolerant Five Level NPC inverter with dc1 source failure

The waveform of output voltage under fault condition are shown in Fig. 9.

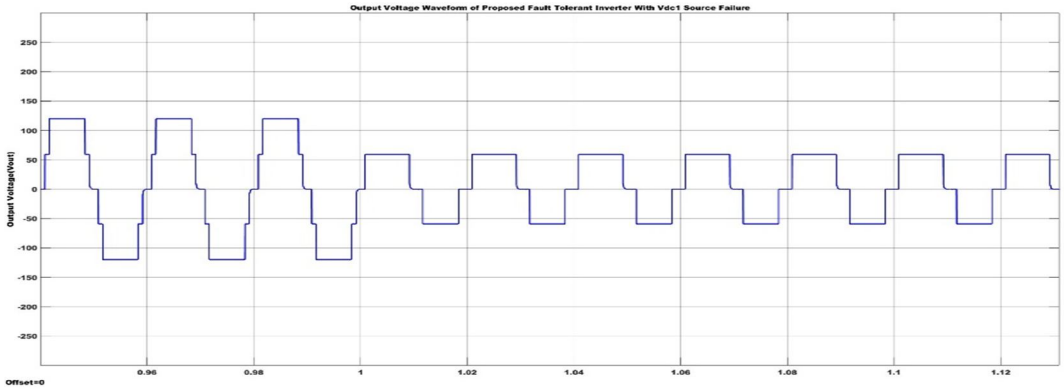


Fig. 9. Output waveform in the presence of a fault

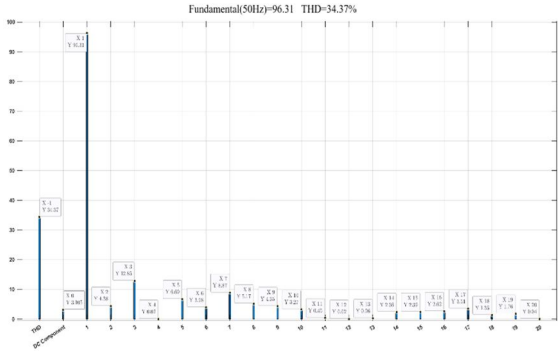


Fig. 10. FFT analysis in the presence of a fault

The harmonic spectrum under fault conditions is presented in Fig. 10, indicating a THD of 34.37%.

B. Fault Tolerant Five Level NPC inverter with PWM Technique

1) Without fault

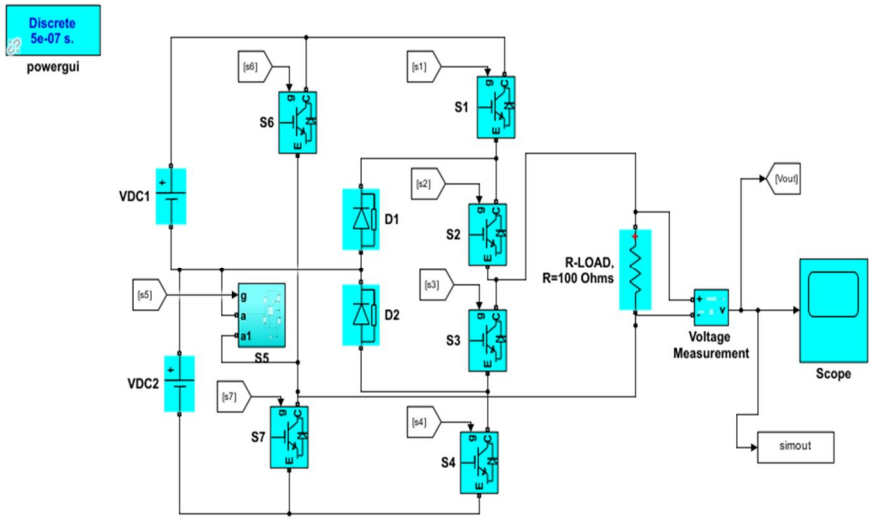


Fig. 11. Simulink model for Fault Tolerant Five Level NPC inverter with PWM Technique

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The waveforms of output voltage under no fault scenario are displayed in Fig. 12.

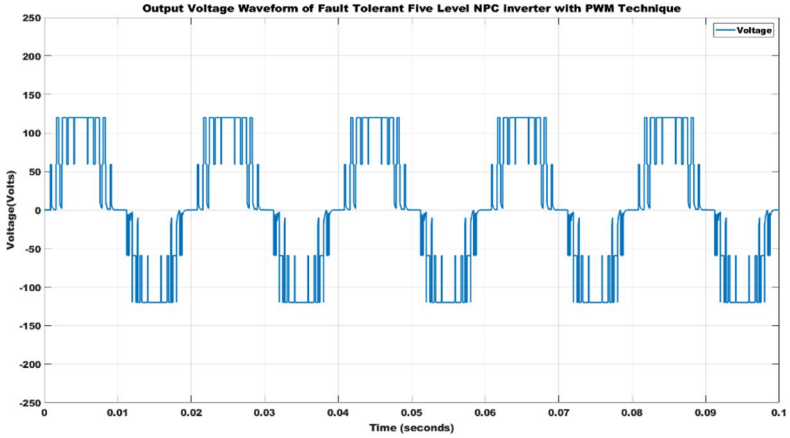


Fig. 12. Output waveforms under no fault condition

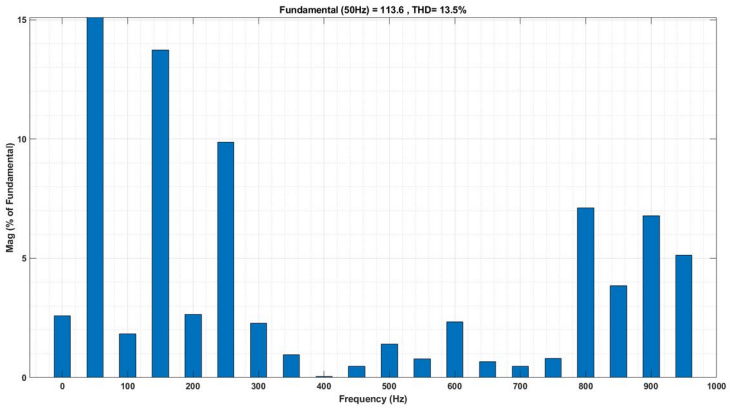


Fig. 13. FFT analysis under no fault condition

The harmonic spectrum under no fault conditions is presented in Fig.13, indicating a THD of 13.5%.

2) With Fault

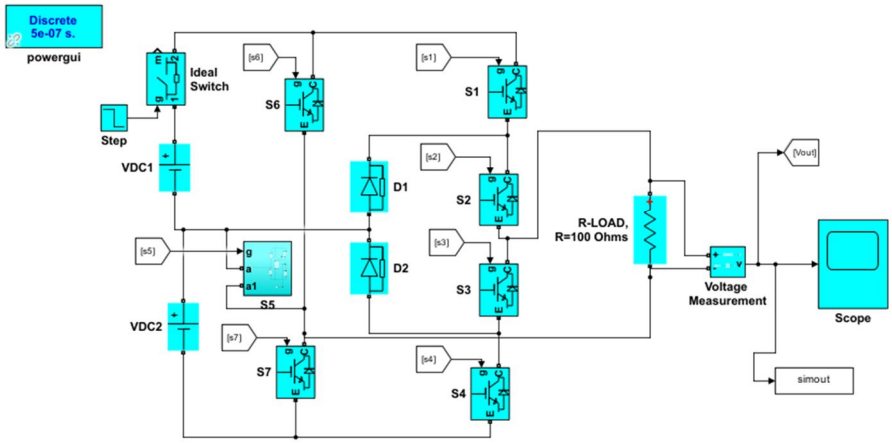


Fig14. Simulink model Conventional Fault Tolerant Five Level NPC inverter with dc1 source failure

The waveform of output voltage under fault condition are shown in Fig. 15.

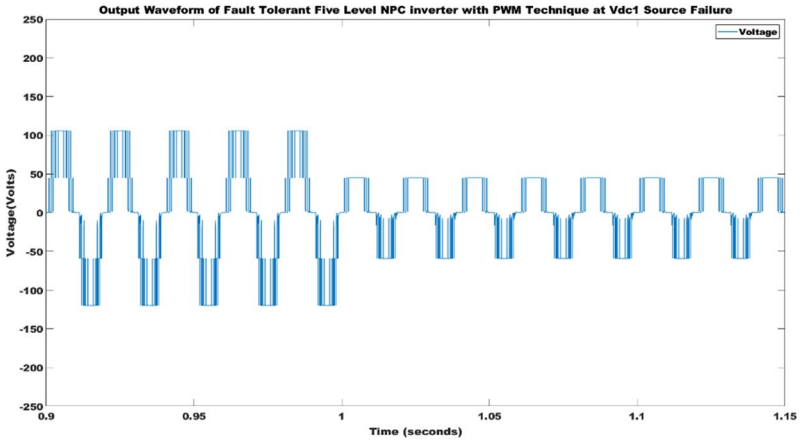


Fig. 15. Output waveform in the presence of a fault

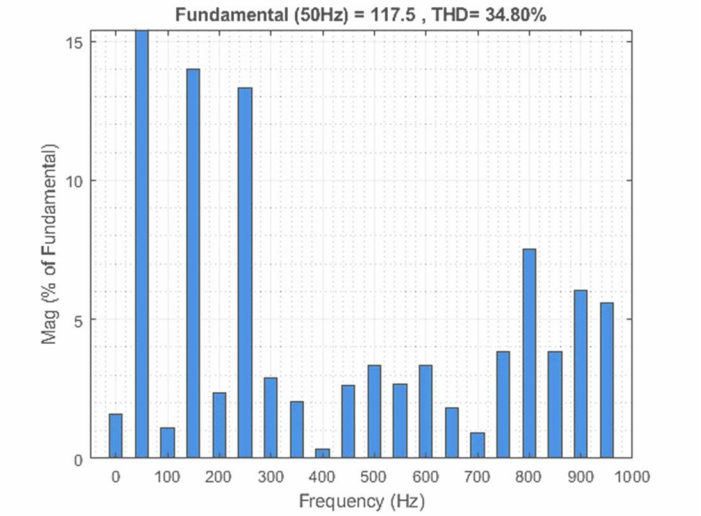


Fig. 16. FFT analysis in the presence of a fault

The harmonic spectrum under fault conditions is presented in Fig. 16, indicating a THD of 34.80%

TABLE III
SUMMARY OF FFT ANALYSIS

Topology	Fundamental Frequency (50)	THD
Conventional Fault Tolerant Five Level Inverter	139.9	20.3%
Conventional Fault Tolerant Five Level Inverter with fault condition	96.31	34.37%
Fault Tolerant Five Level Inverter With PWM Technique	113.6	13.5
Fault Tolerant Five Level Inverter with PWM Technique at fault condition	117.5	34.80

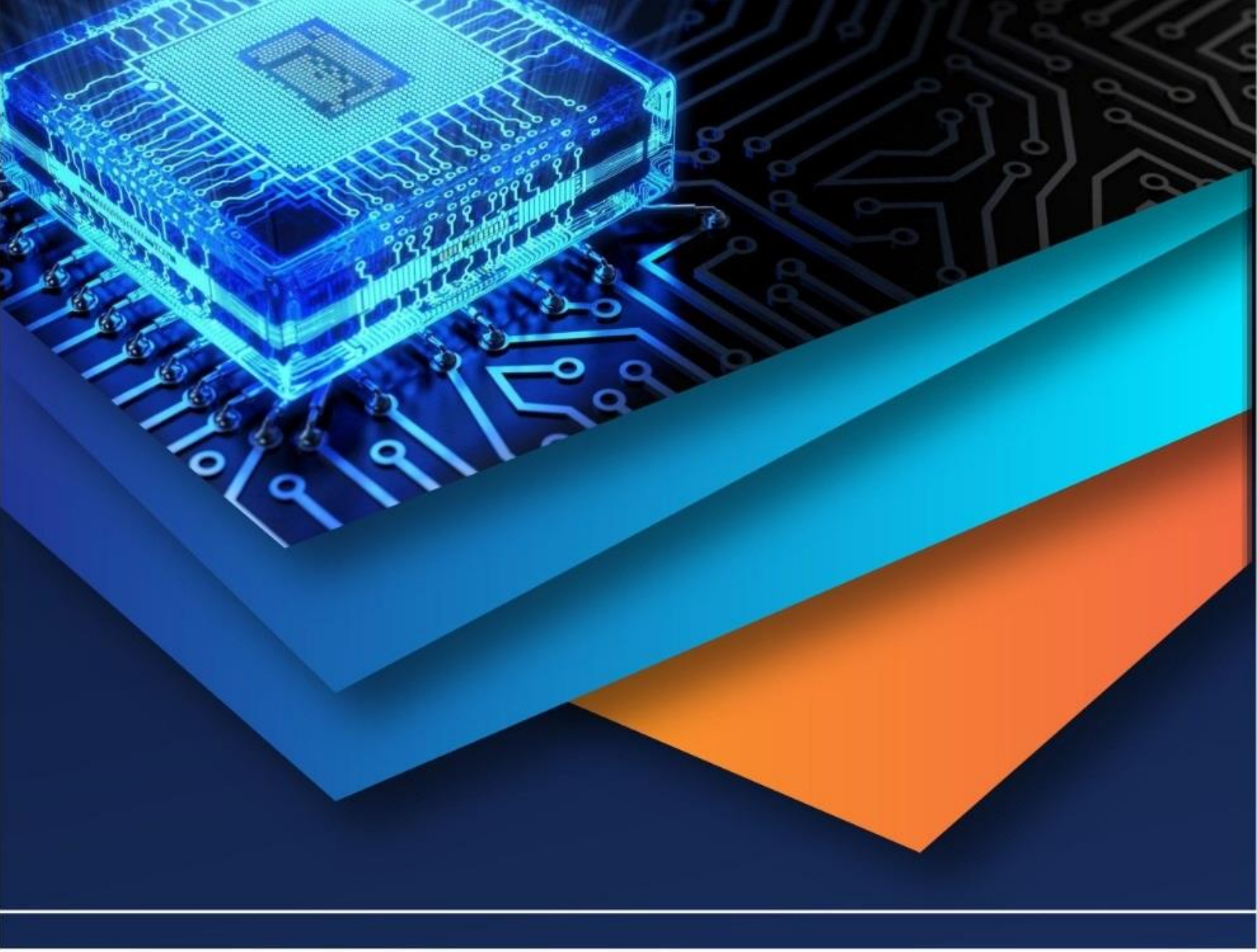
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IV. CONCLUSIONS

The results clearly demonstrate that traditional fault-tolerant five-level NPC inverters show noticeable performance decline when faults such as switch failures, diode malfunctions, or DC-link imbalances occur. These faults cause increased harmonic distortion, voltage imbalance, and disruption in output waveforms, limiting the reliability of the system in critical applications. On the other hand, the fault-tolerant NPC inverter controlled by PWM succeeded in dealing with fault conditions by adjusting the switching patterns and reassigning voltage levels to operating devices. Simulation and experimental results confirmed that the system guaranteed stability of the waveform, minimized THD, and sustained continuous operation even with hardware faults. This stable operation in tough conditions highlights the inverter's suitability to high-load applications like industrial motor drives and Grid systems. The control strategy, without adding significant hardware complexity, enhances the inverter's reliability and renders it a feasible and efficient.

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