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DC Booster with Voltage Multiplier for Renewable Energy Sources

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Abstract: ***An high step-up interleaved dc-dc converter is proposed for high efficiency and voltage gain applications. The configuration is proposed of modified two-phase interleaved boost converter with parallel-input series-output connections and a voltage multiplier module stacking on the output side. In the proposed converter, the parallel-input connection is used to share the input current and to reduce the conduction losses, while the series-output connection and voltage multiplier module are deployed to obtain the high voltage gain without operating at maximum duty ratio. In addition, the input current ripple is reduced due to the interleaved operation. The voltage stresses on the power switches are extremely lower than the output voltage such that the low-voltage-rated MOSFETs with low conduction resistor are available to reduce the conduction losses and to improve the conversion efficiency. Meanwhile, the output diode reverse-recovery problem is alleviated by the leakage inductance of the coupled inductors. Finally, the experimental results from a 1-kW prototype are given to validate the effectiveness of the proposed converter.***

Keywords: high step-up dc-dc converter, interleaved operation, voltage multiplier module, reverse-recovery problem.

I. INTRODUCTION

In renewable energy systems, such as photovoltaic (PV) and fuel cell generation systems, high voltage-gain and high- efficiency of dc-dc converters play a major role as a medium between the low output voltages of these sources and the utility grid. If the line voltage is at 220 V_{ac}, a 380-400V dc voltage bus is needed for the inverter. However, the output voltages of PV and fuel cells are actually ranged from 24 to 40 V due to the safety and reliability considerations. Thus, a dc-dc converter with a high voltage gain is required to boost the outputs of PV and fuel cells.

In general, a conventional boost converter can be deployed to provide a high voltage gain with a maximum duty ratio. However, it leads to large current ripple, high switching losses, severe output diode reverse- recovery problem and electromagnetic interference (EMI) problem. Moreover, the voltage stresses on the power switch and the output diode are equal to the output voltage, the high-voltage-rated MOSEFTs with large conduction resistance are necessary in the high output- voltage conversion system, which leads to large conduction and switching losses. These problems are the main limitations for the conventional boost converter. Commonly, the interleaved boost converter structure is deployed in high current applications to reduce/minimize the current ripple, reduce the size of the magnetic elements and increase the power level due to its advantages of current ripple cancellation and current-sharing performance.

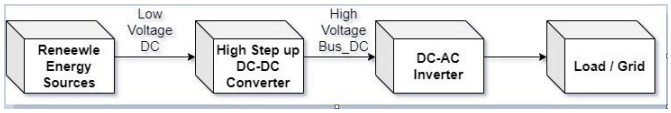


Fig.1. Diagram of renewable energy system.

In order to obtain high step-up voltage gain and high efficiency, many converter topologies have been proposed in the literature. Coupled inductor-based converters are good options for high voltage gain by changing the turns ratio of the coupled inductor. However, the leakage inductance of the coupled inductor causes power loss and high voltage stress on the power switches. The switched-capacitor converter can also achieve high voltage gain conversion. However, these converters require much number of switches, which leads to the complexity of the driving circuit. Some kinds of interleaved high step-up converter with voltage multiplier cells which consist of diodes and capacitors have been proposed. There are some advantages in these converters, such as lower voltage stresses on the switches and diodes, reduction of the input current ripple and high voltage conversion ratio without maximum large duty ratio.

An interleaved high step-up DC-DC converter with high voltage gain and high efficiency is proposed in this paper, which is eligible for power conversion in the renewable energy systems as shown in Fig.1. The proposed converter configuration is composed of modified two-phase interleaved boost converter with parallel-input series-output connection and a voltage multiplier module to achieve higher voltage gain as shown in Fig. 2. The voltage multiplier module is realized by the secondary windings of two coupled inductors and two switched capacitor. The power switches are driven in the interleaved fashion with half switching period shift. The advantages of the proposed converter are as follows.

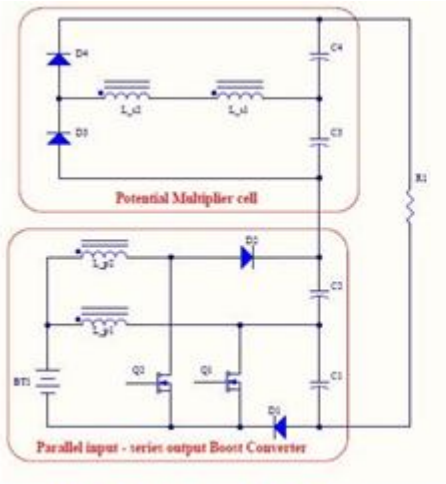
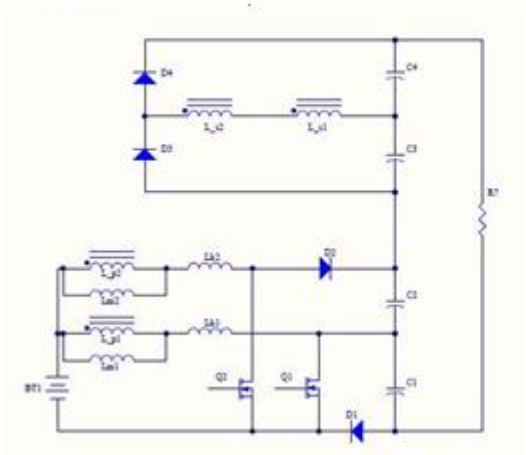


Fig. 2. Circuit schematic of the proposed



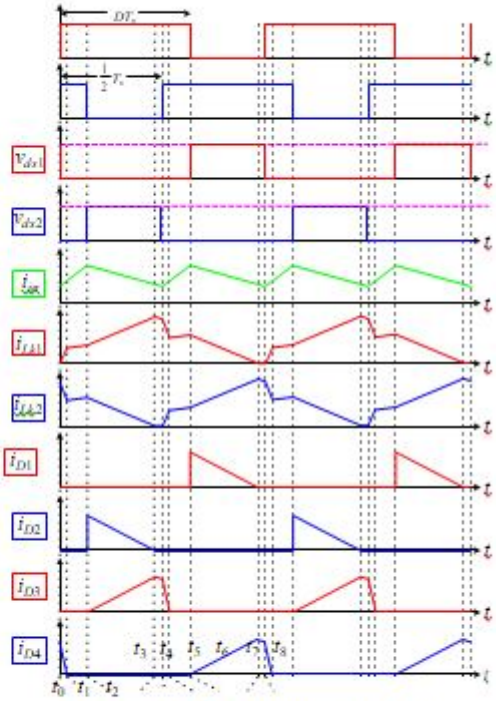


Fig. 4. Key waveforms of the proposed converter.

1) The proposed converter achieves high voltage gain without operating at extreme duty ratio.
2) The voltage stress on the power switches are greatly lower than the output voltage such that the low-voltage-rated MOSFETs with low conduction resistances can be used to reduce the conduction losses.
3) The parallel-input architecture can share the input current, reduce the conduction losses and handle large input current applications.
4) The input current ripple is decreased by the interleaved operation of the proposed converter, which can enlarge the lifetime of renewable energy sources.
5) The reverse-recovery problem of output diodes are alleviated due to the leakage inductances of the coupled inductors. The leakage energy of the coupled inductors is recycled such that the voltage spikes on the power switches are avoided and the efficiency is improved.

All these features show that the proposed converter is suitable for high voltage gain, high efficiency and high power applications. The experimental results on a 1-kW prototype circuit are provided to validate the performance of the proposed converter.

II. CONVERTER CONFIGURATION AND OPERATIONAL PRINCIPLE ANALYSIS

A. *Converter Configuration*

The proposed interleaved high step-up converter is shown in Fig.2. The configuration is composed of modified two- phase interleaved boost converter with parallel-input series- output connection and a voltage multiplier module stacking on the output side to achieve higher voltage gain. There are two coupled inductors in the proposed converter. The coupling references of the coupled inductors are denoted by the marks "∘ " and " □ " as given in Fig. 2. The coupled inductor is modeled as a combination of an ideal transformer with a turns ratio *n*, a magnetizing inductance and leakage inductance in this paper. The voltage multiplier module is realized by the secondary windings of two coupled inductors, two output diodes D_3 and D_4 and two switched capacitors C_3 and C_4 .

The equivalent circuit of the proposed converter is shown in Fig. 3, where L_{m1} and L_{m2} are the magnetizing inductances, L_{k1} and $L_{k\,2}$ are the leakage inductances, *n* is defined as the turns ratio N_s / N_p . S_1 and S_2 are the power switches. C_1 and C_2 are the output capacitors. D_1 and D_2 are the output diodes. The power switches S_1 and S_2 work in the interleaved mode with 180° phase shift and the same duty ratio. The duty ratio is greater than 0.5. The key waveforms are depicted in Fig. 4 when the proposed converter is operated in the steady-state and continuous conduction mode (CCM).

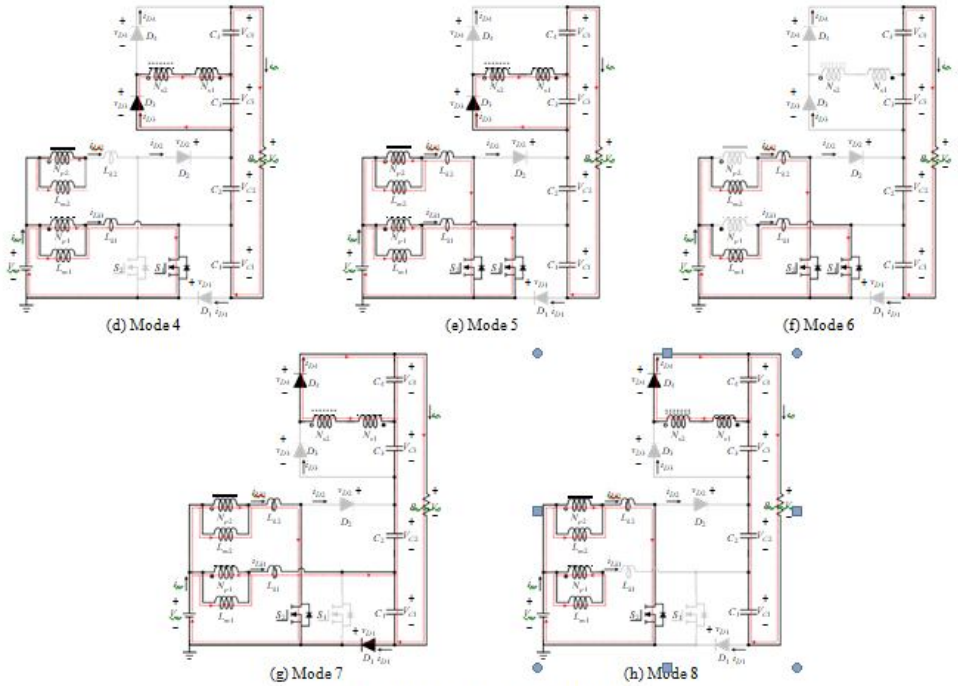


Fig. 5. Equivalent circuits of the modes 1-8.

Under the steady-state operation of the proposed converter, there are eight operational modes in a switching period. The equivalent circuits for each mode are shown in Fig. 5.

1) *Mode 1* [t_0 □ t_1]: At t □ t_0 , S_1 begins to turn on with zero-current condition, while S_2 remains in the turn-on state. The diodes D_1, D_2 and D_3 are reverse-biased, as shown in Fig. 5(a). i_{Lk1} increases quickly and its rate of increment is Fig. 5(a). i_{Lk1} increases quickly and its rate of increment is transfers to the secondary side of coupled inductors charging C_4 via D_4 when i_{Lk1} □ i_{Lm1}. The current through the diode D_4 decreases and its falling rate is controlled by L_{k1} and $L_{k\,2}$, which alleviates the diode reverse recovery problem of D_4 . This mode ends when i_{D4} decreases to zero and D_4 turns off.
2) *Mode 2* [t_1 □ t_2]: At t □ t_1 , S_1 and S_2 are in the turn-on state. All diodes are reverse-biased, as shown in Fig. 5(b). The magnetizing inductors L_{m1} and L_{m2} as well as leakage inductances L_{k1} and L_{k2} are linearly charged by V_{in}. The voltage stress on D_1 and D_2 is the voltage on C_1 and C_2 ,respectively. This mode ends when S_2 is turned off.

3) *Mode 3* [t_2- t_3]: At $t = t_2$, S_2 is turned off, which makes the diodes D_2 and D_3 turn on, as shown in Fig. 5(c). The energy stored in the magnetizing inductor L_{m2} is transferred to the secondary side of coupled inductors charging C_3 via D_3, meanwhile $i_{Lk\,2}$ flows through D_2 , C_2 and S_1 , so that C_2 is charged. The voltage stress on S_2 is clamped by $V_{C\,2}$. $i_{Lk\,2}$ decreases to alleviate the reverse recovery problem for D_2 . V_{in} , L_{m2} and $L_{k\,2}$ release energy to the output side. This mode ends at t_3 , when $i_{Lk\,2}$ decreases to zero and D_2 turns off.

4) *Mode 4* t_3 □ t_4]: At t □ t_3 , $i_{Lk\,2}$ decreases to zero and the diode D_2 turns off, as shown in Fig. 5(d). Thus, there is no diode reverse recovery losses for D_2 . The energy stored inL_{m2} is still transferred to the secondary side of coupled inductors. The current through S_1 is equal to the summation of i_{Lm1} and i_{Lm2}. This mode ends when S is turned on.

5) *Mode 5* [t_4 - t_5]: At $t = t_4$, S_2 is turned on with ZCS due to the leakage inductor L , while S remains in the turn-on state. The diodes D_1, D_2 and D_4 are reverse-biased, as shown in Fig. 5(e). i_{Lk2} increases with high rate. The energy stored in L_{m2} still transfers to the secondary side of coupled inductors charging C_3 via D_3 when $i_{Lk2} < i_{Lm2}$ .i_{D3} decreases and its current falling rate is controlled by L_{k1} and $L_{k\,2}$, which alleviates the diode reverse recovery problem for D_3 . This mode ends when i_{D3} decreases to zero and D_3 turns off.

6) *Mode 6* [t_5 □ t_6]: At t □ t_5 , S_1 and S_2 are in the turn-on state. All diodes are reverse-biased, as shown in Fig. 5(f). The magnetizing inductances L_{m1} and L_{m2} as well as leakage inductances L_{k1} and $L_{k\,2}$ are linearly charged by V_{in}. This mode ends when S_1 is turned off.

7) *Mode 7* [t_6 □ t_7]: At t □ t_6 , S_1 is turned off, which makes D_1 and D_2 turn on, as shown in Fig. 5(g). The energy stored in L_{m1} begins to transfer to the secondary side of coupled inductors charging C_4 via D_4. Meanwhile i_{Lk1} decreases and flows through C_1 and D_1. This mode ends at t_7 , when i_{Lk1} decreases to zero and the diode D_1 turns off.

8) *Mode 8* [t_7 - t_8]: At $t = t_7$, the diode D_1 turns off with zero-current condition, as shown in Fig. 5(h). There is no diode reverse recovery losses for diode D_1. The energy stored in L_{m1} is still transferred to the secondary side of coupled inductors. The current through S_2 is equal to the summation of i_{Lm1} and i_{Lm2}. This mode ends when the switch S_1 is turned on. The next switching period subsequently begins.

III. STEADY-STATE ANALYSIS

To simplify the steady-state analysis of the proposed converter in CCM, some assumptions are made as follows. The capacitances are sufficiently large, such that the voltages on the capacitors are considered as constant in one switching period. Two coupled inductors are considered to be identical, namely N_{s1} /N_{p1} = $N_{s\,2}$/$N_{p\,2}$ = n , $L_{m1} = L_{m2} = L_m$, $L_{k1} = L_{k\,2} = L_k$, and the coupling coefficient $k = L_m/(L_m + L_k)$.

A. *Voltage Conversion Ratio*

The voltages on the capacitors C_1 and C_2 can be calculated analogously to conventional boost converter, whichare given by

$$V_{C1} = V_{C2} = \frac{1}{1-D} V_{in} \qquad (1)$$

where D is the duty ratio of the switch. From aforementioned operational principle, the voltages $V_{C\,3}$ and V_{C4} can be derived from mode 3 and mode 7, respectively.

$$V_{C3} = V_{NS1} - V_{NS2} = nkV_{C2} = \frac{nk}{1-D} V_{in} \qquad (2)$$

$$V_{C4} = V_{NS2} - V_{NS1} = nkV_{C1} = \frac{nk}{1-D} V_{in} \qquad (3)$$

From (1)-(3), the output voltage is derived by

$$V_O = V_{C1} + V_{C2} + V_{C3} + V_{C4} = \frac{2nk+2}{1-D} V_{in} \qquad (4)$$

Therefore, the voltage conversion ratio is given by

$$\frac{V0}{Vin} = \frac{2nk+2}{1-D} \qquad (5)X$$

Due to the magnetizing inductances are much greater than the leakage inductances, the coupling coefficient *k* has only minor influence on the voltage conversion ratio. If the leakage inductances are neglected, then *k* is equal to one. The ideal voltage conversion ratio is obtained by

$$\frac{V0}{Vin} = \frac{2n+2}{1-D} \qquad (6)$$

Equation (6) shows that the proposed converter can achieve high voltage conversion ratio without an extreme duty ratio operation. Two degrees of freedom exist to enlarge the voltage gain by increasing the coupled inductor turns ratio and duty ratio. The ideal voltage conversion ratio versus the duty ratio under various turns ratio of the coupled inductors is shown in Fig. 6. As the turns ratio increases, the voltage gain is extended significantly.

B. Voltage Stresses on Power Devices

Assume that the coupling coefficient *k* equals one to simplify the analysis. Based on the operational principle, the

$$V_{S1} = V_{S2} = \frac{1}{1-D} V_{in} = \frac{1}{2n+2} V_0 \qquad (7)$$

$$V_{D1} = V_{C2} = \frac{1}{1-D} V_{in} = \frac{1}{2n+2} V_0 \qquad (8)$$

$$V_{D2} = V_{C1} + V_{C2} = \frac{2}{1-D} V_{in} = \frac{1}{n+1} V_0 \qquad (9)$$

$$V_{D3} = V_{D4} = V_{C3} + V_{C4} = \frac{2N}{1-D} V_{in} = \frac{1}{n+1} V_0 \qquad (10)$$

From (7)-(10), it can be seen that the voltage stresses on the switches and diodes are always lower than the output voltage. The relationship between the normalized power- device voltage stress and the turns ratio is drawn in Fig. 7. As the turns ratio of the coupled inductor increases, the switch voltage stresses decrease. As a result, the low-voltage-rated MOSFETs with low $R_{ds(on)}$ can be employed in the high voltage applications. The conduction losses and cost are reduced compared with the conventional boost converter.

C. Limitation of the Turns Ratio

For the correct operation, the duty ratio of the proposed converter should be exceeded than 0.5. Based on the voltage gain expression in (6), it can be concluded that the limitation of the turns ratio can be expressed as

$$n < \frac{V0}{4Vin} - 1 \qquad (11)$$

IV. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed converter, a 1000-W prototype with 40-V input voltage, 400- V output voltage and the switching frequency 40 kHz is built and tested with the parameters as follows.

L_{m1} , L_{m2} : 135 μH ; L_{k1} , L_{k2} : 1 μH ; C_1 ,C_2 ,C_3 ,C_4 : 100 μF ; D_1 , D_2 , D_3 , D_4 : DSEC60-03A; S_1 , S_2 : IRFP4227; n □ 1 .

The following experimental results from Figs. 8-11 aregiven under 1000-W full-load condition.

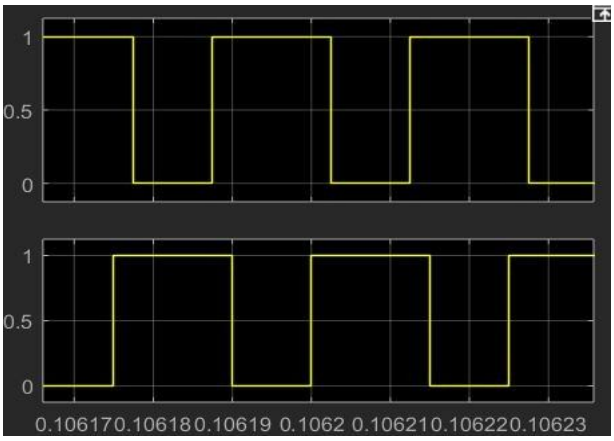


Fig. 8. Measured waveforms of v_{gs1}

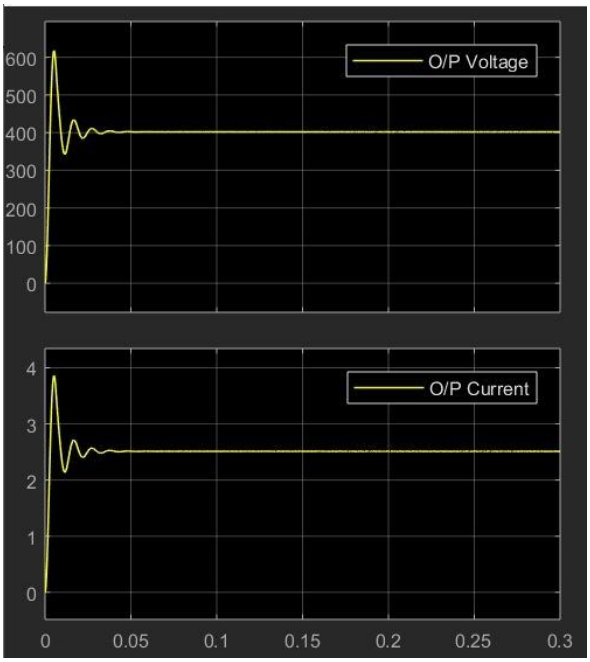


Fig. 9. Measured waveforms of output parameters

The measured waveforms of the gate signals $v_{gs}1$ and $v_{gs}\,2$, and the drain-source voltages v_{ds1} and $v_{ds}\,2$ are shown in Fig. 8. The extreme duty ratio existed in the conventional interleaved boost converter is avoided because the voltage gain of the proposed converter is extended. The switch voltage stress is about 100 V, which is only one-fourth of the output voltage. Therefore, low-voltage-rated MOSFETs with low $R_{ds(on)}$ are available to reduce the conduction losses.

Fig. 9 shows the measured waveforms of the input current i_{in} and the leakage inductance currents i_{Lk1} and i_{Lk2} with $i_{in} = i_{Lk1} + i_{Lk2}$. It can be seen that the input current ripple of i_m is much lower than those of i_{Lk1} and i_{Lk2} due to the interleaved operation.

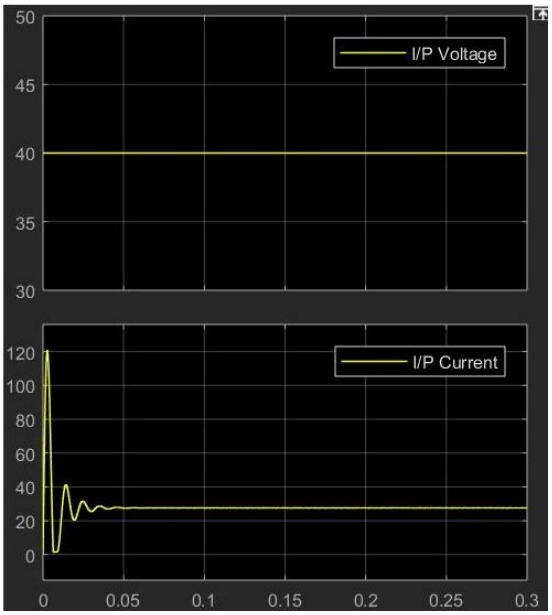


Fig.11. Measured waveforms of input parameters

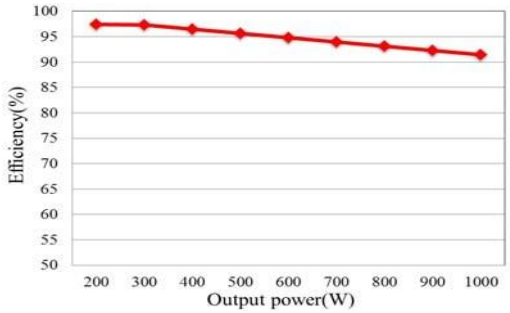


Fig.12. Measured efficiency versus the output power

The voltage and current waveforms on the diodes $D_1 \sim D_4$ are given in Fig. 10 and Fig. 11. It is shown that there is almost no reverse recovery current because the diode turn- off current is controlled by the leakage inductances of the coupled inductors. As a result, the reverse recovery losses are minimized and the EMI noise is suppressed compared with the conventional interleaved boost converter. Furthermore, the voltage stress on the diode D_1 is about 100V and that on the diodes $D_2 \sim D_4$ is 200V, which is consistent with the results of steady-state analysis and lower than the high output voltage.

Fig. 12 shows the experimental conversion efficiency at different loads measured by the power analyzer (HIOKI 3390). The maximum efficiency is around 97.44% at Po = 200 W. The full-load efficiency is appropriately 91.39%. The results show the proposed converter has high-efficiency conversion.

V. CONCLUSIONS

An interleaved high step-up DC-DC converter with parallel-input and series-output configuration and voltage multiplier module is proposed in this paper. The voltage conversion ratio can be greatly extended and the extreme duty ratio can be avoided in the high voltage gain applications. The switch voltage stress is much lower than the output voltage. As a result, low-voltage-rated MOSFETs with low on-resistance can be adopted to reduce the conduction losses. The input current ripple is reduced by the interleaved operation. The output diode reverse-recovery problem is alleviated by the leakage inductances of the coupled inductors to reduce reverse-recovery losses. Finally, a 1-kW prototype of the proposed converter is built to show the converter performance. The experimental results have demonstrated the proposed converter is suitable for the high voltage- gain and high efficiency applications.

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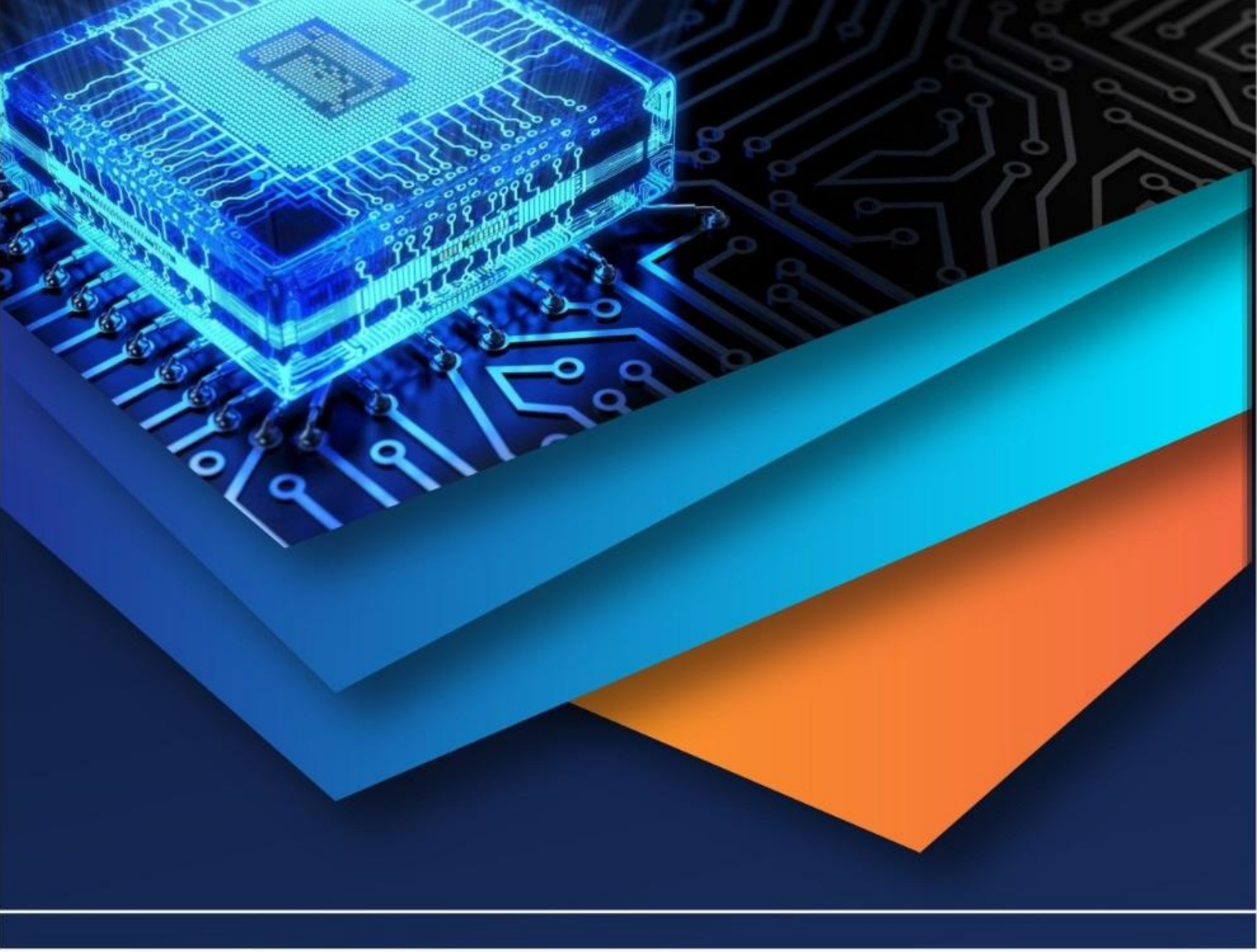

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