iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 14 **Issue:** IV **Month of publication:** April 2026

DOI: https://doi.org/10.22214/ijraset.2026.80490

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 14 Issue IV Apr 2026- Available at www.ijraset.com

Design and Analysis of Full Adder Using Pass Transistor Logic

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Abstract: ***There is a demand for high-performance and power-efficient arithmetic circuits in modern electronics has driven extensive research into full adder (FA) designs. This report presents the design, implementation, and comprehensive analysis of a low-power, high-speed hybrid full adder based on a 90nm CMOS process technology. The proposed system integrates separate optimized modules for SUM and CARRY generation to achieve superior performance by leveraging the strengths of different logic styles. Specially, this work details a 14-transistor(14-T) hybrid FA cell that combines the advantages of Pass Transistor Logic (PTL) and Gate Diffusion Input (GDI) techniques. The primary objective is to minimize power consumption, reduce propagation delay, and decrease the overall Power-Delay Product (PDP), which are critical metrics for applications in contemporary VLSI systems.***
Keywords: PTL, PDP, Full-Adder, CMOS.

I. INTRODUCTION

Adders are basic components of digital systems and are they are very important in arithmetic and logic units(ALUs), microprocessors, digital signal processors, and other VLSI applications. Among various adder designs, the full adder is one of the most basic one because it adds two binary bits and a carry input, and produce sum and carry as output. As in CMOS technology, power dissipation and area optimization have become important design factors in modern VLSI designs. Whereas in standard CMOS logic circuits, they often lead to increase in transistor count, increase in power dissipation and delay. So, we proposed pass transistor logic method, which helps to reduce the transistor count needed for implementing logic functions by allowing inputs to drive source/drain terminals rather than gate terminal, thus reducing switching activity and circuit complexity. In this paper, a full adder circuit using pass transistor logic(PTL) is designed and analysed using cadence virtuoso software. The proposed design will focus on achieving better performance in terms of reducing power dissipation and size of area, with acceptable speed characteristics. The performance of the full adder designed using pass transistor logic(PTL) is calculated with parameters like power dissipation, propagation delay, and number transistors used. Both CMOS full adder and full adder using pass transistor logic(PTL) is compared and differentiated with results and outputs.

II. LITERATURE REVIEW

Researchers like R. Zimmermann and W.Fichtner have discussed the benefits of reducing transistors and demonstrate the pass transistor logic can lower power consumption compared to conventional designs[5].

Singh et al. have described a full adder circuit based on pass transistor logic that provide lower power consumption and delay, when compared to CMOS logic, also explained difficulties of threshold voltage drop and signal degradation[4].

Recent developments in hybrid logic solutions have combined pass transistor logic and CMOS to optimize performance and output quality[3]. Practically a hybrid PTL/full-swing adder implementation results improve in speed and full voltage swing at larger area. In addition, transistor-level optimization methods are considered for further improvement in performance of pass transistor logic(PTL) in nanoscale technology[1].

The fact is that most designs have shown significant improvements, like power consumption, delay and output swing. Which aims to calculate efficiency of pass transistor logic(PTL) full adder design simulated in cadence virtuoso software by assessing power consumption, delay, and transistor usage.

Weste and Harris provides a comprehensive CMOS VLSI design methodology[7].

Chandrakasan et al. discuss low-power design techniques

Yin et al. and Yadav et al. demonstrate pass transistor logic(PTL) full adders in 90 nm and 45 nm technologies[6].

Sonawanediscuss present energy-efficient pass transistor logic(PTL) designs with improved speed and reduced transistor count[9].

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III. EXISTING METHOD

In VLSI design, the full adder circuit is typically designed using static CMOS logic, which use complementary pull-up and pull-down networks in performing sum and carry operations. This design approach results in full voltage swing, large noise margins, and robustness. Even though it has disadvantages, the CMOS full adder circuit has been extensively used for its few advantages in arithmetic circuits of digital systems.

However, to get area and power efficiency, transmission gate logic(TGL) has been used as an alternate design to static CMOS logic. The full adders designed using transmission gate logic used for efficient logic levels.

The common method to generate output is to generate CARRY out and its complement. Then signals are used for 2to-1 multiplexer which generates the SUM output. This structure is more efficient and typically need 28 transistors. The PUN and PUD are designed to be complementary, for given input combination, with always low resistance path from output to VDD or GND.

The standard Boolean expressions are:

Sum = A ⊕ B ⊕ Cin,

Carry = A B + B Cin + A Cin.

A. Basic full adder

Architecture of a basic full adder contains 3 inputs A, B, Carry in, and outputs Sum and Carry. Basic truth table of full adder is shown below:

TABLE I. Truth table for basic full adder.

A	B	Cin	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

B. Structural simulation of CMOS full adder

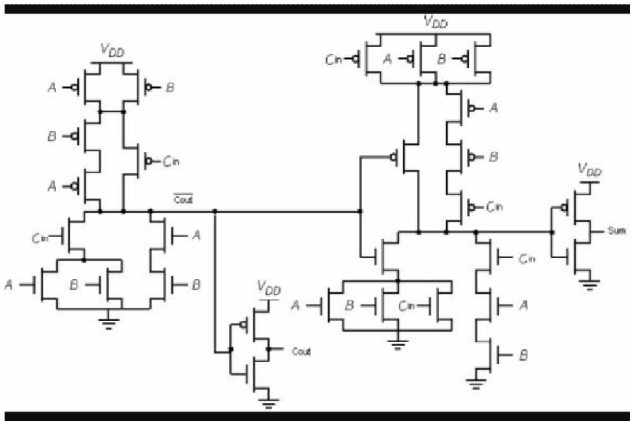


Fig. 1. Basic circuit of CMOS full adder with 28 transistors.

Negativity of this CMOS full adder is, it requires more spacing of silicon area, and it requires more power consumption and not much efficient in output threshold voltage.

Particularly the standard 28-transistor (28T) static CMOS implementation, are known for their robustness and full-swing output.

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However, they are inefficient in terms of transistor count, silicon area, and power consumption.CL is known for its high speed operation and logic is formed by fast NMOS transistors. Output inverters make full voltage swing and make it suitable for cascading in larger VLSI structures. The large number of transistors, especially the slower PMOS transistors in pull-up network, leads to significant switching capacitance and limits the operational speed. Other logic styles, such as complementary pass-transistor logic (CPL), offer high speed but cost of even higher transistor counts. The problem is that to design a full adder that reduces the transistor count and power consumption compared to conventional designs, maintaining competitive performance and without introducing design complexities.

The conventional method for designing a full adder is used for comparison, Complementary metal-oxide semiconductor (CMOS) logic style. This design directly implements the Boolean equations for SUM and CARRY out using a pull-up network (PUN) of PMOS transistors and a pull-down network (PDN) of NMOS transistors. To create a low-power VLSI circuit, we must navigate to atrade-offs with power, performance (speed), and area(PPA).

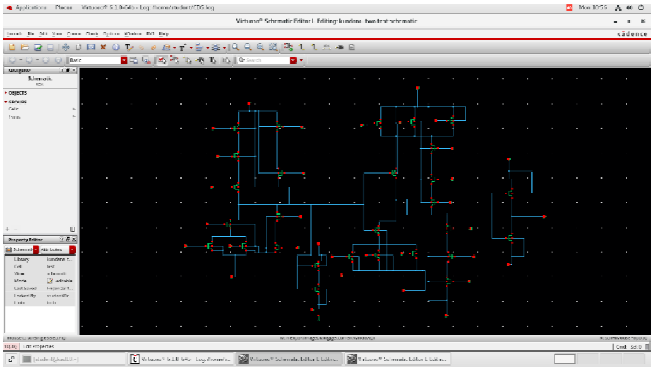


Fig. 2. Schematic circuit of CMOS full adder in Cadance Virtuoso

C. Obtained results in CMOS full adder.

The CMOS full adder is simulated with values estimated for a 180nm CMOS technology operating at 1.8v and 90nm technology also operating at 1.8v.

Power consumption is up to (15-25µW) and propagation delay of range (250-300 ps).

In performance analysis and limitations, with 28 transistors, the circuit occupies large silicon area, which effects increases manufacturing cost also contributes to higher static power consumption due to leakage current of all transistors. High power consumption, large number of transistors, the wider PMOS transistor required for symmetric switching, leads to high input and internal capacitance. Operational speed is often limited by critical path, as the low mobility of holes in PMOS transistor are slower than the pull-down path.

TABLE II. Outputs of CMOS in different Technologies (nm).

CMOS Full adder	180 nm	90 nm
Transistor Count	27	27
Delay(ns)	70	60
Power Consumption(µW)	487.549	409.865
VDD (V)	1.8	1.8
PDP	98.989fJ	90.413fJ

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 14 Issue IV Apr 2026- Available at www.ijraset.com

IV. PROPOSED METHODOLOGY

It offers an optimized design for a full adder circuit using pass transistor logic (PTL) to achieve low power dissipation and transistor count with acceptable speed and functionality. In proposed method logic functions are implemented by simply allowing input signals to control source and drain terminals.

The sum and carry outputs of full adder circuit are simulated with reduced number of transistors compared to conventional CMOS. The sum is obtained using a pass transistor (PTL) based XOR-XNOR circuit, while carry is obtained using combination of pass transistor networks based on logical expression with low hardware. Which logic functions are better in achieving a compact circuit implementation.

Threshold voltage degradation is major and common problem in existing method, to overcome these the proposed design develops transistor sizing and logic structuring.

The simulation results exhibits that the proposed full adder circuit using pass transistor logic (PTL) has low power dissipation and area sizing, with comparable delay, making it ready for low-power and area efficient VLSI designs, particularly in arithmetic-intensive digital systems.

A. Circuit block diagram, schematic structure and symbol created in Cadance Virtuoso software.

1) Transistor count is reduced 50% compared to CMOS full adder

2) Power and Delay also reduced to improve efficiency.

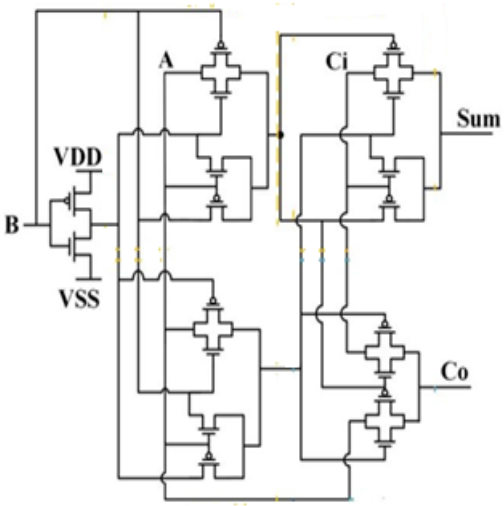


Fig 3. Block Diagram of PTL full adder

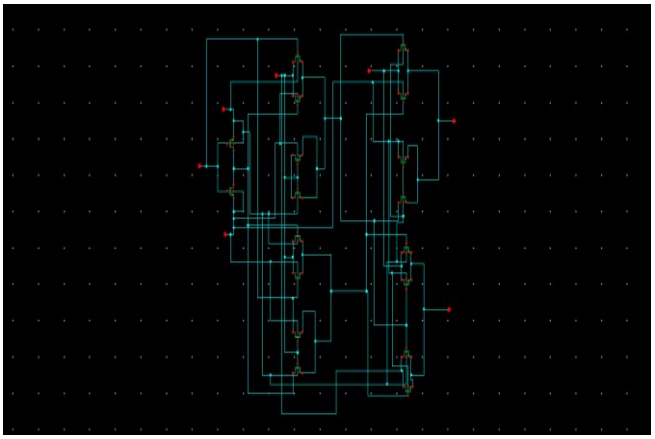


Fig 4. Schematic structure designed in Candance virtuoso.

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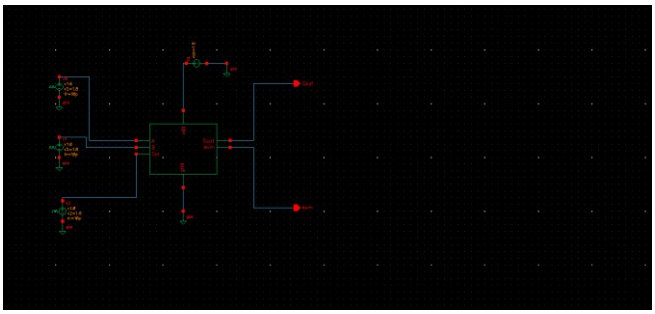


Fig 5. Symbol created with designed schematic circuit for PTL full adder.

B. Simulation process of PTL full adder

Calculation part of finding average power and delay with respect to PDP and TDP in pass transistor logic (PTL) full adder

1) Schematic Implementation

Open cadence virtuoso-create schematic-place NMOS and PMOS transistors according to PTL full adder design-write inputs A, B, Cin and outputs SUM, CARRY-connect Vdd(supply voltage) and GND-use voltage source (Vdc + Vpulse) for inputs-Vdc for constant supply-Vpulse for switching simulation.

2) Simulation Setup

a) Transient Analysis

Open ADE-setup-Analyses-transient-set tstop (e.g., 50 ns) to cover multiple input transitions- use vsource pulse for A, B, Cin with suitable period & rise/fall times-run simulation and observe waveforms.

b) Power Analysis

Measure average power consumption-in ADEtools-simulator-set up output variables-use i(Vdd)*v(Vdd) to calculate instantaneous power.

c) Propagation Delay

Measure delay from 50% input transition to 50% output transition-note max delay among all transitions.

3) Technology/Environment

Set technology library(180 nm or 90 nm)-ensure simulation temperature 27°C-use minimum sizing as per PTL design. Also try technology 45 nm to get exact output configuration and may get exact simulation results.

C. Formulas used to obtain values.

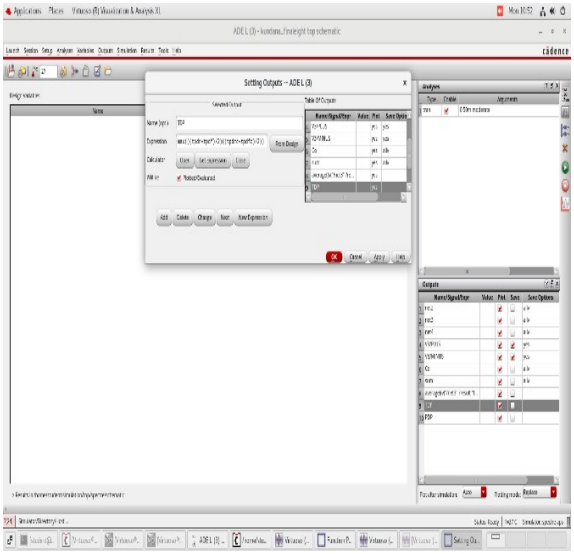


Fig. 1.TDP formula

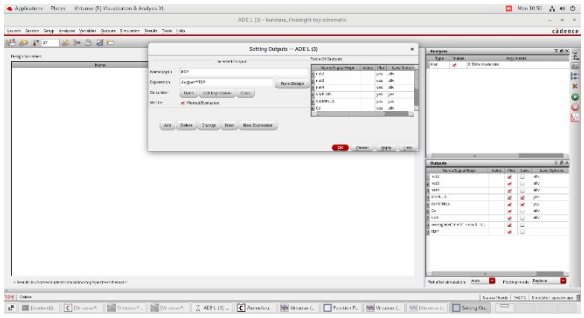


Fig. 2.PDP formula.

Figures show the formulas used to calculate TDP and PDP (Power-Delay Product) using obtained average power and with obtained pulse waveforms.

V. SIMULATION RESULTS

The simulated waveforms show that the proposed full adder generates the sum and carry as per the truth table. The output transitions shows the full adder is free from glitches and works in a stable manner. Also transistor sizing is done in such a way that the voltage levels are acceptable at output, problem of threshold voltage degradation is common in pass transistor logic.

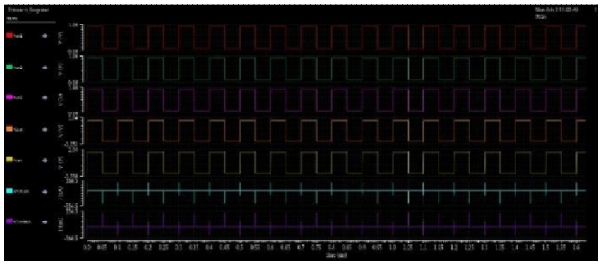


Fig 6. Waveforms of pass transistor logic (PTL) full adder

Power analysis was calculated by average power dissipation during switching activity. In proposed PTL full adder few transistors are used and low switching capacitance, power dissipation is much lower compared to CMOS circuit.

The transistor count of proposed pass transistor logic (PTL) full adder is decreased by almost 50%. This directly affects average power dissipation, decreased one. Also delay, and in some cases even better than the existing circuits due to decrease in capacitances.

The power-delay product (PDP) values show better energy efficiency for both technologies. Though there is a slight degradation in threshold voltage due to pass transistors, output voltage swing is still in limits, which helps making it suitable for cascading in larger arithmetic circuits.

The results declare that proposed pass transistor logic (PTL) full adder circuit provides optimal trade-off between power, delay, and area, which is suitable for low-power VLSI applications.

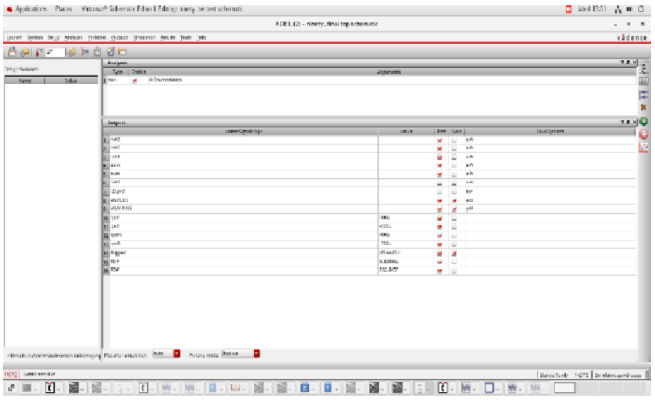


Fig 7. Power and delay outputs for PTL full adder in Cadance virtuoso.

VI. CONCLUSION

In this work, design and analysis of a pass transistor logic (PTL) based full adder using cadence virtuoso tool. Proposed design targets reducing power and area while satisfying performance, thus applicable for modern low-power VLSI design. This report gives complete analysis of a next generation full adder using pass transistor logic (PTL). Primary objective is to develop a cost-effective, highperformance, low-power full adder.

The simulation performed on 90 nm CMOS processes and proposed PTL full adder provides improvement in average power and power-delay product (PDP) compared to conventional CMOS. Also the reduced number of transistors results in lower switching capacitance. To overcome limitations of a conventional designs pass transistor logic (PTL) is introduced. This facilitates a significant reduction in transistor count, which directly leads to smaller silicon area and lower over all switched capacitance, resulting in reduced dynamic power dissipation.

Power–Delay Product (fJ)

PDP=Average Power (W)×Propagation Delay (s).

TABLE III. Comparing of CMOS and PTL in Technology 180 (nm)

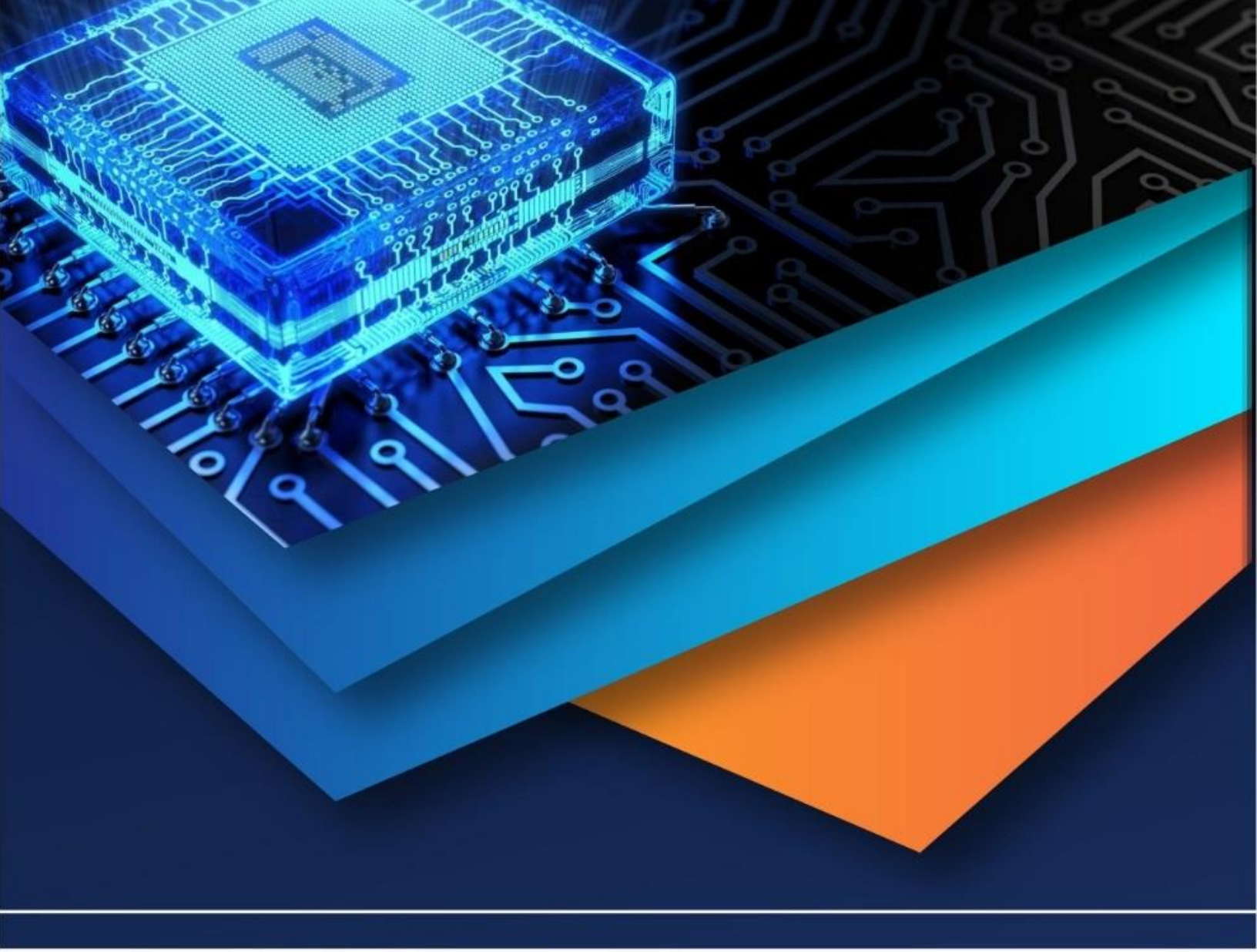
Parameters	CMOS	PTL
Technology (nm)	180 nm	180 nm
Width of Transistor (nm)	120	120
Supply Voltage (V)	1.8	1.8
Delay(ns)	70	37
Power Consumption (μW)	487.549	35.015
Number of Transistors used	27	18

Though PTL may cause a slight drop in threshold voltage, but it has proper circuit design and transistor sizing which ensure proper output voltage. Future research may include extension of proposed design, implementation of level restoration methods for improved voltage swing, and performance on advanced technology nodes.

REFERENCES

[1] V.V. Kumar and V.V. Nandha, Design and simulation of high-speed hybrid-logic full adder. International journal of engineering trends and technology, 2014, pp.191-195.
[2] S. Lakshmi, C. Meenu Raj, D. Krishnadas, Optimization of hybrid CMOS designs using a new energy efficient 1 bit hybrid full adder, ICCES, 2018, pp.905-908.
[3] H. Naseri, S.Timarchi, Low-power full adder by exploring new XOR and Xnor gates, IEEE trans, VLSI syst, 2018, pp.1481-1493
[4] S. Singh, T. Sharma, K. G. Sharma, and B. P. Singh, “PMOS based 1-Bit Full Adder Cell”, 2012, international journal of computer applications 975.
[5] R. Zimmermann and W. Fichtner, ”Low-Power logic styles: CMOS versus pass-transistor logic”, 1997, pp.1079-1090.
[6] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, ”Low-power CMOS digital design”, IEEE journal of solid-state circuits, vol. 27, no. 4, p.473-484, Apr. 1992
[7] Cadence Design Systems, Cadence Virtuoso® User Guide, Cadence Design System, Inc., USA.
[8] S. Nuthalapati, C. Jyothirmayi, G. Saikiran et al., “Design of various low power and high speed full adder designs using 45 nm CMOS technology,” Zenodo, Apr. 2022.

[9] A. Yadav, P. Sonawane, and S. Mane, “Design and analysis of a low-power full adder in 90-nm CMOS technology,” May 2025, pp. 3624–3630.
[10] A low-power full adder for embedded architectures- Fayed & M.A. Bayoumi, Proc. IEEE int. Symp. Circuit Syst.,2001.\
[11] C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang, “A Low-Power High-Speed Hybrid CMOS Full Adder for Embedded Systems”, Proc. IEEE Design Diagnostics Electron. Circuits Syst., Apr. 2007.
[12] “Low Power Pass-Transistor Logic Based Full Adder and 8-Bit Multiplier”, MDPI Electronics, 2023 — discusses PTL full adder design principles.
[13] “XNOR-XOR based Full Adder Using Double Pass Transistor Logic”, IEEE Conference Publication.
[14] “Hybrid Full Adder Circuit Utilizing Pass Transistor Logic and PFAL Logic”, Nilam et al. (HSBPVTs College of Engineering).
[15] “Investigation on Performance of High Speed CMOS Full Adder Circuits”, K. Kalyani & G. Vasanth Rao.
[16] C. Mead & L. Conway, Introduction to VLSI Systems — foundation for transistor-level logic design.
[17] J. G. Reddy, "Analysis of CMOS Full Adder Circuits for Multiplier Logic Architectures," International Conference on Distributed Computing and Optimization Techniques (ICDCOT), Bengaluru, India, 2024, pp. (1-5).



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