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Design and Implementation of 1-bit Full Subtractor Using FinFET

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Abstract: ***A full subtractor is a digital combinational circuit that performs subtraction involving three bits, namely A (minuend), B (subtrahend), and Bin (borrow-in) . It accepts three inputs: A (minuend), B (subtrahend) and a Bin (borrow bit) and it produces two outputs: D (difference) and Bout (borrow out). Unlike a half adder, which adds only two binary digits and produces a sum and carry, a full adder considers an additional carry input from a previous less significant bit addition. The full adder's design includes three inputs: A, B, and Cin (carry-in), and two outputs: Sum (sum) and Cout (carry-out). The sum output Sum is derived by XOR-ing the three inputs, while the carry-out Cout is obtained by considering the majority function of the inputs. This means Cout is set when any two or more of the three inputs are high (logical 1). Full subtractors are fundamental components in the construction of arithmetic logic units (ALUs), binary adders, and other computational circuits in digital systems, enabling the handling of multi-bit binary addition by cascading multiple full adders.***

I. INTRODUCTION

The increasing demand for portable, battery-powered devices such as laptops, wristwatches, mobile phones, calculators, and Internet of Things (IoT) gadgets has made power consumption in digital electronic circuits a significant concern. In modern very largescale integration (VLSI) applications, like microprocessors and digital signal processors (DSPs), arithmetic operations such as addition and subtraction are fundamental.

These operations rely heavily on adders and subtractors, which are essential components in digital systems. Full adders and subtractors play a crucial role in the architecture of DSPs and microprocessors. Efficient implementation of Arithmetic Logic Units (ALUs) and floating-point units, which utilize full adders and subtractors, is vital for executing specialized algorithms, especially in low and ultra-low voltage systems.

This paper the full subtractors are designed in various techniques and technologies. The project is aiming to analyse the delay and power characteristics of 10T full subtractor in different techniques and technologies. Finally, we conclude that which is the best design for applications.

II. LITERATURE SURVEY

1) Pakniyat et al. (2018) proposed “Design of High performance and Low Power 16T Full Adder Cells for Subthreshold Voltage Technology”. This paper focused about two new structures of 1–bit full adder circuits suitable for sub-threshold voltage. Comparison has been carried out for propagation delays, power dissipations, PDP, and EDP in sub threshold regime

2) Kumar and Baghel (2017) proposed a paper on “energy efficient single-bit hybrid full adder circuit” for ultra low voltage applications. In this work, a 1-bit full adder (FA) circuit is designed by employing CMOS based XNOR modules and Pass Transistor Logic (PTL) logic for sum and carry generations.

3) Mehr et al. (2006) presented a paper on “Novel power efficient 12T full Adder”. The proposed adder is operated at 1 volt supply with power consumption of 1.894 µW at 90 nm technology

4) Vijayakumar et al. (2019) outlined the leakage currents in SRAM circuits for low voltage applications. From that research it has been observed that the maximum effort lay on binary arithmetic circuits with less number of transistors.

III. AIM, OBJECTIVES, AND ADDITIVE CIRCUIT

A. Aim

The main aim of the project is to reduce power and delay and compare the design parameters of various transistor technologies of full subtractors.

B. Objectives

The objectives of the project are

1) To Desigd and implement efficient full subtractor using 10T FinFET technology in Cadence Virtuoso tool.
2) Measurement of parameters of the designed full subtractor in FinFET technology.
3) Measurement of parameters of the designed full subtractor with (20,14,10) Transistor Technology.
4) comparison of results of the measured parameters of designed and simulated full subtractor.

C. Subtrctive Circuit:

The Subtractive circuit that we are using to the project is 10T FINFET full subtractor. FINFET stands for Fin Field-Effect Transistor which is a type of 3D Transistor used in modern semiconductor devices for improved performance and lower power consumption. FINFETs have better control over the channel, reducing short-channel effects that are common in traditional MOSFETs.

IV. SOFTWARE USED

Cadence Virtuoso is a prominent Electronic Design Automation (EDA) solutions provider, offering a comprehensive suite of tools for analog, mixed signal and integrated circuit (IC) design. It provides a suite of tools and features that enable us to process the design from initial schematic capture to final layout and verification.

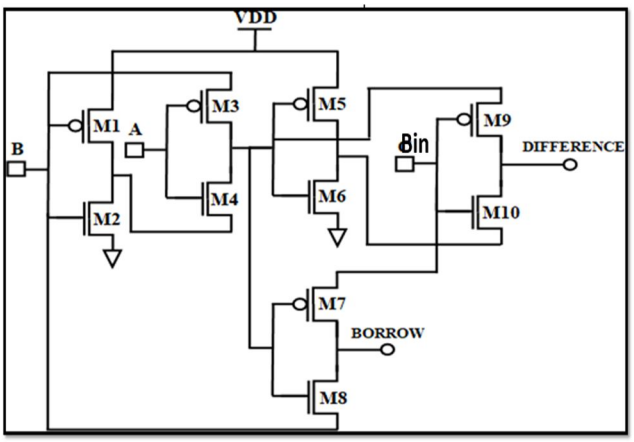
The Key features of Cadence Virtuoso are Schematic Capture, Layout Editor, Simulation and Analysis, Design and Rue Checking, Physical Verification, Parametric Analysis and Custom Design.

The Advantages of Cadence are:

1) Miniaturuzation
2) Powerful routing tools
3) Advanced process node support
4) Customization and Automatiom
5) Extensive verification and validation.

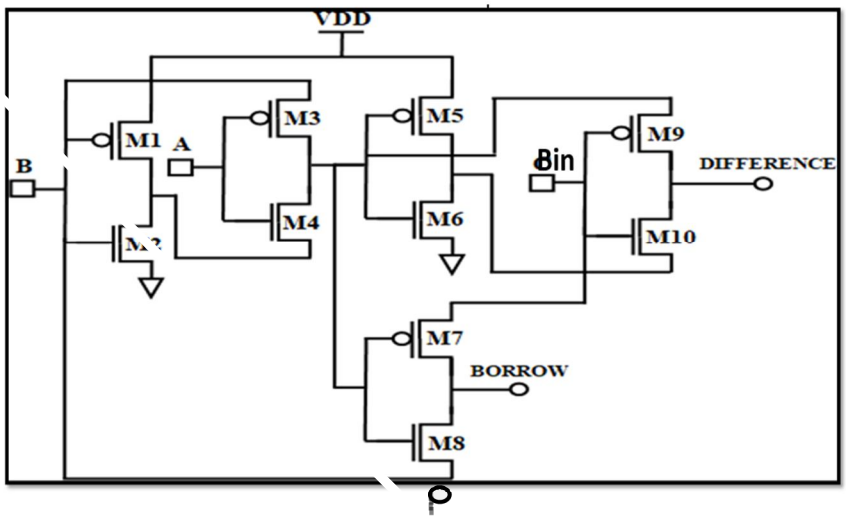
V. BLOCK DIAGRAMS

A. 10T FinFET full subtractor



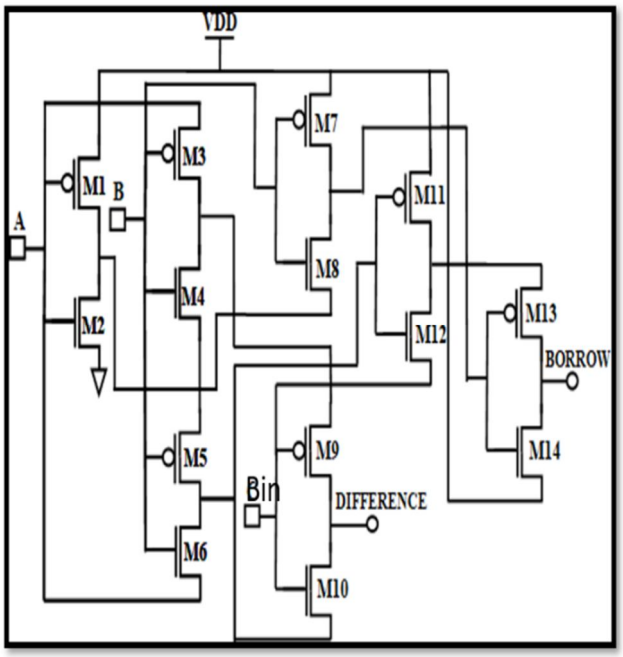
A 10-transistor FinFET full adder as shown above at 45nm leverages superior leakage and short-channel control for faster switching, lower power, and reduced area compared to planar CMOS. This efficient design benefits low-power, high-performance applications in mobile and compact VLSI systems, showcasing FinFET's potential in modern IC design**.** Fin Field-Effect Transistor, is a type of 3D transistor architecture used in modern semiconductor devices. Traditional planar transistors, which have been the standard for many years, are reaching their physical and performance limits as semiconductor technology scales down to smaller nodes. FinFET technology addresses these challenges by introducing a three-dimensional structure

B. 10 T CMOS full Subtractor



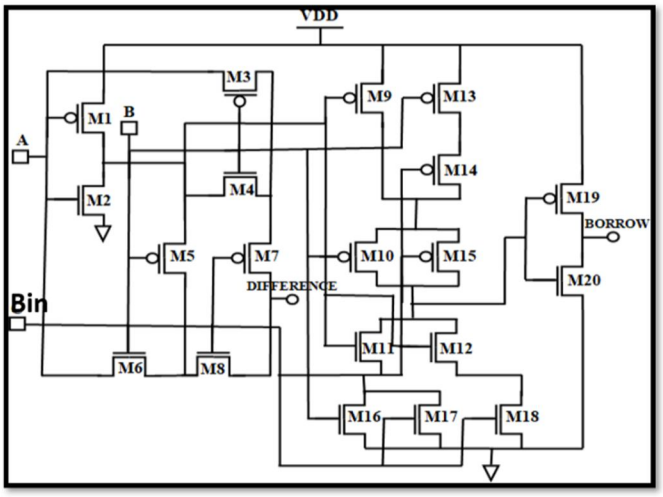
A 10T full subtractor design in above diagram utilizes XOR gates and a multiplexer for reduced transistor count compared to prior designs (14T and 20T). Implemented with transistors as shown in Figure 6, XOR gates and the multiplexer efficiently generate difference and borrow outputs. The multiplexer selects B or Bin based on the first XOR output for borrow. This design achieves similar functionality to a 1-bit full adder with fewer transistors as shown in Figure 7. Simulations as shown in Figure 8 are needed, but this approach is promising for reducing transistor count in full subtractors.

C. 14T CMOS full subtractor



A 14-transistor (14T) full subtractor (OBFS) design in Figure 2 utilizes XOR-XNOR modules with feedback topology and a 2x1 multiplexer to achieve full-swing outputs. The feedback topology and multiplexer interaction enable efficient borrow generation with a low transistor count. Analysis and simulations can assess its effectiveness in transistor reduction, high performance, and full-swing outputs. This aligns with trends in compact and efficient IC design.

C. 20T CMOS full Subtractor



20T full subtractor design reduces transistor count compared to 34T C-CMOS. This offers smaller chip area and potentially lower power. Design allocates: 6T for difference, 10T for borrow, and 4T for inversion. Analysis/simulations needed to evaluate effectiveness in transistor reduction, power, and functionality. Aligns with compact, low-power IC design trends. The OBFS circuit which consists of 14 transistors by employing XOR-XNOR modules and a 2 × 1 multiplexer is shown in Figure 3. The XOR-XNOR module is based on feedback topology and able to produce full swing output voltage both at difference output and output borrow. The pre layout timing waveform of the designed OBFS is shown in Figure 4. The inclusion of multiplexer unit is able to achieve higher performance with reduced transistor count. Totally 12 transistors were in the part of difference output and multiplexer is able to generate borrow output in correspondence with feedback network.

VI. SCHEMATIC DESIGN AND SIMULATION RESULTS

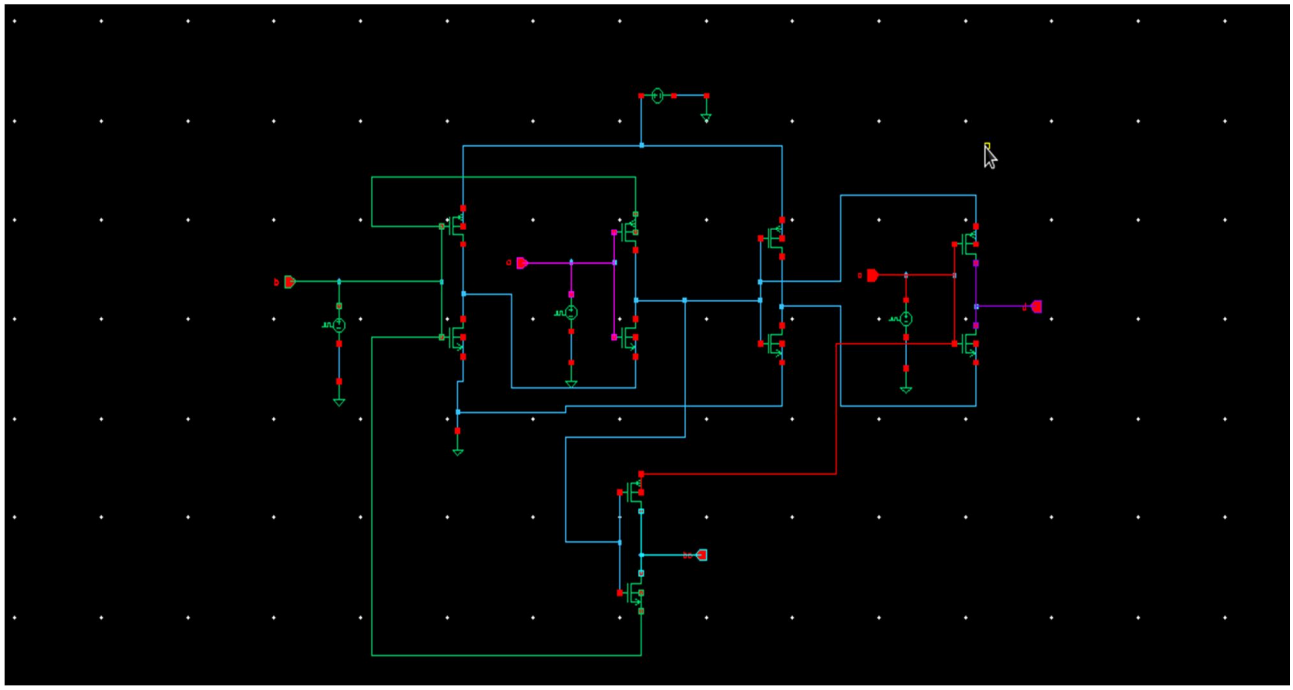


Fig 1. Schematic of 10TFinFET Full Subtractor

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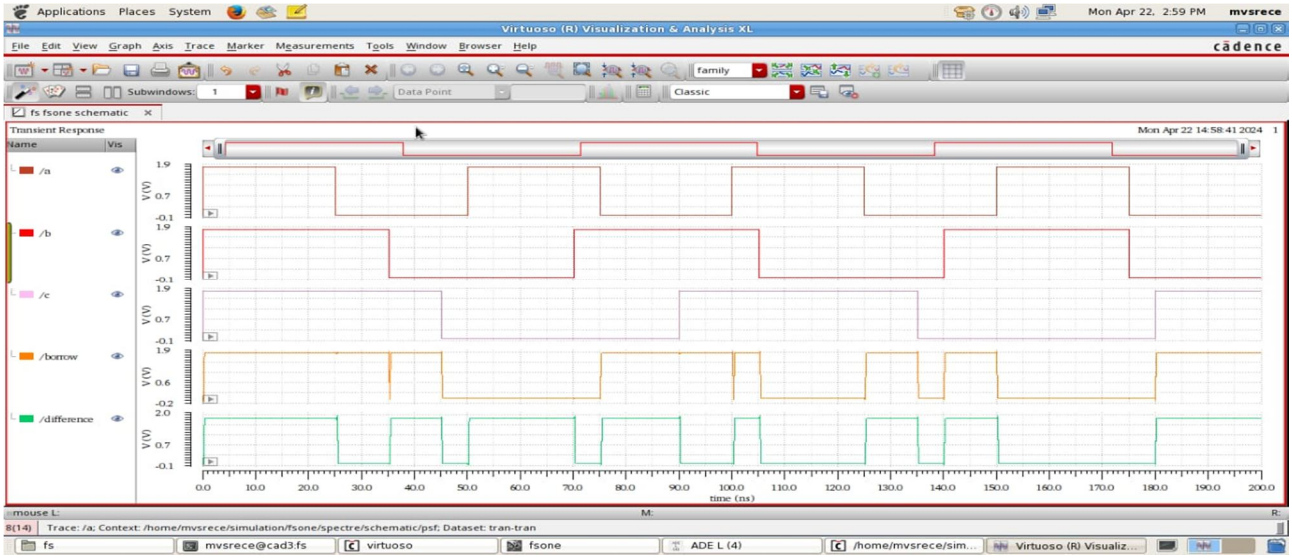

Fig.2 Output of 10T FinFET full subtractor

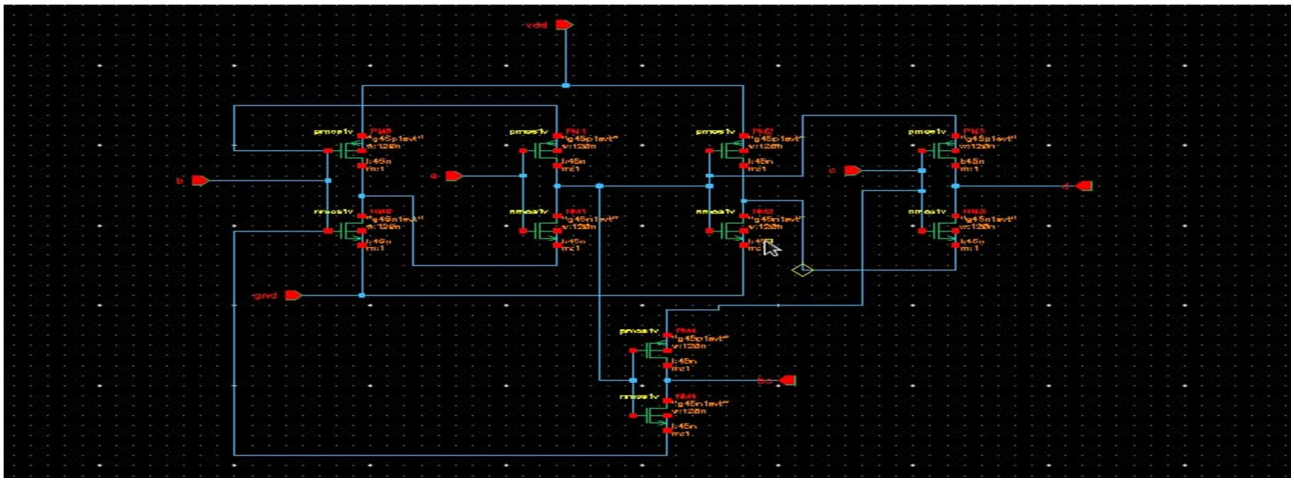

Fig.3 schematic of 10T Full subtractor

Fig.4 Output of 10T Full subtractor

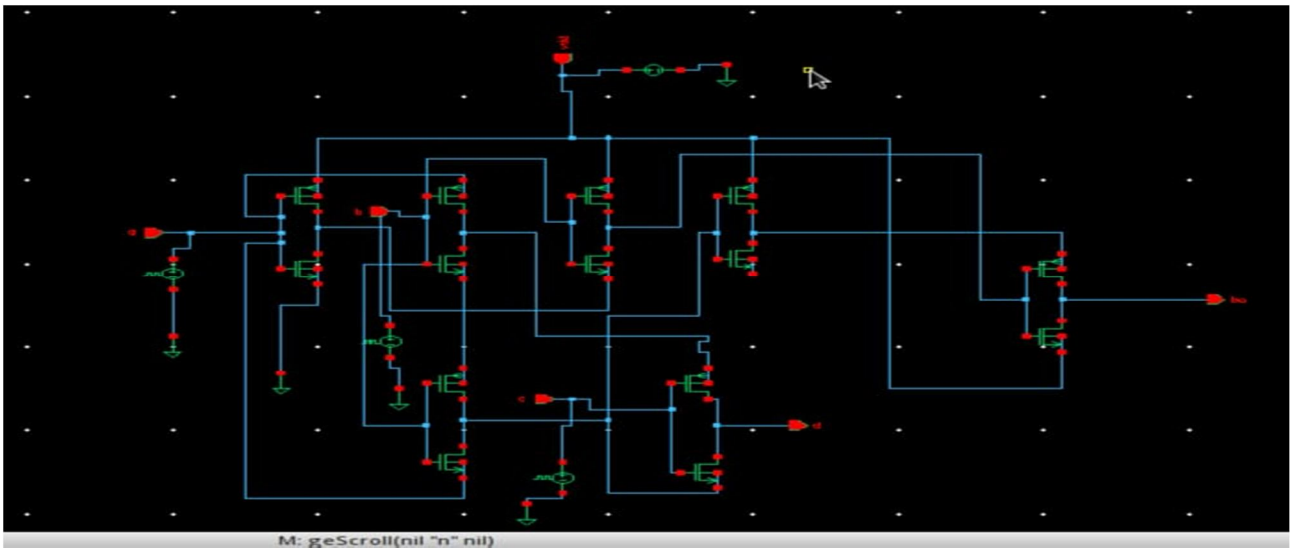

Fig.5 schematic of 14T Full subtractor

Fig.6 Out of 14T Full subtractor

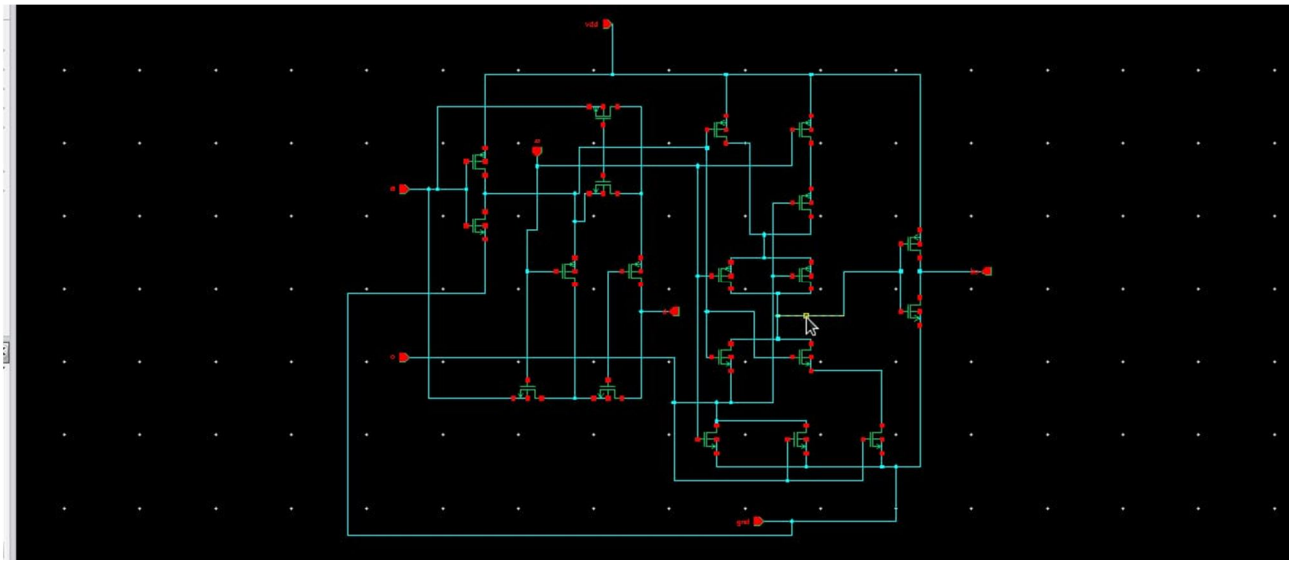

Fig.7 Schematic of 20T Full subtractor

Fig.8 Output of 20T full subtrctor

VII. EXPERIMENTAL RESULTS

S.no	Full Subtractor with different technologies	POWER(W)	DELAY(S)
i.	20T CMOS	24.615u	681.11p
ii.	14T CMOS	799n	242.12E-15
iii.	10T COM	263.09p	78.11E-15
iv.	10T FinFET	9.418p	38.6E-15

VIII. CONCLUSION

From the results it is clear that the 10T one-bit full subtractor (FinFET) consume less power and less delay compared to 20Transistor, 14Transistor, 10Transistors with CMOS technology, the proposed 10T, 14T, and 20T OBFS digital system have been used to implement a divider circuit. 10T full subtractor have low power consumption and low delay so it is used for low power applications.

IX. FUTURE SCOPE

The future scope of a 1-bit full subtractor using FinFET technology is promising due to the various advantages FinFETs offer over traditional MOSFETs. here are some key areas where this technology could have a significant impact :

1) Speed and Power efficiency
2) Leakage Reduction
3) High-Performance Computing
4) Quantum and Neuromorphic Computing
5) Miniaturization

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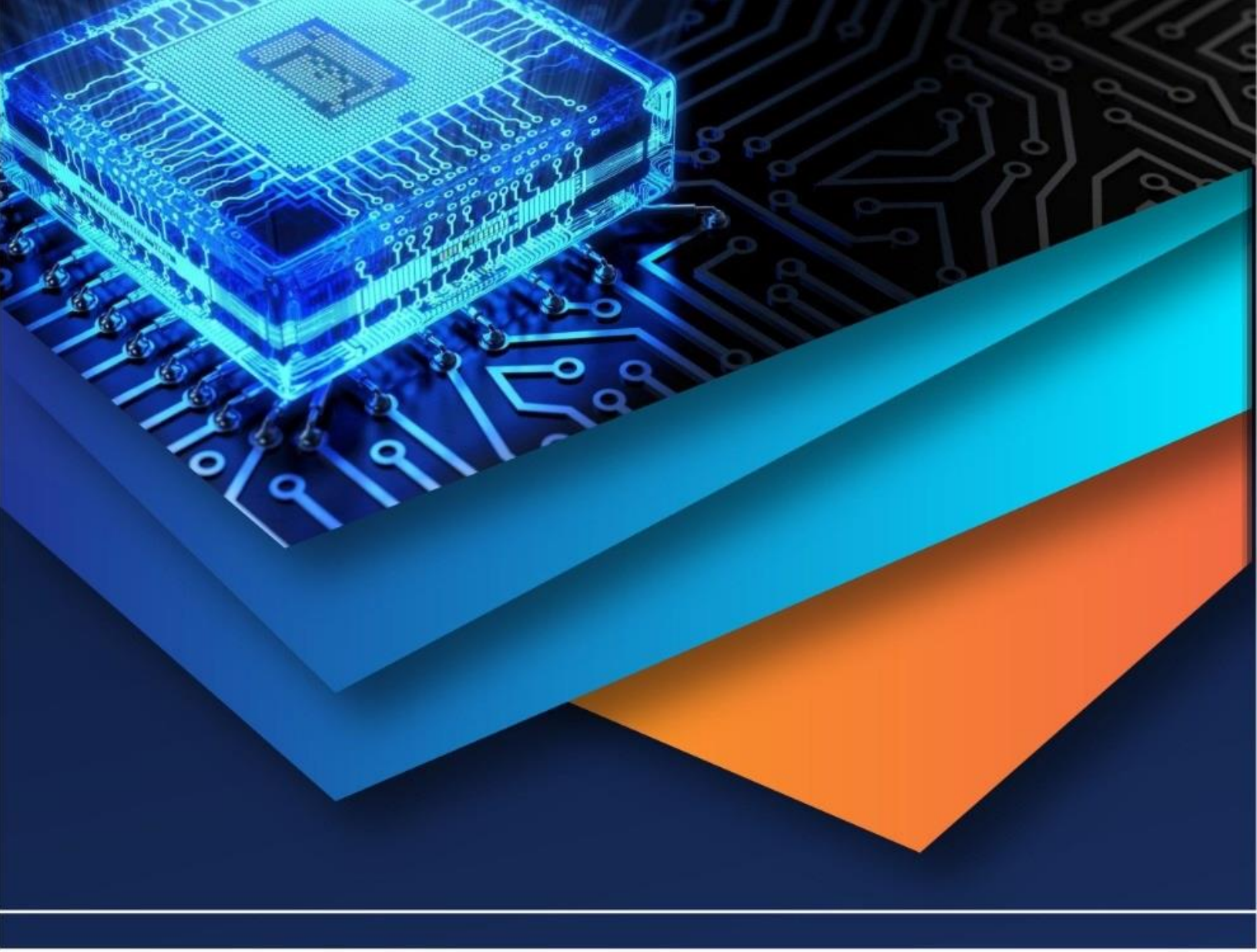

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