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Design and Implementation of 6-Tap FIR Filter Using MAC for Low Power Applications

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Abstract: ***A Significant number of mathematical operations, such as multiplication and accumulation, are often required by a digital signal processing (DSP) algorithm. Many DSP applications have latency limitations, which mean that the DSP operation must be performed within a certain amount of time for the system to function, and because DSP gives high accuracy, filters constructed in DSP have tighter control over the output accuracy. As a result, DSP applications must be fast, have a high throughput, and use little power. Filters with a finite impulse response (FIR) are commonly employed in digital signal processing (DSP) applications. A FIR filter that is efficient in terms of electricity is being built. The multiplier and accumulator (MAC) unit used a new implementation approach to develop this system. FIR filter is a type of filter. Multipliers, adders, and a variety of other components are commonly used in FIR filters. Multipliers, adders, and a series of delays are used to form the filter's output in FIR filters. The goal of this project is to design and implement a 6-tap finite impulse response (FIR) filter by replacing multipliers with an 8-bit Multiplier and Accumulator (MAC) unit within the FIR filter, where a low-power MAC unit is always a key to achieving high performance in a DSP system, and D flip-flops are used in place of delays and constructed using a latch-based design. The Wallace tree Multiplier was utilised in the construction of the MAC unit because it reduces the amount of partial products, and the adders used for accumulation are half adders and full adders. In the FIR filter, for the purpose of summing This work evaluates performance of FIR filter in terms of speed and power and synthesis are executed in Xilinx Vivado 2018.1 software environment and the implementation is done using VHDL codes. The result analysis shows that the proposed FIR filter consumes low power than conventional (standard) FIR filter. As the dynamic power results up to 11.932W and after implementation it results up to 12.029W.***
Keywords: ***MAC, Low power, latch-based design.***

I. INTRODUCTION

In today's society, power is seen as the most significant restraint. Excessive power dissipation affects dependability and raises the cost imposed by cooling systems and packaging in high-performance systems, and battery technology cannot keep up with rising demands for devices with light batteries and long time between recharges in portable systems. The expanding market for portable devices like as cell phones, gaming consoles, and battery-powered electronic systems necessitates the development of microelectronic circuits with extremely low power dissipation. As chip integration, size, and complexity grow, the difficulties of providing proper cooling may increase the cost of computing systems that utilise such integrated circuits or limit the operation of those systems.

As a result, power dissipation reduction approaches are not restricted to dynamic power. Power dissipation has become an important characteristic in low power VLSI circuit designs as a result of the increased use of portable electronic devices and the evaluation of microelectronic technology. The circuit complexity and fast speed of evolving VLSI technology imply a large increase in power consumption. To maintain a continuous flow of data, the time taken for input/output and processing must both be less than the sampling period. Because high sampling frequencies are required for accurately converting an analogue signal to digital, DSPs must be fast and power efficient.

II. LITERATURE SURVEY

In this paper, [1]"Design of area and power efficient digital FIR filter using modified MAC unit" they, propose an area and power efficient FIR filter implementation using modified Multiply and (MAC) unit. In general, the key blocks of the filter are multipliers and adders, in which multiplier is the one which occupies the major silicon area and consumes more power. The performance analysis of the proposed FIR filter is estimated with the MAC unit realized by the conventional adder and the modified carry select adder as well. The proposed FIR filter architecture with length of 5-tap and 9-tap are developed using Verilog HDL and implemented using SAED 90nm CMOS technology. The ASIC synthesis results show that the Area Delay Product (ADP) of the proposed 5-tap and 9-tap filter gains an improvement of 18.26% and 13.94%, respectively over the conventional method. Similarly, the Power Delay Product (PDP) is improved by 16.80% and 12.54%, respectively. This paper,[2] "Computationally Efficient Multiplier-Free Fir Filter Design" presents a very simple multiplier-free finite impulse response (FIR) low pass filter design procedure. It involves

Approximation of an equiripple FIR by rounding operation and application of the sharpening technique. It proposed simple efficient method for the design of multiplier-free. FIR filters without optimization. The method uses the rounding to the nearest integer of the coefficients of the equiripple. In that way the overall filter is based on combining one simple filter with integer coefficients. The parameters of the design are the rounding constant and the parameters of the sharpening polynomials such as the order of tangencies m and l. Our analysis indicates that utilizing this approach the required number of total nonzero bits becomes quite low and less than in the minimum number of signed powers-of-two (MNSPT) design. The cost is the increase of the total numbers of sums and the delays. This paper, [3] "FPGA implementation of efficient FIR Filter with quantized fixed-point coefficients" gives brief overview of the basic structure and hardware characteristics of the Finite Impulse Response (FIR) digital filter. FIR filter has been designed efficiently using mat lab and implemented on Field Programmable Gate Array (FPGA) platform. They have implemented a design of digital FIR filter
using Finite State Machine (FSM). In this approach it is possible to reuse the hardware implemented so that the area will be reduced significantly, and also the delay and power will be reduces as compared to the MATLAB – Simulink based FIR Filters. In this design the filter coefficients used are fixed-point coefficients, which will reduce the truncation and computation complexity. The work reported in this paper, [4] This paper, "A High-Performance 8-Tap FIR Filter Using Logarithmic Number System" presents an approach to implement a high-performance 8-tap digital FIR (Finite Impulse Response) filter using the Logarithmic Number System. In the past, FIR filters were implemented by a conventional number system. their speed was limited because of the multiply-accumulate operations. Her, they realize a fast FIR filter by utilizing the Logarithmic Number System, which allows a simple implementation of multiplication using a fixed-point adder. And the serious demerit of Logarithmic
Number System's algorithm, conversions to and from the conventional number representations, is effectively overcome by pipelining to reduce the delay and complexity of the filter. The critical path was reduced from a multiply-accumulate operation to an add operation. Our FIR filter can operate at 1.3 GHz under the condition of 1.2 V power supply using the SMIC 0.13micro m CMOS technology, and requires 27% less area than the original FIR filter [5] "FIR digital filter design by using windows method with MATLAB" deal with of Finite Impulse Response FIR digital filter design by using window method. The window method is easiest to design FIR, but lacks flexibility especially when the pass band and stop band ripples are different. The digital filter is used to filter discrete time signals with the ability to modify the frequency response of the filter at any time and it used in many applications such as data compression, biomedical signal processing, communication receivers, etc. Using MATLAB package software programs are developed for designing FIR digital filter and good results are obtained.

III. METHODOLOGY

A. *Basic Block Diagram of FIR Filter*

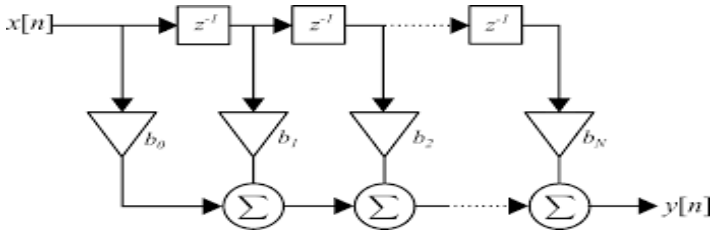

Fig: Basic block diagram of FIR filter

The use of FIR in a digital signal processing system is one sort of filter whose impulse response is of finite duration and settles to zero in finite time. This is in contrast to the IIR filter, which has internal feedback and can respond forever.
The top section of the above graphic is a N stage delay line with total N+1 taps, while the bottom part is a discrete time FIR filter of N number of orders. In the Z transform notation, each unit delay is a z-1 kind of operator.
The operation is described by the following equation, which defines the output sequence of y[n] in terms of its input sequence of x [n] given below.

$$y[n] = \sum_{i=0} b_i x\,[n-i]$$

Where, x[n] = input signal and y[n] = output signal

B. 6- Tap (Fifth-Order) FIR Filter

In this paper, we suggest a design for a six-tap FIR filter, as illustrated in the image above. The input is delayed and supplied to each multiplier, which produces products corresponding to different filter coefficients, which are then collected to produce the FIR filter output. We used several coefficients from Matlab and converted them to binary for input to the design filter; otherwise, we could use any coefficient. N=6 since it's a 6-tap FIR filter.

$$y[n] = b_0x[n] + b_1x[n-1] + b_2x[n-2] + b_3x[n-3] + b_4x[n-4] + b_5x[n-5]$$

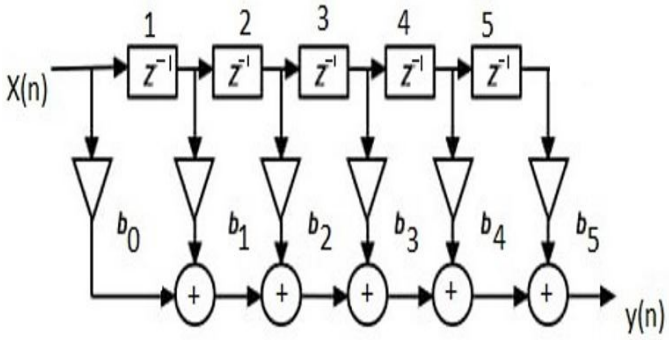

Figure 2: 6 tap FIR filter

C. Block Diagram of 6-Tap FIR Filter Using MAC Unit

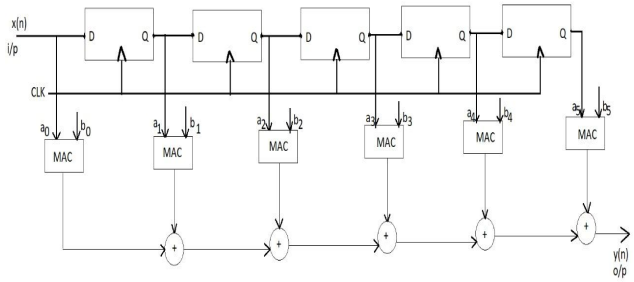

Figure 3: Block diagram of 6-tap FIR filter using MAC unit

This paper presents a design for a low-power 6 tap FIR filter. The power reduction is accomplished by using a MAC unit inside the filters rather than multipliers, which lower total activity and thus dynamic power. The essential building blocks of the MAC unit are identified, and each block's performance is evaluated. The total dynamic power of the FIR filter is determined. The 6 tap digital FIR filter was created with the goal of lowering total power usage.

D. MAC UNIT

A multiplier and an accumulator make up a traditional MAC unit. Which multiplies two values and then adds the result to the previously accumulated value, which must then be Restored in the registers to allow for future accumulations. A low-power MAC unit is always a cornerstone to achieving a high-performance digital signal processing system. Wallace tree multiplier and binary adders are the multiplier and adders used to construct the MAC unit.

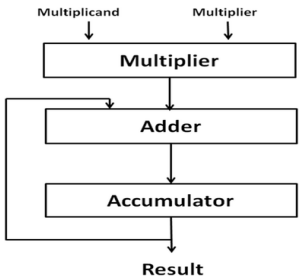

Figure 4: Block diagram of MAC unit

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IV. RESULTS

Actually, the coefficients used for the purpose of designing the FIR filter were "6" taken from the MAT Lab, they are;

Hexadecimal	Decimal
F1	241
F3	243
07	07
26	38
42	66
4e	78

Table 1: hexadecimal and decimal values of taken MAT lab coefficients

From the FIR filter equation

$$y[n] = a_0x[n] + a_1x[n-1] + a_2x[n-2] \ldots\ldots\ldots\ldots + a_{N-1}x[n-N]$$

$$y[n] = \sum_{i-0}^{`} a_i x\,[n-i]$$

As it is a 6-tap FIR filter, N= 6

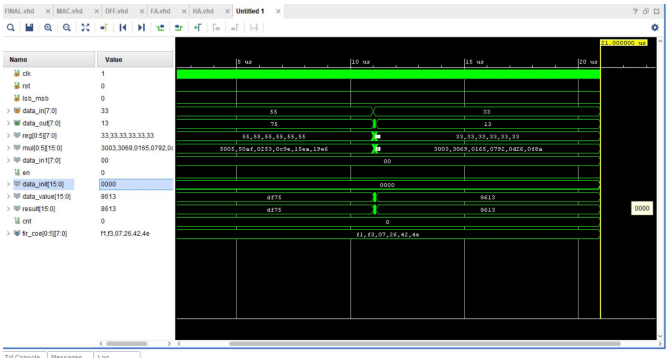

Figure 5: Observed graph by taking two different inputs

for example, **55**. From the output shown above for input given 55, the resulted output is **df75.**

Hexadecimal	Decimal
55	85
df75	57205

Table 2: hexadecimal and decimal values of taken input and observed output

From equation (1);

y[n] = 241[85] + 243[85] + 7[85] + 38[85] + 66[85] + 78[85]

y[n]= 20485 + 20655 + 595 + 3230 + 5610 + 6630

where, y[n] = **57,205……(1)**

Therefore, hence it is proved that the result from the filter is df75 when input is 55 which is equal to the theoretical calculation resulted from FIR filter equation as shown in equation (1)

for example 2, **33**. From the output shown above for input given 33, the resulted output is **8613.**

Hexadecimal	Decimal
33	51
8613	34323

Table 3: hexadecimal and decimal values of taken input and observed output

Conversion 55 hexadecimal to decimal Conversion df75 hexadecimal to decimal

From equation (1);

y[n] = 241[51] + 243[51] + 7[51] + 38[51] + 66[51] + 78[51]

y[n]= 12291+12393+ 357 + 1938 + 3366 + 3978

where, y[n] = **34,323**…….……. (2)

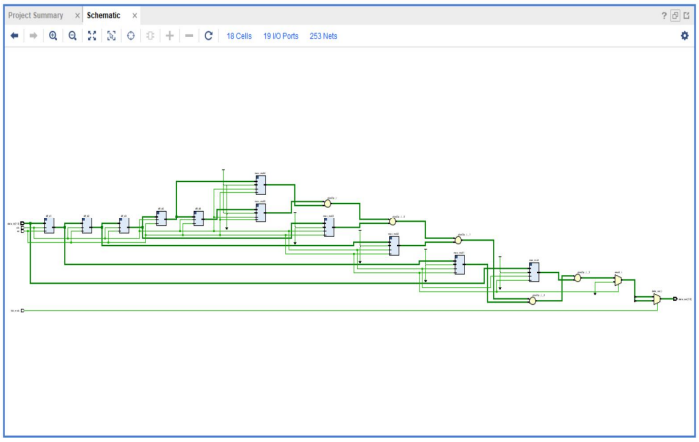

Figure 6: Schematic diagram of 6 tap FIR filter

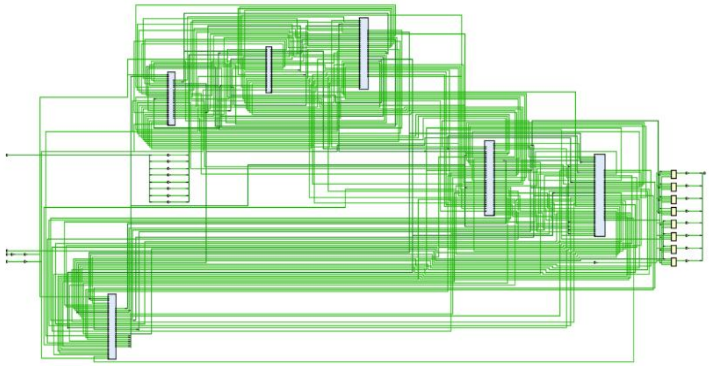

Figure 7: The entire schematic diagram after implementation with entire wiring

V. CONCLUSION

FIR filters are common in signal processing and can be implemented in a variety of ways. However, due to extensive computations, the speed, cost, and flexibility of big order filters are hampered. The design and simulation of a 6-tap digital FIR filter utilising an 8-bit Mac unit are the major topics of this paper. The design of FIR filter coefficients was done in MATLAB. The hardware description was entered using VHDL. VHDL codes have been developed, synthesised, mapped, and configured successfully. The FIR filter is designed to meet all design requirements. The power reduction is accomplished by utilising a MAC unit within the filters, which reduces total activity and thus dynamic power. The Xilinx Vivado 2018.1 software is used to model dynamic transients effectively.

VI. ACKNOWLEDGEMENT

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BIOGRAPHIES

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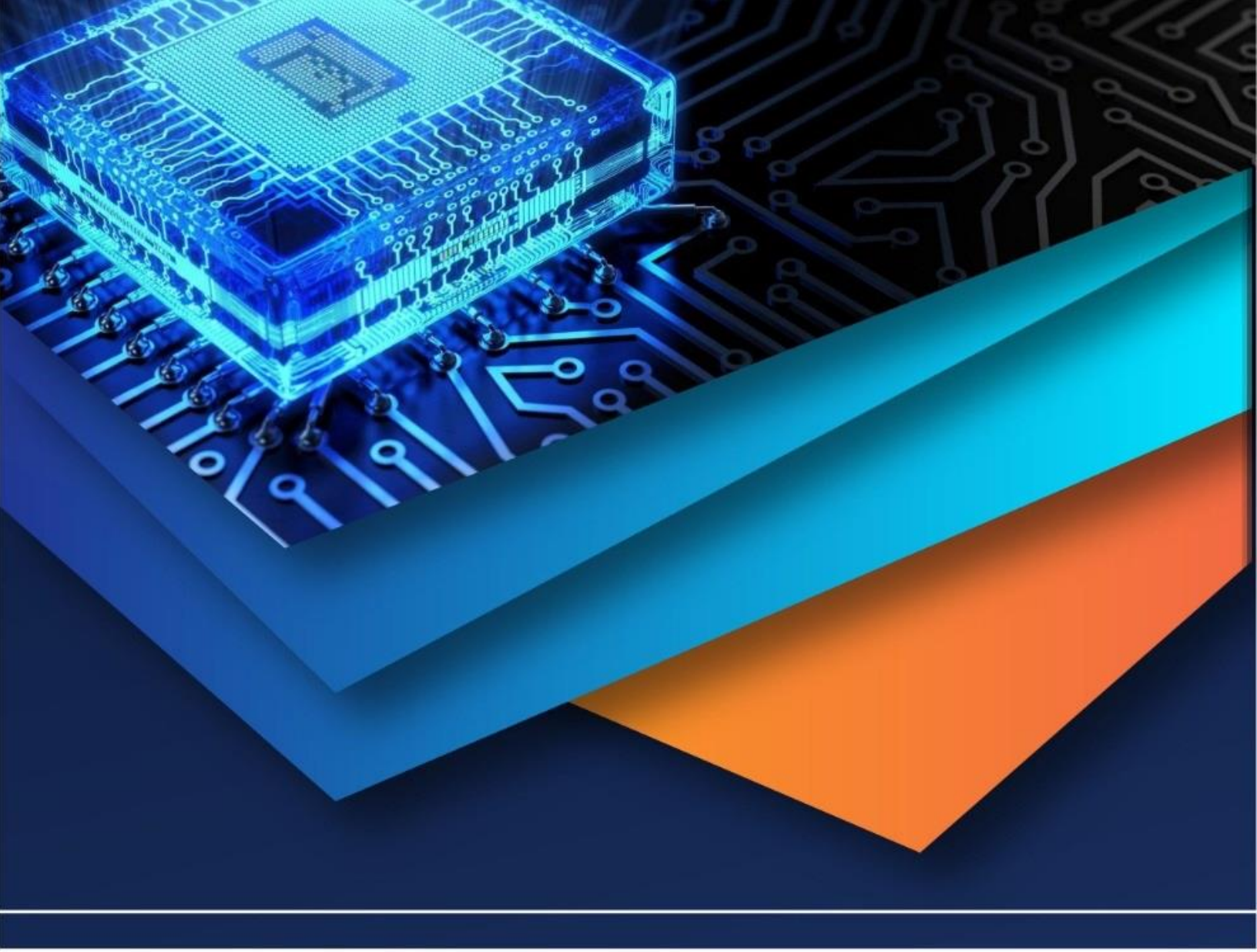

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