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Design and Implementation of an Analog PWM DC Motor Controller using 555 Timer and MOSFET

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Abstrac: ***DC motor speed control is a crucial part in industrial automation as well as consumer appliances. Use of microcontrollers is very common for these applications, but often face difficulties facing external high frequency noises. These circuits are often complex and need a simpler cost effective solution. This paper presents the design methodology, simulation & hardware results on implementing DC motor control using NE555 timer IC, which is configured in astable multivibrator mode. It generates a varying PWM signal assisted by a 50kΩ potentiometer and two 1N4007 diodes to steer the path for charging and discharging of the timing capacitor. This method enables approximately 0% to 100% duty cycle variation with maintaining a near constant operating frequency of 283Hz. This PWM signal drives the IRFZ44N MOSFET which would be used to provide power to the motor enabling high frequency switching. This method shows linear relationship between potentiometer and PWM generation, and the hardware results demonstrates software-free motor speed regulation. This purely analog approach retains substantial relevance***

Keywords: PWM; Astable Multivibrator; MOSFET; DC Motor control; Analog Electronics

I. INTRODUCTION

Pulse Width Modulation (PWM) is an essential method for regulating power supplied to electrical loads through rapid switching of signals in high or low states. For DC motors control, PWM ensures high efficiency speed control with no heat dissipation issues associated with resistive voltage dividing, making it invaluable for various applications starting from conveyor belts to household power tools [1].

Modern motor drives rely heavily on the use of microcontrollers and DSPs to create PWM signals. However, in the electromagnetic interference-prone environment of an industrial facility, fully analog designs provide distinct benefits, including freedom from software errors, instantaneous startup, and lower hardware costs. Having a grasp of analog PWM design basics is therefore crucial for students of power electronics [2].

The paper describes the development of an analog PWM DC motor control based on NE555 Timer IC, the ubiquitous versatile building block that found a wide range of uses in electronics. A potentiometer and steering diodes are used to separate charging and discharging circuits of a timing capacitor, thus allowing individual variation of the pulse ON time (Ton) and OFF time (Toff) while maintaining a constant frequency. The generated PWM signal drives an IRFZ44N MOSFET, effectively separating the fragile 5V control circuit from the motor with heavy current draw. The remainder of this paper is organized as follows: Section II reviews relevant prior work; Section III details the circuit design methodology; Section IV presents and discusses experimental results; Sections V and VI address applications and limitations respectively; Section VII concludes the paper.

II. LITERATURE REVIEW

Gayakwad [1] established a basic supporting structure for operational amplifiers and linear integrated circuits, providing the foundational understanding of timing, comparator working and voltage level trigger to use NE555 as a timer.

Salivahanan and Bhaskaran [2] extend this grounding to practical linear IC applications in closed-loop control and waveform generation.

Reddy et al. [3] demonstrated DC motor speed control using a 555 timer combined with a 7805 voltage regulator, confirming the feasibiliity of purely discrete analog architectures for variable-speed drive systems. Their work validated that the 555 IC in astable configurations can produce stable PWM outputs which is sufficient for motor actuation without digital intervention.

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Kedir [4] explored simultaneous speed and direction control of DC motors without the use of a microcontroller which highlights the engineering challenges of bidirectional analog drive. While that work included an H-bridge topology, it supported that analog PWM generation is a robust and scalable technique applicable across a spectrum of motor control scenarios.

The Texas Instruments NE555 datasheet [5] and Infineon IRFZ44N datasheet [6] provide the parameters as well as boundaries within which this design operates. Particularly the timer's output source/sink current limits and the rating of MOSFET's gate threshold voltage and drain current.

III. CIRCUIT DESIGN METHODOLOGY

A. PWM Generation Using the 555 Timer

NE555 Timer IC is set in astable mode, where it generates a self-sustained square wave at its output terminal (Pin 3). In the normal astable circuit design, the resistor path for both charge and discharge time periods is the same, limiting the possible duty cycle variation range. To bypass this constraint, two 1N4007 silicon switching diodes (D_1 and D_2) have been added to direct the capacitor's charging and discharging currents via different resistor paths.

A 50 kΩ potentiometer (R_1) is connected such that its wiper separates the total resistance into two complementary portions:

$$\mathbf{R_{1A} + R_{1B} = 50\ k\Omega}$$

A fixed resistor R_2 = 1 kΩ is placed in series with the supply rail to prevent a dead short during extreme wiper positions. A timing capacitor C_1 = 0.1 µF completes the RC network, while a 0.01 µF bypass capacitor C_2 is placed at the control voltage pin (Pin 5) to suppress high-frequency noise.

B. Charge and Discharge Path Analysis

Charging interval (T_{on}): The capacitor C_1 charges from V_{CC} through R_2 and R_{1A} via forward-biased diode D_1. Diode D_2 is reverse-biased during this phase, preventing current from flowing through R_{1B}. The ON-time is therefore:

$$T_{on} = 0.693 \times (R_2 + R_{1A}) \times C_1 \quad \textit{-(1)}$$

Discharging interval (T_{off}): The capacitor discharges through D_2, R_1B, and Pin 7 (Discharge) to ground. D_1 is reverse-biased, blocking the charge path. The OFF-time is:

$$T_{off} = 0.693 \times R_{1B} \times C_1 \quad \textit{-(2)}$$

The total period and frequency of oscillation are:

$$T = 0.693 \times (R_2 + R_1) \times C_1 \quad \textit{-(3)}$$

$$f = 1 / T \approx 283\ Hz \quad \textit{-(4)}$$

Since $R_2 + R_1$ remains constant regardless of wiper position, the frequency is effectively invariant. Duty cycle D is defined as:

$$D\ (\%) = (T_{on} / T) \times 100 \quad \textit{-(5)}$$

C. MOSFET Power Stage

The PWM signal from Pin 3 of the 555 timer is applied to the gate of an IRFZ44N N-Channel Power MOSFET via a 100 Ω gate resistor (R_3). This resistor prevents the inrush current that might occur during the switching transitions of the gate, thus preventing oscillations and electromagnetic interference.

MOSFET acts as a low-side switch: When the voltage on the gate is greater than the threshold voltage, VGS(th) (around 1.0 V minimum, around 2 V typical), the device enters the saturation region, connecting the negative terminal of the motor to the ground; therefore, current can be delivered.

When the PWM signal is LOW, the MOSFET will be turned off, interrupting the current delivery process. Fast cycling between these two conditions modifies the average voltage applied to the motor to control its speed.

The IRFZ44N features an on resistance, RDS(on) of around 17 mΩ at VGS = 10 V with the capability to conduct a drain current continuously up to 49 A.

A freewheeling diode across the terminals of the motor prevents an induced voltage rise when switching off the MOSFET, protecting the device from exceeding its drain-source voltage rating.

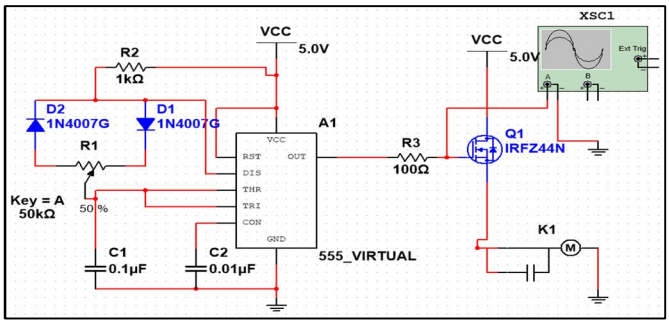


Fig. 1: Circuit Schematic of the Analog PWM Motor Controller

IV. RESULTS AND DISCUSSION

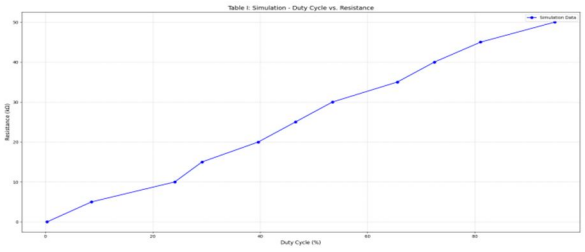
A. Simulation Results

The circuit was simulated using a virtual 555 timer model in a SPICE-based environment. The potentiometer wiper was swept from 0 kΩ to 50 kΩ with increment of 5 steps which provided 11 readings, and the resulting duty cycle of the output waveform was recorded in TABLE I, which summarizes the simulation data.

Table I
Simulation: Duty Cycle vs. Potentiometer Resistance

Duty Cycle (%)	Resistance (kΩ)
0.34	0
8.60	5
24.11	10
29.18	15
39.66	20
46.56	25
53.45	30
65.53	35
72.43	40
81.04	45
94.83	50

The data exhibits a clearly linear trend ($R^2 \approx 0.998$). This confirms that by incrementing R_{1A} in equal steps produces increase in duty cycle proportionally as predicted by equations (1) and (5).



Graph -1: Simulation Resistance vs Duty Cycle

The frequency of the output of the simulated PWM generator circuit remained stable at approximately 225 Hz, which has a slight deviation from the theoretical 283 Hz attributable to virtual component modeling approximations.

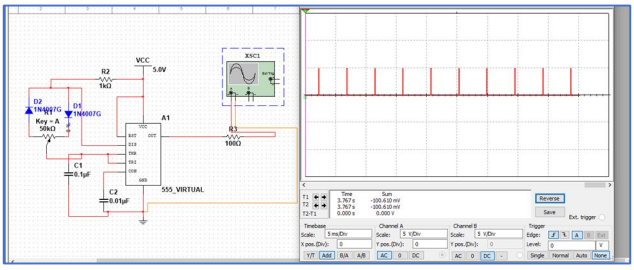


Fig-2: Output Waveform at 0% duty cycle

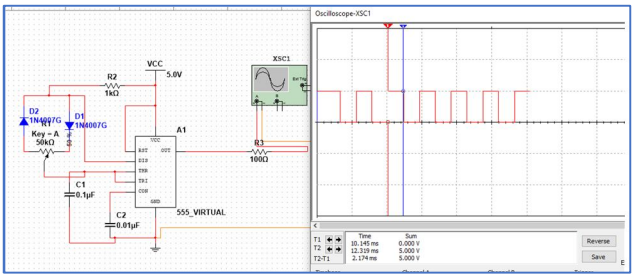


Fig-3: Output Waveform at 50% duty cycle

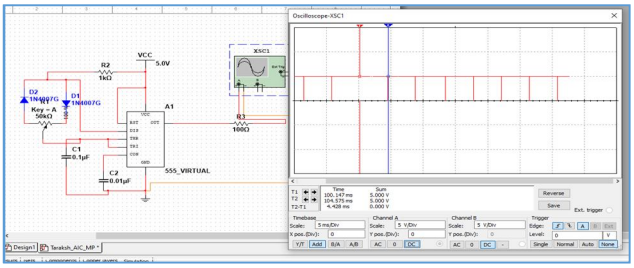


Fig-4: Output Waveform at 100% duty cycle

B. Hardware Measurement Results

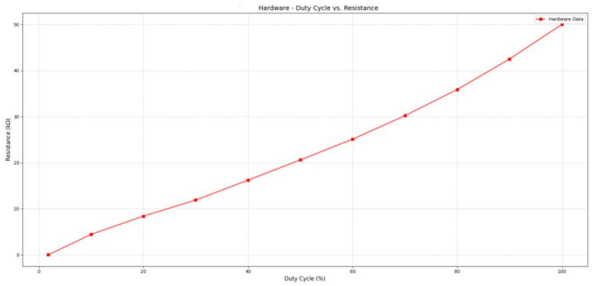
The circuit was first assembled on a solderless breadboard and subsequently transferred to a Zero PCB for improved mechanical stability and reduced parasitic resistance. TABLE II presents the measured duty cycle values across the range of potentiometer.

Table II
Hardware: Duty Cycle VS. Potentiometer Resistance

Duty Cycle (%)	Resistance (kΩ)
1.8	0.00
10	4.44
20	8.39
30	11.89
40	16.20
50	20.59
60	25.10

Duty Cycle (%)	Resistance (kΩ)
70	30.19
80	35.88
90	42.50
100	49.998

Hardware results verify the linear relationship between duty cycle and resistance with a minimum measured duty cycle of 1.8% (instead of ideal 0%), which is due to the finite forward voltage drop (~0.7 V) of the 1N4007 diodes introducing a small residual charge current even at lowest resistance.



Graph -2: Hardware Resistance Vs Duty Cycle

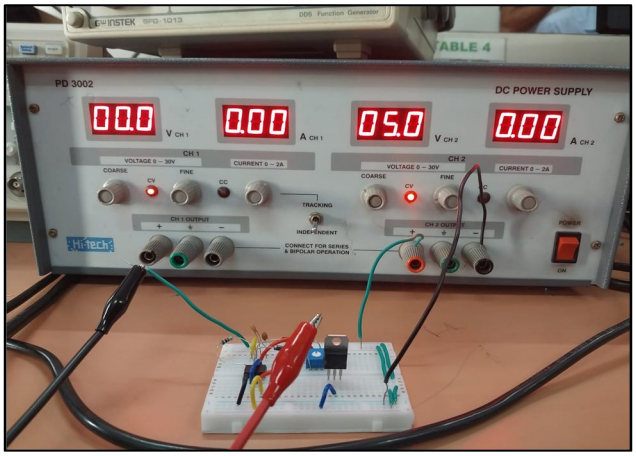


Fig-5: Circuit implementation on Breadboard

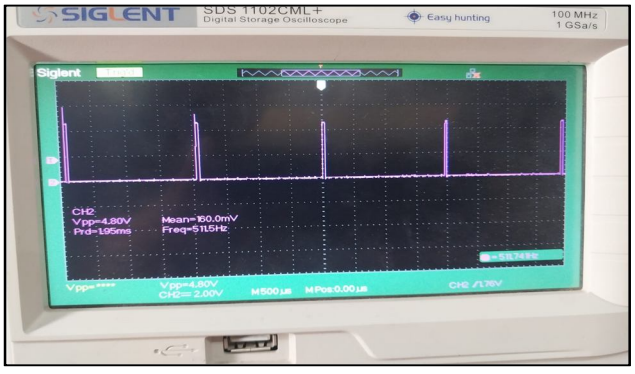


Fig-6: Observed waveform at 0% duty cycle

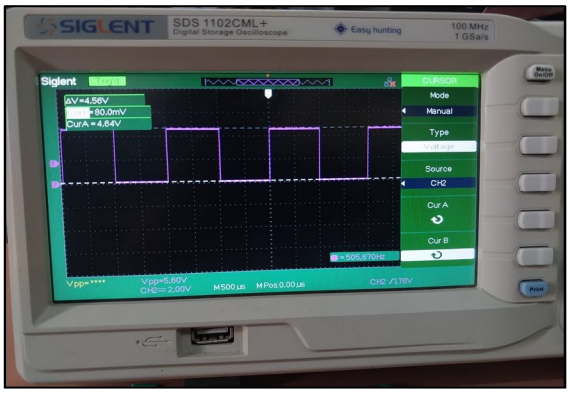


Fig-7:Observed waveform at 50% duty cycle

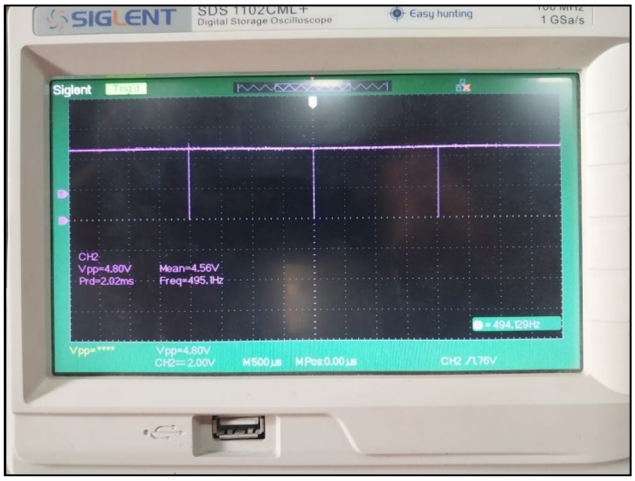


Fig-8:Observed waveform at 100% duty cycle

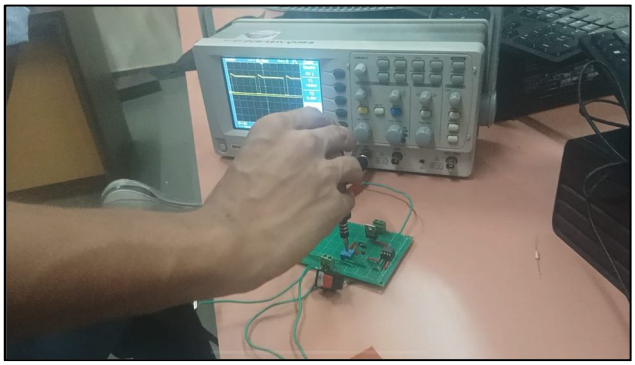
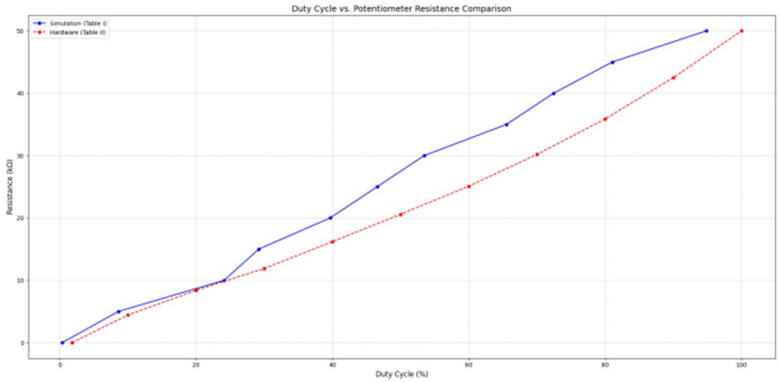


Fig-9: Circuit implementation on Zero PCB

C. Comparative Analysis

Comparing TABLE I and TABLE II, both datasets confirm a highly linear duty cycle-to-resistance mapping. The primary deviation is the non-zero minimum duty cycle in hardware (~1.8%) versus simulation (~0.34%), arising from the physical diode's forward voltage offset. Additionally, the hardware operating frequency range of 300-350 Hz (PCB implementation) deviates from both the theoretical 283 Hz and simulated 225 Hz, because of capacitor and resistor manufacturing tolerances (typically ±5%–±20%) and the stray capacitances on the PCB traces. Despite these minor deviations, the overall system behaviour aligns closely with theoretical predictions, thus validating the design methodology.



Graph -3: Hardware Vs Simulation

V. APPLICATIONS

This circuit architecture is suited for many areas like in industrial automation, these discrete analog PWM controllers offer high immunity against electromagnetic interference when compared to microcontrollers. These make it suitable for conveyor systems and pumps which are used in electrically noisy environments. In addition to it, in HVAC and cooling systems, this circuit enables the fan control which saves energy with the help of speed control over discrete binary switching.

Power tools like cordless drills and mixer grinders utilize a 555-based PWM speed controller stage after the user trigger. This circuit regulates the speed of these machines and the fundamental principle of driving the motor using a MOSFET can be used in light electric vehicles for throttle control.

VI. ADVANTAGES AND LIMITATIONS

A. Advantages

The primary advantage of this design is that it is completely independent from software, firmware bugs, latency while booting up and watchdog reset which affect the microcontroller-based implementations. The overall cost of the circuit is economical (total cost: ₹125 / ~USD 1.50) and is suitable for mass production. Low R_{DS}(on) of IRFZ44N MOSFET (17 mΩ) yields power loss below 1 W at moderate load currents. This offers superior thermal performance compared to equivalent BJT based controllers. Finally, the steering diode configuration enables a smooth duty cycle sweep between near 0% to 100% range without requiring additional control circuitry.

B. Limitations

The existing design uses the open loop approach, whereby the regulation of speed under varying loads is a passive process; as the load torque increases, the motor speed decreases without any corrective measure being employed. Bidirectional motor operation calls for the use of the H-bridge architecture, which makes the system much more complex. Analog component tolerances result in changes in frequency under changing temperatures and different specimens due to the lack of crystal-locking found in digital systems.

These constraints suggest the design is best suited for applications with relatively constant loads where approximate speed setting is sufficient.

VII. CONCLUSION

It can be confidently stated that PWM-based DC motor speed control with highly accurate duty cycle variation is fully viable using purely analog components independent of digital processing architectures.

Using an NE555 timer IC with diodes used for duty cycle control and timing done with a combination of a resistor and half-potentiometer, continuously variable duty cycles ranging from around 0% to 100% are maintained at a constant frequency of around 283 Hz.

This is proven using both simulations in SPICE as well as actual prototype implementation.

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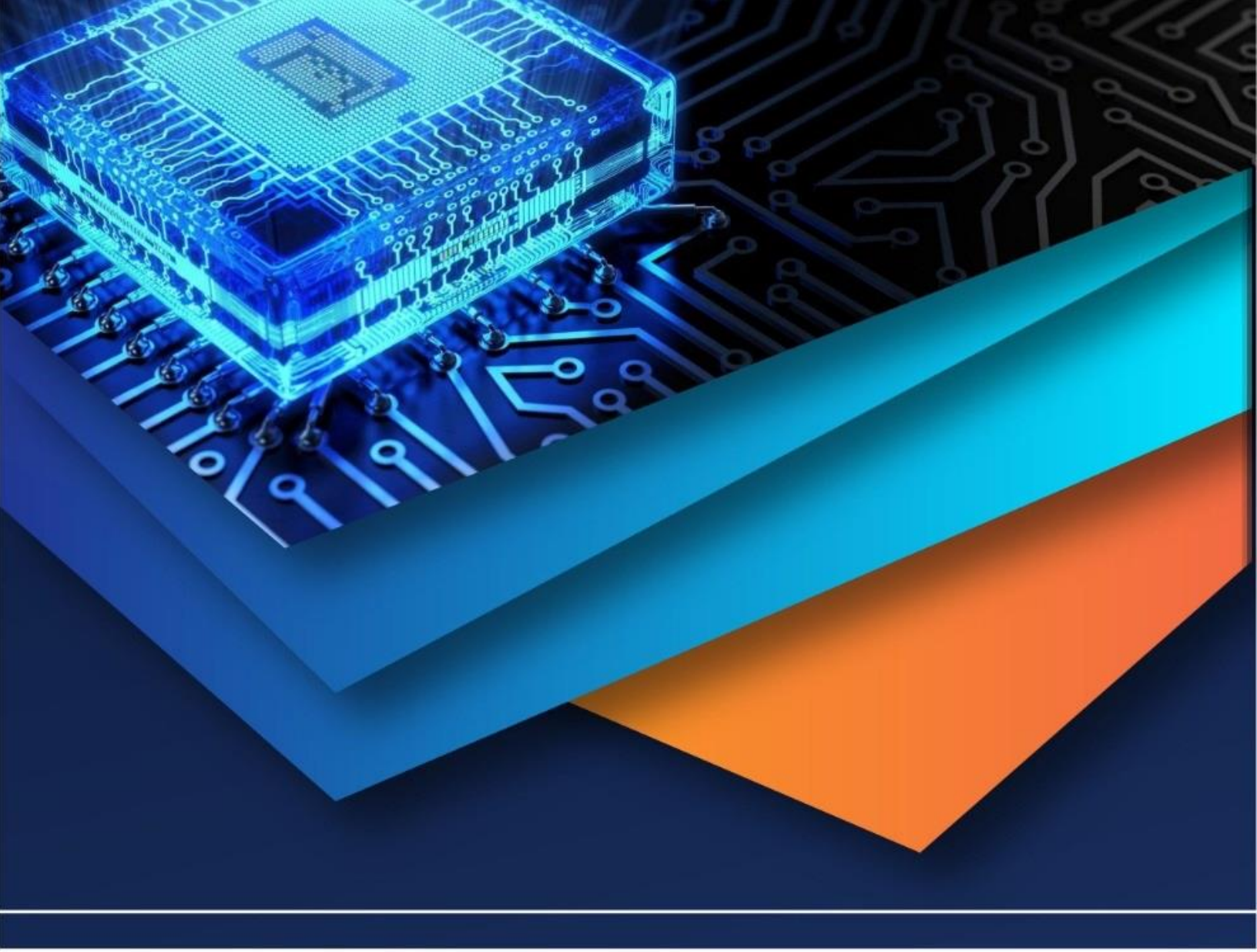
IRFZ44N power MOSFET acts as an effective power stage between the low power 5V control circuit and the motor with higher currents.

This project is expected to a foundational baseline for engineers and educators in understanding the fundamentals of power electronics and analog control systems and can also act as a baseline for more complex applications.

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