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Design and Implementation of an LMS-Based Speech Enhancement System on a Xilinx Zynq-7000 SoC

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Abstract: ***Speech enhancement is essential for improving speech quality in real-time communication and embedded audio systems. This paper presents the design and implementation of an LMS-based speech enhancement system on a Xilinx Zynq-7000 System-on-Chip (SoC) using a model-based design approach. The LMS adaptive filter was developed and validated in MATLAB/Simulink using floating-point arithmetic and subsequently optimized using fixed-point representation for efficient FPGA implementation. Verilog HDL was automatically generated using MATLAB HDL Coder and deployed on the Zynq-7000 SoC through the HDL Workflow Advisor. The implemented system was evaluated using Signal-to-Noise Ratio (SNR), Mean Square Error (MSE), Short-Time Objective Intelligibility (STOI), and FPGA implementation metrics including resource utilization, timing, and power consumption. Experimental results demonstrate successful hardware implementation while preserving speech quality. The proposed workflow provides an efficient transition from algorithm development to FPGA-based speech enhancement systems.***

Keywords: Speech Enhancement, Least Mean Square (LMS), Adaptive Filtering, Xilinx Zynq-7000 SoC, MATLAB/Simulink, FPGA, HDL Coder.

I. INTRODUCTION

Speech enhancement is widely used in mobile communications, hearing aids, teleconferencing, healthcare, and voice-controlled systems to improve speech quality in noisy environments. Background noise degrades speech intelligibility and reduces the performance of speech processing systems. Adaptive filtering, particularly the Least Mean Square (LMS) algorithm, is widely employed for speech enhancement because of its low computational complexity, modest memory requirements, and stable convergence characteristics. The Xilinx Zynq-7000 System-on-Chip (SoC), which combines an ARM-based Processing System (PS) with Programmable Logic (PL), provides an efficient platform for real-time adaptive signal processing. Although previous studies have implemented LMS algorithms on FPGA and SoC platforms, most focus on algorithm implementation or hardware realization, with limited attention to a complete model-based design workflow.

This paper presents a MATLAB/Simulink-based implementation of an LMS-based speech enhancement system on the Xilinx Zynq-7000 SoC. The proposed workflow integrates algorithm validation, fixed-point optimization, automatic HDL generation, hardware deployment, and implementation analysis. System performance is evaluated using SNR, MSE, STOI, and FPGA implementation metrics to demonstrate an efficient transition from simulation to hardware realization.

II. LITERATURE REVIEW

Adaptive filtering has been widely applied in speech enhancement, echo suppression, channel equalization, and system identification. Widrow and Stearns introduced the Least Mean Square (LMS) algorithm, while Haykin established its theoretical framework and convergence characteristics [1], [2].

Recent studies have implemented LMS-based adaptive filters on FPGA and SoC platforms using hardware–software co-design and MATLAB/Simulink-based workflows [3] – [5]. These works demonstrate the feasibility of FPGA implementation for real-time signal processing; however, most focus on either algorithm realization or hardware implementation.

In contrast, this work presents a unified model-based design methodology that integrates algorithm validation, fixed-point optimization, automatic HDL generation, hardware deployment, and implementation analysis within a single development workflow. The implemented system is further evaluated using speech enhancement metrics together with FPGA implementation results.

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III. PROPOSED METHODOLOGY

The proposed speech enhancement system adopts a model-based design approach to simplify the transition from algorithm development to FPGA implementation. The complete workflow, including algorithm modeling, functional verification, fixed-point optimization, automatic HDL generation, hardware deployment, and implementation analysis, is performed within MATLAB/Simulink. This unified approach reduces manual development effort and enables efficient implementation on the Xilinx Zynq-7000 SoC.

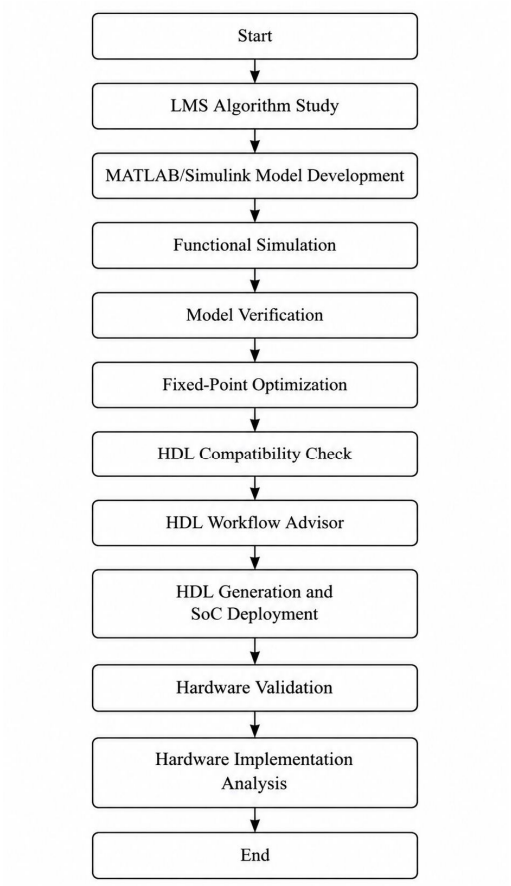

Figure 1. Proposed Design Methodology

Figure 1 illustrates the proposed implementation workflow. A clean speech signal is corrupted with additive white Gaussian noise (AWGN) to generate the primary input, while a correlated reference noise signal is supplied to the LMS adaptive filter. After floating-point verification, the model is converted to fixed-point representation and automatically translated into Verilog HDL using MATLAB HDL Coder for deployment on the Xilinx Zynq-7000 SoC.

A. LMS Adaptive Filtering Algorithm

The Least Mean Square (LMS) algorithm iteratively updates the filter coefficients to minimize the estimation error between the desired signal and the filter output. Owing to its low computational complexity and stable convergence, it is widely used in real-time speech enhancement applications.

The filter output is given by

$$y(n) = w(n)^T \cdot x(n)$$

where x(n) is the input vector and w(n), is the adaptive filter coefficient vector.

The estimation error is computed as

$$e(n) - d(n) - y(n)$$

where d(n) is the desired signal.

The filter coefficients are updated according to the LMS weight update equation

$$w(n+1) - w(n) + 2\mu e(n)x(n)$$

where μ is the step-size parameter that controls the convergence speed and stability of the adaptive filter.

B. Proposed System Architecture

Figure 2 shows the proposed speech enhancement system. The noisy speech signal and correlated reference noise are converted to fixed-point representation before entering the LMS adaptive filter. The filter estimates the correlated noise and subtracts it from the primary input to generate the enhanced speech signal, which is then used for waveform visualization and performance evaluation.

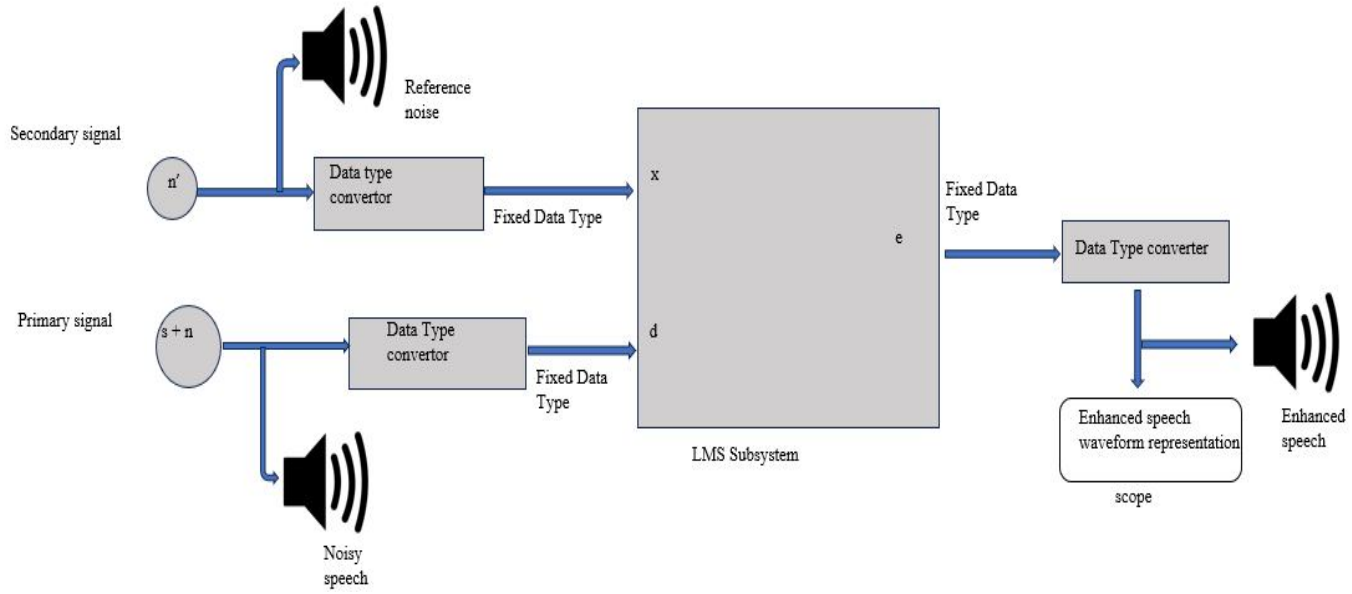

Figure 2. Proposed Design Implementation

C. Fixed-Point Optimization

The LMS algorithm was first verified using floating-point arithmetic and then converted to fixed-point representation for FPGA implementation. A signed (1,32,29) fixed-point format was selected because it preserved numerical accuracy while ensuring compatibility with automatic HDL generation and efficient hardware implementation.

D. HDL Generation and SoC Implementation

After functional verification, the fixed-point model was converted into synthesizable Verilog HDL using MATLAB HDL Coder and HDL Workflow Advisor. The generated HDL was synthesized and implemented in Xilinx Vivado, where the LMS adaptive filter IP was integrated with the Xilinx Zynq-7000 SoC through an AXI4-Lite interface. The Processing System (PS) handled control functions, while the Programmable Logic (PL) executed the adaptive filtering operations. The design was deployed on the ZedBoard for hardware validation.

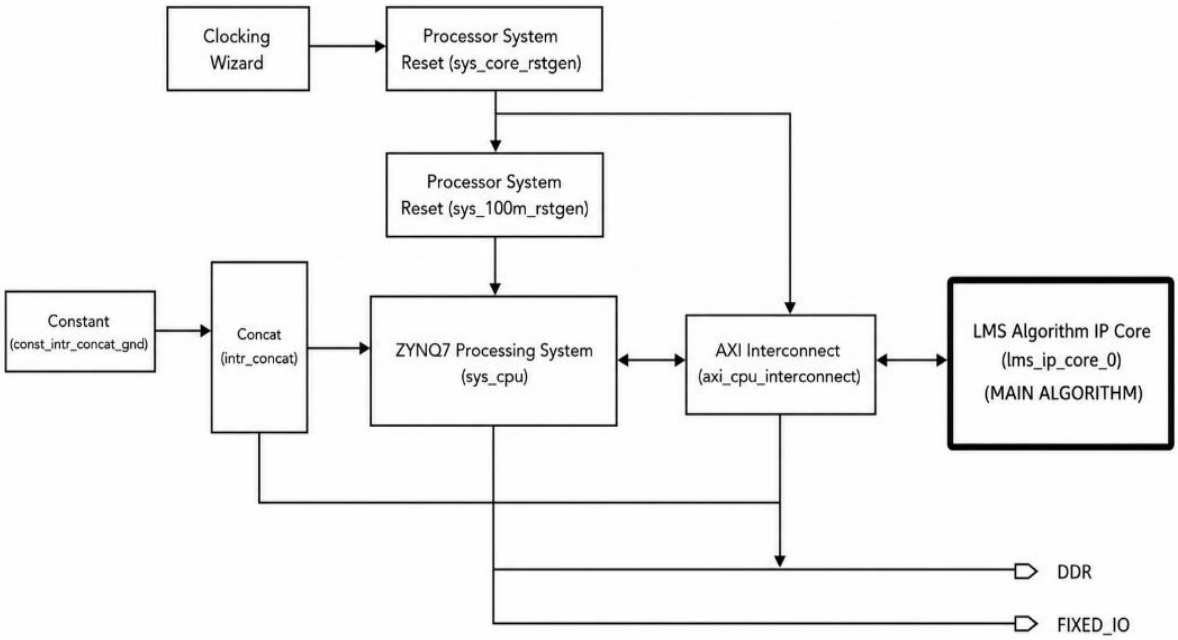

Figure 3. Zynq-7000 SoC Architecture Incorporating the Proposed LMS Adaptive Filter IP

Figure 3 illustrates the integration of the LMS adaptive filter IP into the Xilinx Zynq-7000 SoC architecture. The custom IP communicates with the ARM-based Processing System (PS) through an AXI4-Lite interface, while the adaptive filtering operations are executed in the Programmable Logic (PL). This architecture enables efficient hardware acceleration while maintaining seamless interaction between software and hardware components.

TABLE I
HARDWARE IMPLEMENTATION SUMMARY OF THE PROPOSED LMS ADAPTIVE FILTER

Parameter	Used	Available	Utilization (%)
Slice LUTs	2707	53200	5.09
Slice Registers (FFs)	2233	106400	2.10
DSP48 Slices	68	220	30.91
Slice Resources	1310	13300	9.85
Total On-Chip Power	1.773 W	-	-
Worst Negative Slack (WNS)	+19.770 ns	-	-
Total Negative Slack	0 ns	-	-

Table I summarizes the FPGA implementation results. The proposed design achieved low LUT and register utilization, successful timing closure with a positive WNS of 19.77 ns, and an estimated on-chip power consumption of 1.773 W, demonstrating efficient hardware implementation.

IV. EXPERIMENTAL SETUP AND PERFORMANCE EVALUATION

The proposed LMS-based speech enhancement system was evaluated through MATLAB/Simulink simulation and hardware implementation on a Xilinx Zynq-7000 SoC (ZedBoard). The workflow included floating-point verification, fixed-point optimization, automatic HDL generation, and hardware validation. Performance was assessed by comparing the enhanced speech obtained from simulation and hardware implementation with the original speech signal.

A. Experimental Setup

The LMS adaptive filter was developed in MATLAB/Simulink and converted into synthesizable Verilog HDL using MATLAB HDL Coder. The generated HDL was synthesized and implemented in Xilinx Vivado, and the resulting hardware design was deployed on the ZedBoard through HDL Workflow Advisor.

B. Input Test Signals

The system was evaluated using a primary input consisting of speech corrupted by additive white Gaussian noise (AWGN) and a correlated reference noise signal. The same input signals were used for floating-point simulation, fixed-point simulation, and hardware validation to ensure consistent performance evaluation.

C. Performance Evaluation Metrics

Performance was evaluated using Signal-to-Noise Ratio (SNR), Mean Square Error (MSE), and Short-Time Objective Intelligibility (STOI). Convergence behavior and FPGA implementation metrics, including resource utilization, timing performance, and power consumption, were also analyzed.

$$SNR = 10\log_{10}\left(\frac{P_{signal}}{P_{noise}}\right)$$

$$MSE = \frac{1}{N}\sum_{n=1}^{N} e^2(n)$$

D. Hardware Validation

The generated LMS adaptive filter IP was integrated with the Xilinx Zynq-7000 SoC through an AXI4-Lite interface and deployed on the ZedBoard. Hardware validation was performed using prerecorded speech and noise signals supplied from MATLAB/Simulink, and the hardware output was compared with the simulation results to verify correct operation.

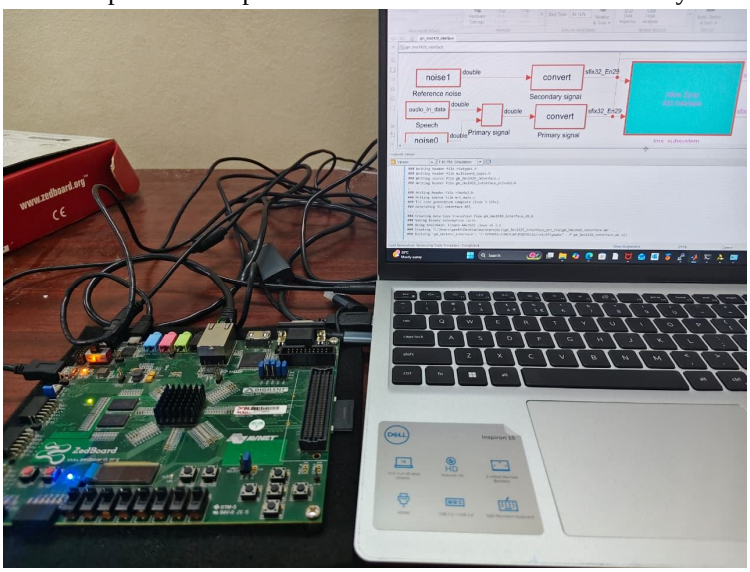

Figure 4. Hardware Validation Setup

V. RESULTS AND DISCUSSION

The performance of the proposed LMS-based speech enhancement system was evaluated through MATLAB/Simulink simulation and hardware implementation on the Xilinx Zynq-7000 SoC. The system was assessed using waveform analysis, SNR, MSE, STOI, convergence behavior, and FPGA implementation metrics.

A. Ground (Original) Speech Signal

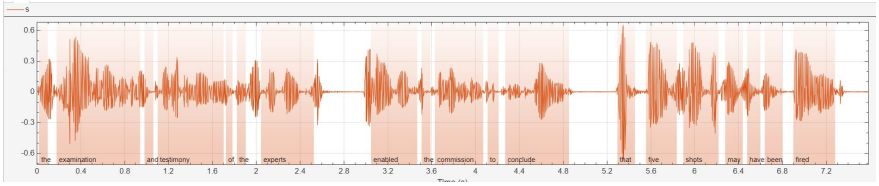

Figure 5. Ground (Original) Speech Signal

Figure 5 shows the original speech signal used as the reference for evaluating the proposed speech enhancement system.

B. Input Signals

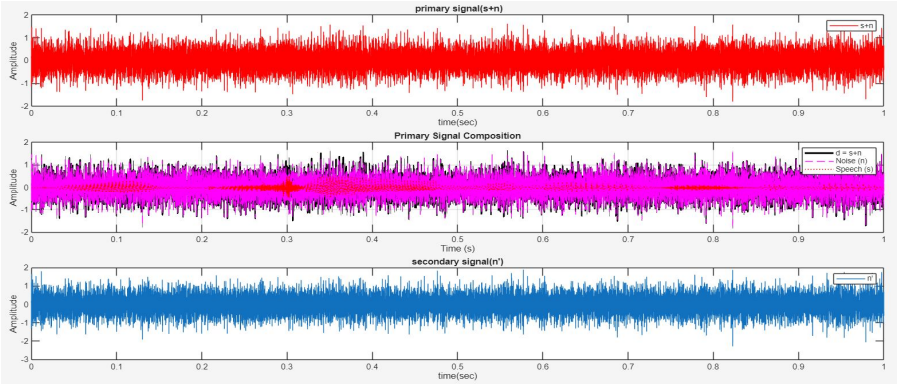

Figure 6. Primary Input and Reference Noise Signals Used for Adaptive Filtering

Figure 6 shows the noisy speech signal and the correlated reference noise supplied to the LMS adaptive filter for speech enhancement.

C. Floating-Point Enhanced Speech

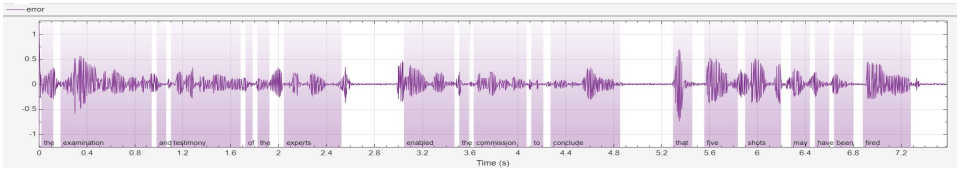

Figure 7. Floating-point Enhanced Speech

Figure 7 shows the enhanced speech obtained using the floating-point implementation. The proposed system achieved an SNR of 13.71 dB, an MSE of 1.84×10^{-4}, demonstrating effective speech enhancement.

D. Fixed-Point Enhanced Speech

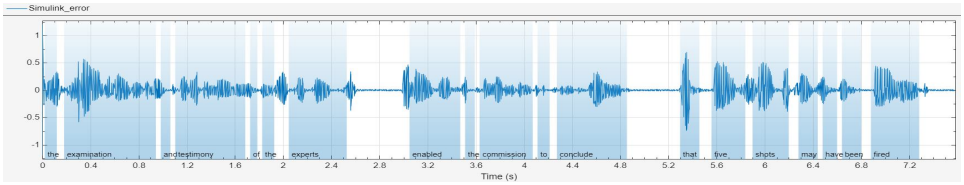

Figure 8. Fixed-point Enhanced Speech

Figure 8 presents the fixed-point implementation. The results closely match the floating-point model, indicating that the selected fixed-point representation preserves numerical accuracy with negligible performance degradation.

E. Convergence Analysis

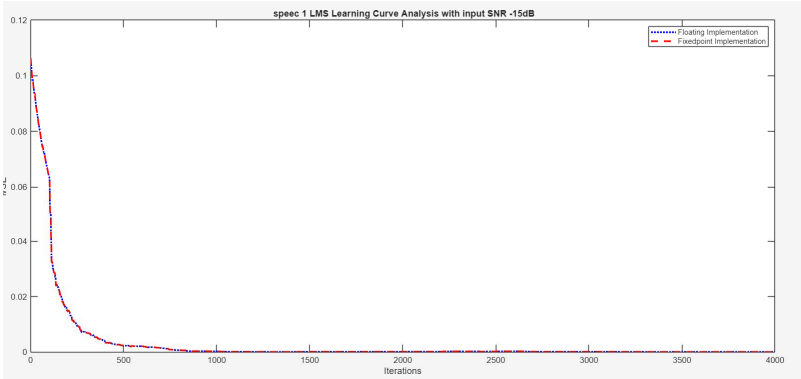

Figure 9. LMS Learning Curve

Figure 9 illustrates the convergence behavior of the LMS adaptive filter. The estimation error decreases rapidly during the initial iterations and gradually reaches a steady state, confirming stable convergence.

F. Hardware Enhanced Speech

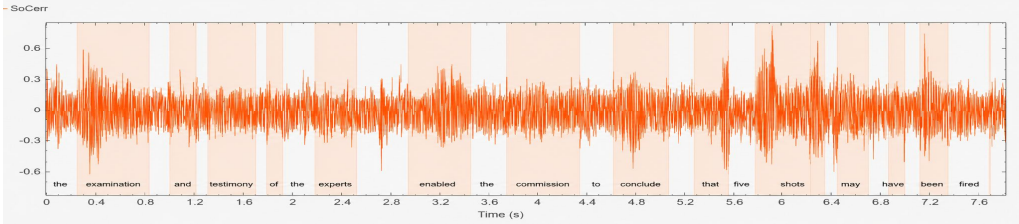

Figure 10. Hardware Enhanced Speech Output

Figure 10 presents the enhanced speech obtained from the ZedBoard implementation. The hardware implementation successfully executed the proposed LMS adaptive filter and produced speech enhancement with acceptable performance under FPGA implementation constraints.

G. Performance Comparison

Table II summarizes the quantitative performance of the floating-point simulation, fixed-point simulation, and hardware implementation. The comparison evaluates the impact of fixed-point optimization and hardware realization on speech enhancement performance using objective speech quality measures.

TABLE II
PERFORMANCE COMPARISON OF FLOATING-POINT, FIXED-POINT, AND SOC IMPLEMENTATIONS

Implementation	**SNR (dB)**	**MSE**	**STOI**
Floating Point (Double)	13.7136	0.000184103301704	0.9832
Fixed Point (1,32,29) (Simulink)	13.7108	0.000184220542948	0.9832
Fixed Point (1,32,29) (SoC)	-3.958325	0.010771035713966	0.6074

Table II compares the floating-point, fixed-point, and hardware implementations. The floating-point and fixed-point simulations achieved nearly identical performance, confirming the effectiveness of the selected fixed-point format. Although the hardware implementation exhibited lower SNR and STOI than the simulation results, this performance reduction is mainly attributed to fixed-point quantization and finite arithmetic precision during FPGA realization. Nevertheless, the proposed system successfully demonstrated real-time speech enhancement on the Xilinx Zynq-7000 SoC

VI. CONCLUSION

This paper presented the design and implementation of an LMS-based speech enhancement system on a Xilinx Zynq-7000 SoC using a model-based design approach. The proposed workflow integrated algorithm development, fixed-point optimization, automatic HDL generation, and FPGA deployment within the MATLAB/Simulink environment. Experimental results demonstrated effective speech enhancement, successful hardware implementation, and efficient FPGA resource utilization. The proposed methodology provides a practical framework for implementing adaptive signal processing algorithms on FPGA-based embedded systems. Future work will focus on real-time microphone input, advanced adaptive algorithms such as NLMS and RLS, and further optimization of hardware performance.

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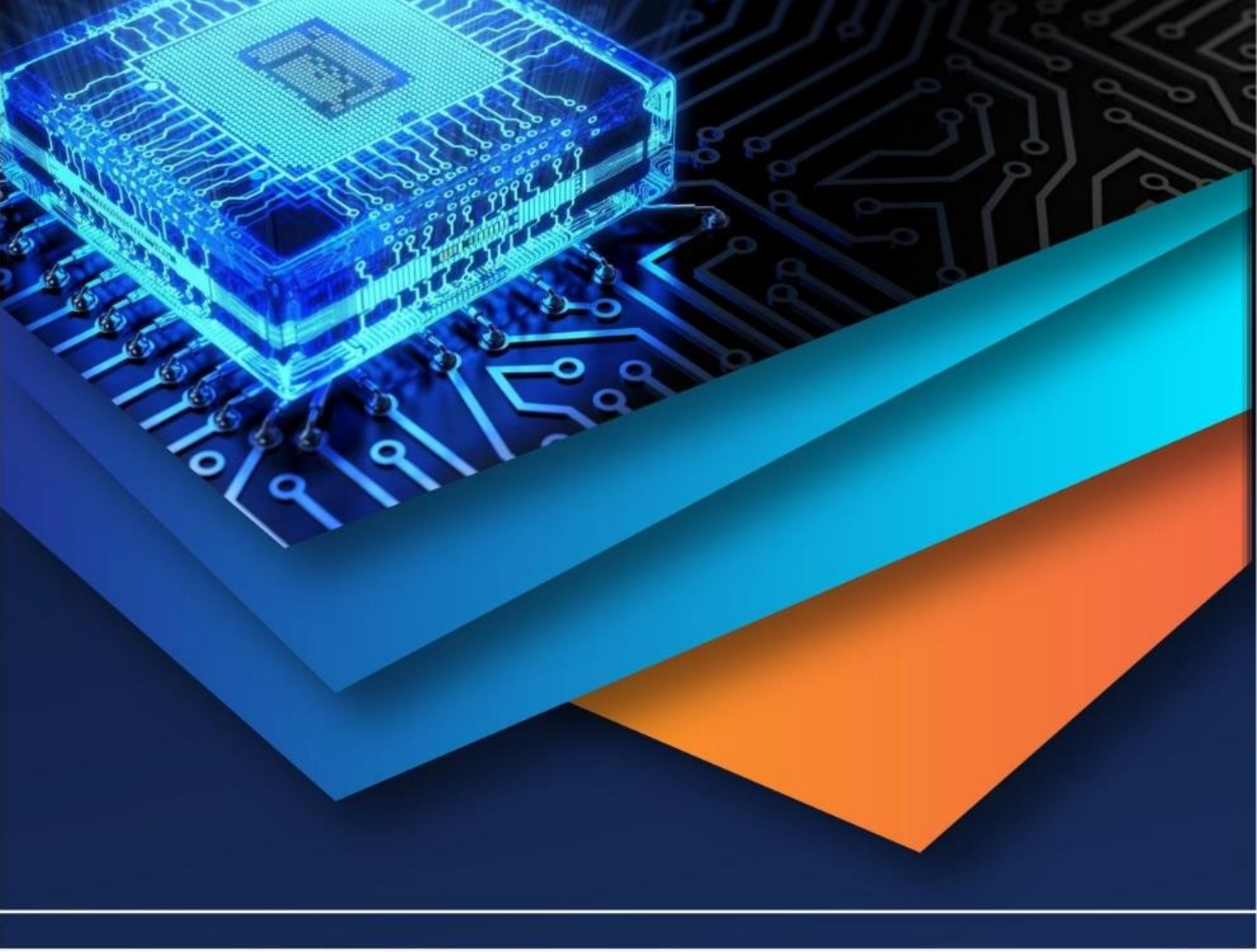

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