iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 12 **Issue:** V **Month of publication:** May 2024

DOI: https://doi.org/10.22214/ijraset.2024.62374

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 12 Issue V May 2024- Available at www.ijraset.com

Design and Implementation of Braun Multiplier using Verilog: Research

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Abstract: ***Multiplication is widely used in places like digital signal processing, image processing, instrumentation that require multilayer components. Carry Save Adder and ripple carry adder both are used in parallel processing architecture. They are widely used for signed multiplication i.e. for both negative and positive numbers. We have now designed a Braun multiplier (BM) to improve the speed, power and area capability. We are using the Xilinx tool to verify Braun multipliers using Verilog. We are taking the following considerations: checking using FPGA based instruments and implementing code using Verilog-VHDL. The adders are integrated into multipliers. The result of this research is to modify BM to improve the performance along with reduction in power consumed and also using less area.***
Keywords: Verilog, FPGA, Power Consumed, Parallel processing Architecture, Digital signal processing.

I. INTRODUCTION

An elementary arithmetic operation is multiplication. They are used in many DSP applications, including filtering and FFT, and they frequently cause large delays in processing times and occupy a sizable portion of silicon in DSP systems.

Multipliers are essential components in digital signal processing and FPGA-based applications, perhaps because they consume more power and space than other devices. Multipliers, which in turn depend on adders, are essential components of DSP and FPGA-based systems because they provide power, speed, and area. Therefore, the latency can be reduced by using adders.

The need for efficient operations that involve multiplication is growing due to the increasingly complex nature of today's computer tasks. With its creative design, the Braun Multiplier offers a workable answer by reducing the number of required processes. This makes it a viable option for applications requiring accurate and speedy multiplication, such as digital signal processing and encryption. Verilog offers a variety of abstraction levels at which the behaviour of the Braun Multiplier can be explained, from the high-level algorithmic view to the low-level digital implementation. We can simulate the Verilog model to confirm its validity, optimise its efficiency, and validate its usefulness.

This work is organised to provide a succinct overview of some of the innovative methods and techniques that different authors have used to discuss Braun multipliers that use FPGA.

Figure 1 illustrates how a Kogge stone adder and Braun multiplier were employed in one of the publications that we examined to increase the area yet decrease the delay. Kogge Stone Adder and Ripple Carry Adder findings were additionally compared in this study.

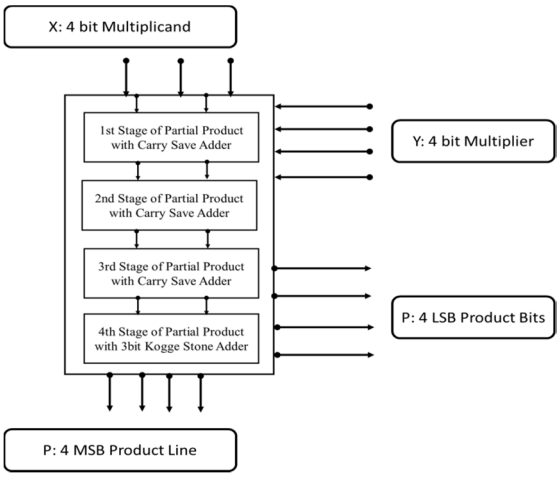


Figure 1: The Braun Multiplier with Kogge Stone Adder block diagram shows four stages.[14]

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A different study offered an innovative form for creating and evaluating a Braun array multiplier; they used multiplier modelling and simultaneous prefix adders to boost the multiplier's functionality. The multiplier multiplies binary numbers more quickly by utilising the 4-bit precession and ripple carry adder. The results show that the new techniques can be used to construct and analyse the multipliers.

A Field-programmable Gate Array (FPGA) is a kind of integrated circuit designed exclusively to be incorporated into another one. The FPGA's layout is designed to facilitate a wide range of operations. The hardware Braun's Multiplier implementation in the Virtex-4, Spartan-3E, and Verilog HDL has been investigated in this article. The multipliers were developed in Verilog HDL, synthesised, and simulated using ISE 11.4 Design Architect after being executed in ISE 12.4 design tool.

Along with simulation and multiplier synthesis, the Braun Multiplier can also be implemented in FPGAs deploying various FPGA platforms, such as Spartan-3E, Virtex-4. The Braun multipliers can be executed on Field Programmable Gate working with a range of technologies and resources, as we will describe further. FPGAs are extremely versatile and adaptable integrated circuits, which are chips that can be tuned and set up for a variety of purposes, methods and techniques as shown in Table 1.

Xilinx (version 14.7) ISE design tools along with Verilog (version 14.7) HDL are the primary application programs used in implementing the Braun multipliers onto FPGAs.

S.No.	FPGA	Delay for Braun Multiplier using Ripple Carry Adder (ns)	Delay for New Braun Multiplier using Kogge Stone Adder (ns)
1	Spartan 2 (xc2s 15-6cs144)	16.019	15.929
2	Spartan 2 (xc2s 200-5fg 256)	18.446	18.346
3	Spartan 2E (xc2s 100e-7ft 256)	14.251	14.161

Table 1: Evaluation outcomes between the FPGA version of the Braun Multiplier with the Kogge Stone Adder and the Ripple Carry Adder.

A Framework of the core recommendations and a certain degree of expertise anticipated for the demonstrated work is provided as: Among the FPGA applications include the following, An integrated circuit that can be enhanced for a number of uses is referred to as a field programmable gate array, or FPGA. Additionally, we have explored the FPGA platforms for implementing Braun's Multiplier in this study's methodology.

Four-bit precession and ripple carry adder: This multiplier, which has its foundation on the ripple carry adder, uses four bits of precession to multiply binary integers with greater efficiency. Although it brings about carry in O [log n] instances, the Kogge stone adder—a parallel prefix form carry look-ahead adder—is most frequently referred to as the world's fastest adder.

Verilog prototypes of Braun multipliers can be generated using various abstractions levels, from the highest-level algorithmic explanations to more primitive digital automation implementations. Test benches serve the purpose for behaviour validation and outcome endorsement during functional verification using simulations.

By moving to a lower level of abstraction and time analysis, limitations can be achieved and productivity can be optimised. In order to achieve project goals while striking a balance between accuracy, performance and functionality, the method involves continually changing design adjustments and comprehensive records.

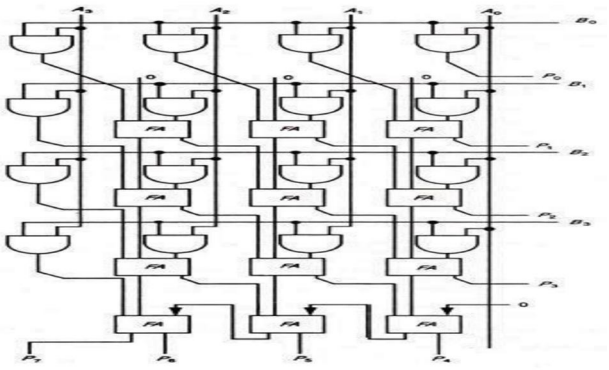


Figure 3: Braun multiplier

II. LITERATURE REVIEW

In the paper named "Implementation of parallel multiplier based on Booth computing method using FPGA"[1] proposed by B. Jeevan, P. Samskruthi, P. Sahithi and K. Sivani in the year 2022, put forward a method using booth encoding which was developed for partial products. This process is divided into two parts. The final product is considered as the third part. This paper provides various architectures of multiplication. It also gives us information that the parallel multiplier is faster as compared to serial multiplier. In this paper they have discussed the serial of action.

In the first step we get partial products, in the second step we add the two rows and get the result in two rows, in the last step we obtain the final result. This multiplication is performed using the booth encoding method in this paper. To get the partial product booth encoding scheme is proposed for obtaining the operational stability from the existing plans. During multiplication the partial product addition is obtained with martial product reduction tree or OPPT method.

In the year 2020 a paper entitled “Design of High-Speed Multiplier using Parallel Prefix Adder” [2], presented by N Venkateswara Rao, B Navya Surya Ratnam, et al. this paper presented the idea that different types of Kogge stone adder developed using various logic gates can be used like 22T XOR,14T XOR and 12T XOR. This paper compares the new model of Braun multiplier with the old method with reference to delay.

Taking the new method the 22T-XOR Kogge stone adder has 222 transistors and gives a delay of 101.01ps. The 14T-XOR Kogge stone adder has 174 transistors and obtains a delay of 152.91ps. And the last 12-XOR Kogge stone adder has 162 transistors and gives a delay of 21.03ns. The new method of Braun multiplier has inputs equal to 4X4 and outputs equal to 8. We have more output pins because a large delay is produced at the output side. The output pins are replaced with Kogge stone adder to reduce the delay.

In a research paper “Design of Efficient Braun Multiplier for Arithmetic Applications” [3] proposed by Telagamalla Gopi in the year 2020, this paper suggested the concept of using pyramid adders. In applications like DSP and FPGA- based applications, multipliers are used as they require more power and area as compared to other devices. Area, power, and speed are considered as the most important features in applications like FPGA and DSP. All the above parameters depend on multiplication which then depends on adders.

Using pyramidal adders which have both the half adder and full adder increase the performance and reduce the quantity of gates required in the multiplier and also decrease the latency. The modern pyramidal adder that contains XNORs and MUX instead of full adder and half adders uses less gates and less delay is used. As MUX selects only one output among many inputs. Using XNOR and MUX in pyramidal adder reduces the delay.

A paper titled “Comparative study of Braun’s Multiplier Using FPGA Device "[4] was given by Anitha R, Bhagya Veereswaran V in 2019. In this paper a bypassing method is proposed to decrease the computation delay and enhance the use of resources. For designing the Braun multiplier, it is comparing column bypassing and row bypassing technique along with full adder is replaced with fast adder. In this paper it is implemented on Virtex 6, Virtex 5 and Spartan 3E.

In this paper they have also used fast adder to decrease slices. The value of delay and look up table is also decreased in comparison to the ol method. It is found that Virtex-6 uses a less powerful FPGA chip which has reduced combinational path latency and also decreased the average pin delay. Hence comparing an FPGA device with virtex-6, virtex-6 gives better results with low power. Braun multiplier is mainly used in applications like image processing, multimedia technology and digital signal processing.

A research conducted on ‘An Efficient Multiplication of Braun and BW Multiplier’ [6] authored by K.Sireesha, Dr.T. Lalithumar, T.V.Nirmala, and S.Haneef during 2018. This paper tells us about the usage of multipliers in the field of signal processing and digital signal processing. This paper also tells the importance of using Braun multipliers that can be used for multiplying positive and negative numbers in parallel architecture.

The paper also looked into the design of adders based on CMOS, split path data driven dynamic logic and domino dynamic logic. The important conclusion that we can obtain from this paper is that it reduces the power consumption as well as the delay, which in turn improves the speed and also decreases area in the circuit. The changes made in Braun multiplier and BW improved the performance of the multiplier in comparison to the old design and hence making BM a important component in DSP applications.

A paper titled “Novel Approach to Design Braun Array Multiplier Using Parallel Prefix Adders for Parallel Processing Architectures” [7] by Kunjan D. Sharma, K.D. Amit Kumar, D.S. Rashmi, H.R. Shilpa, and C.R. Vidashree in 2018. This paper focused on the approach of design of Braun array multiprocessor (BAM) along with Parallel prefix Adders (PPA). It's all so known for its fast carry generation network and are the highest speed adders available.

The study of brent kung, Kogge stone and other common types of PPA adder is being conducted to find the worst possible scenario in terms of delay, power consumption and number of transistors being used along with little emphasis on low power being consumed.

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This method shows the importance of adders and microprocessors to meet the speedy processing necessity of current signal processing systems.

A research paper titled “A Review on Various Multipliers Designs in VLSI "[9] proposed in the year 2015 by Khuraijam Nelson Singh and H. Tarun kumar introduced a novel design. A dual array tree structure and the temporal tilling method are used in the design. We also study several approaches to the optimization of Wallace array multipliers. We have built a low power array multiplier with a modified booth encoding method, based on the Nikhilam sutra. The performance of the new multiplier is 30% and 50% better than that of the conventional CMOS.

In spite of being the most power-hungry and delayed part of the research, Shivaling S. Mahant's demonstration indicates that the array multiplier may be effectively optimised. Choi Junghwan and associates (2000) and Shetti and associates (1999). With Booth encoding, the Wallace tree multiplier is the fastest and most efficient optimization for improved display. Effective planning of a Wallace tree multiplier with Booth encoding can also be achieved as a pipelined structure, as shown by Rahul D. Kshirsagar and colleagues (2013) to rise.

Jyoti Sankar Sahoo and Nirmal Kumar Rout are the authors of the 2015 book "Comparative Study of Different Low Power Designs of Braun Multiplier using Double Gate MOSFET at 45nm Technology" [10]. This study focuses on the AND gate and double gate MOSFET designs used in the Braun multiplier. An essential component of the multiplier structure is the AND gate. The Cadence program is utilised in the implementation of the AND gate and power multiplier designs. The results are given for different designs of Braun multipliers.

This paper discusses the design of a low-power Braun's multiplier using three different low-power technologies and a double-gate MOSFET in a full addition. A power delay product is appended to the delay product. We make comparisons and computations between the three designs. Using a complete DOUBLE-TOUCH MOSFET adder and a DOUBLE-TOUCH MOSFET sleeping array of AND doors, the third design demonstrates how technology can be preserved while improving power savings. dissipation of power delay products, delay, and energy. In 45 nm and Cadence Virtuoso Tool technology, three low-power, high-speed Braun multifunction are utilised.

A Research paper titled "Braun's Multiplier Implementing FPGA Using Bypassed Techniques" was released in 2011 [15]. Using Kogge Stones adders in conjunction with the Braun Multiplier's capabilities, Anitha (R) and Veereswara (B) demonstrated a revolutionary multiplication method. Using a normal digital multiplication technique, the Braun Multiplier consists of a [N-1] Carry-Save Adder and a Ripple Carry Adder. The new Braun Multiplier that was suggested and the current one were compared in research.

To determine the advantages and disadvantages of the new Kogge Stone multiplication method, the research evaluated factors such as speed, area use, and performance. Kogge Stone and Adder This adder has a great reputation due to its fast carry bit computation. It is incorporated to improve performance even if it takes up more space. A few of the many applications for the adder are data preparation, result handling, and prior processing. It can generate carry signals with O(log n) temporal complexity and amazing efficiency. There is a noticeable decrease in the total latency of the adder.

The Research was titled "Braun's Multiplier Implementation using FPGA with Bypassing Techniques" In order to create Braun's Multiplier, Anitha R. Bagyaveeraswaran V., India, [15] conducted research using the "fast addition" method in combination with FPGA technology and cutting-edge bypassing techniques. This research was motivated by the prohibitively high cost of developing ASICs and the fact that multipliers are essential operations that support a wide range of applications, such as digital signal processing (DSP) and image processing.

Braun multipliers can be implemented in FPGAs at a lower cost using FPGAs. A comparison of FPGAs based on various platforms (Spartan-3E/Virtex-4/Virtex-5) and FPGA Low Power (Virtex-6) is included in the study. The following are the study's findings: The number of slices, delay, and LUTs used are much less than in typical architectures.

A research article titled "Design and analysis of low power Braun multiplier architecture" was published [16]. The primary objective of the research is to investigate the potential power dissipation caused by multipliers within Digital Signal Processing, or DSP, blocks. The main source of power dissipation in these kinds of applications is multipliers. The ways to achieve power optimization across different CPU modules are also examined in the current investigation.

The study offers a thorough examination of the various ways that DSP blocks, multipliers, and other elements contribute to power dissipation. It also examines the various power-optimization strategies for CPU components. The research concludes with a comparison of the power and design achievable utilising low-power sign array multipliers. Full and partial adders are the fundamental building blocks implemented in the paper and are thought to be crucial for multiplier creation. After including such low power adders into its suggested multiplier architecture, the paper evaluates the results.

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III. EXPERIMENTAL DETAILS

A. Hardware and Software Requirements:

1) FPGA development board (e.g., Xilinx Spartan-3E)
2) Verilog coding tool (e.g., Xilinx ISE)
3) ISIM Simulation and synthesis software

Typically, an FPGA application stores configuration images in a single, non-volatile, memory. Illustrating the new capabilities of the kit board, it has three different configuration memory sources, all of which need to work well together.
The additional configuration functionality makes the starter kit board a bit more complicated than typical applications in the Spartan-3E FPGA family. On-chip circuitry simplify the device programming experience in typical applications.

B. Braun Multiplier Implementation:

1) Xilinx ISE software will be used to write and synthesis the Verilog code for the Braun multiplier.
2) The design will be implemented on the FPGA development board.
3) The Verilog code will be mapped to the FPGA device during implementation, and it will be programmed to carry out the multiplication operation.

C. Testing and Verification:

1) The functionality of the Braun multiplier will be verified through simulation using the Verilog testbench.
2) To ensure the accuracy of the result, test vectors will be fed into the multiplier.
3) To make sure the multiplier is operating as intended, the simulation's output will be examined.

IV. THEORY

A. RTL schematic and Technology Schematic

The Register Transfer Language (RTL) describes the implementation logic of a memory chip circuit. RTL design is an abstraction level in digital circuit design. It describes the behaviour of the circuit in terms of the data flow between the registers, as well as the logic that processes that data as it flows between the registers.
RTL design refers to the process of describing a circuit's behaviour by describing the data flow between registers, as well as the logic used to manipulate that data. Verilog, an HDL (Hardware Description Language), allows engineers to describe how data flows between registers, and how it's processed by the combined logic between those registers.
This approach allows engineers to provide a detailed description of the operation of a circuit, while abstracting from the details of the physical implementation. By concentrating on the data flows and logic operations of a digital circuit, the RTL design process allows for efficient simulation and verification, as well as synthesis, of digital circuits.
RTL design is a fundamental abstraction in the field of digital circuit design, providing a bridge between the high-level concepts of design and the details of hardware implementation.

B. Technology Schematic

A technology schematic is a visual representation of how a digital system such as the Braun multiplier works. It describes the structure and connections of important parts such as AND gate and adders. It explains the binary multiplication process, making it easier to understand, design and analyse.
A technology schematic is essential for the engineers and designers who are responsible for implementing the multipliers in digital hardware. It allows them to plan and troubleshoot and optimize the performance of the system.

V. RESULT

A. RTL Schematic

Figure 4 showcases the layout design of RTL Schematic for Braun Array Multiplier

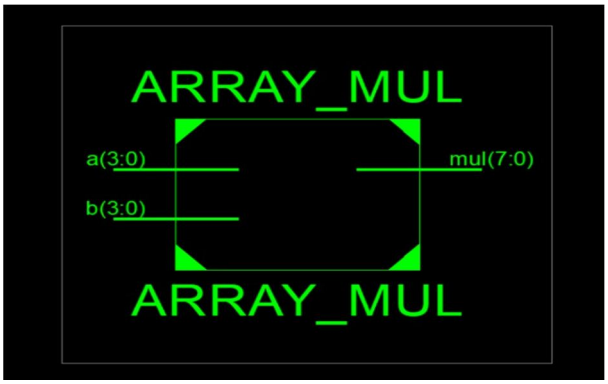


Figure 4: RTL Schematic for Array Multiplier

The following diagram Figure 5. showcases the detailed schematic for the designed Braun multiplier with proper specifications.

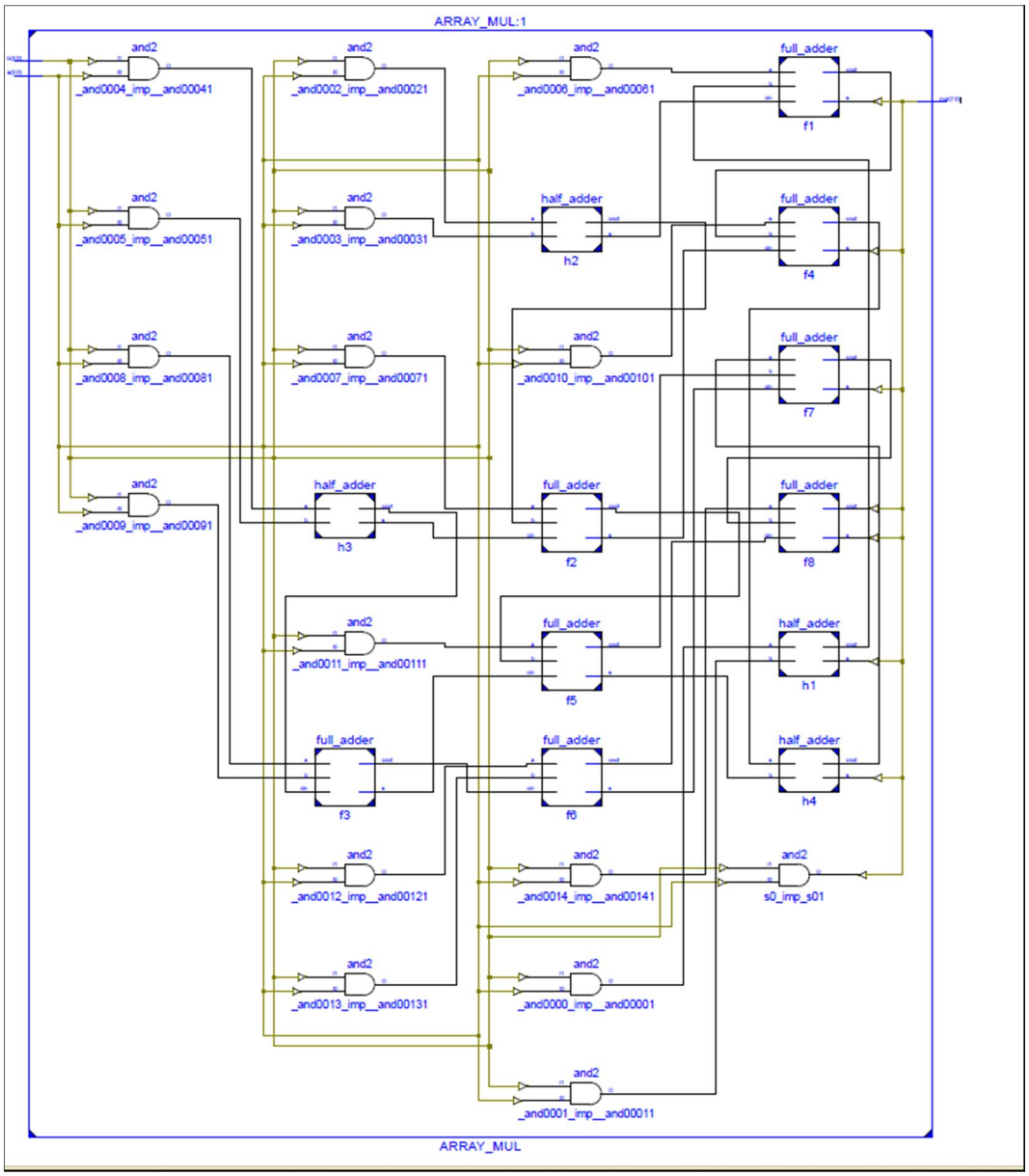


Figure 5: Detailed RTL Schematic for Array Multiplier

The following illustration Figure 6 shows the Technology Schematic of Braun Multiplier:

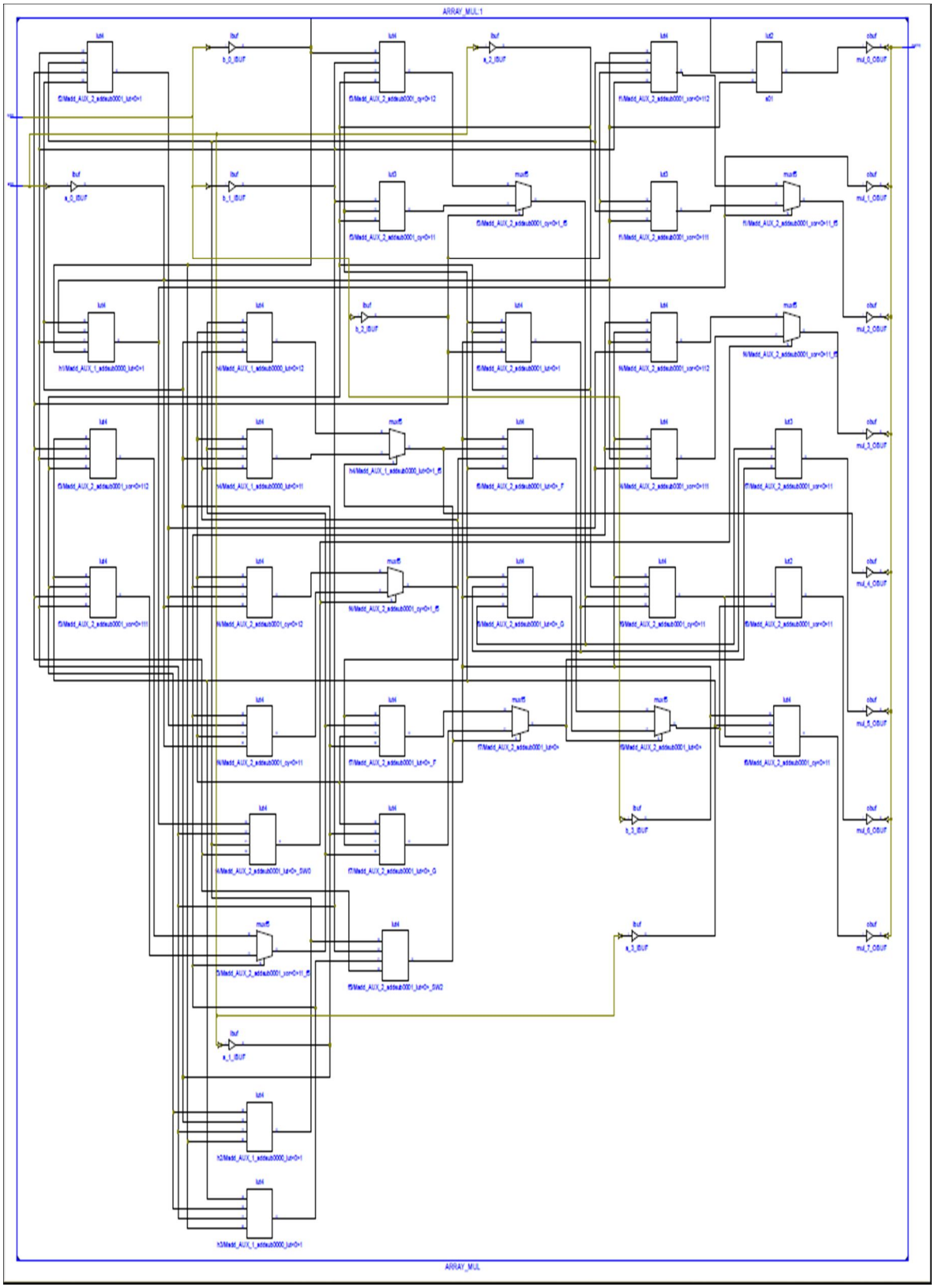


Figure 6: Detailed Technology Schematic for Array Multiplier

B. Look Up Table (LUT):

1) Half Adder

- *Synthesis results of Half Adder*

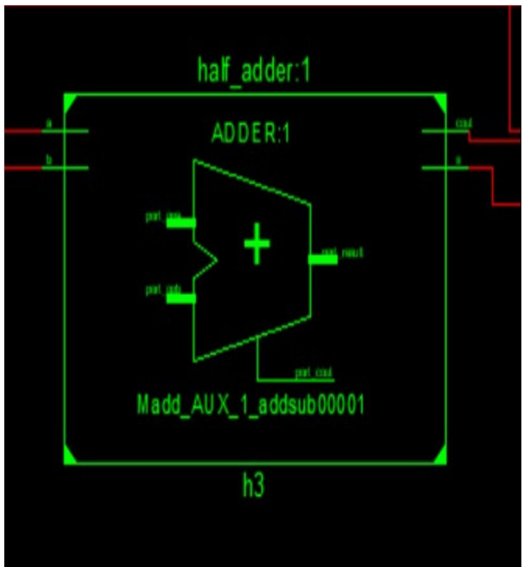


Figure 7: Layout of Half Adder

- *Schematic of Half Adder*

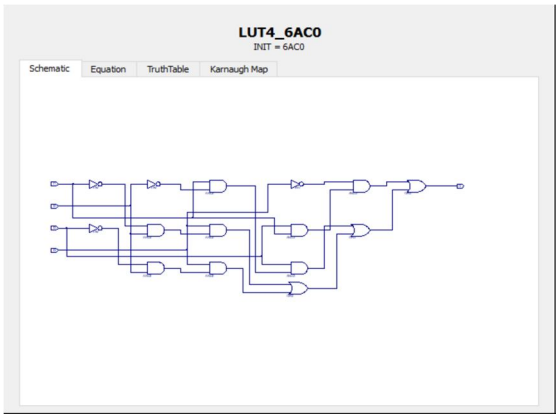
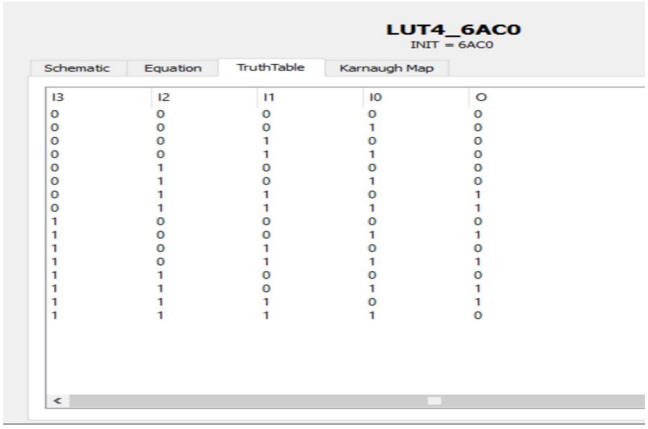


Figure 8: Schematic of Half Adder

- *Truth Table of 4 Input Half Adder:*



I3	I2	I1	I0	O
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Figure 9: Truth Table of 4 Input Half Adder

- *K Map of Half Adder*

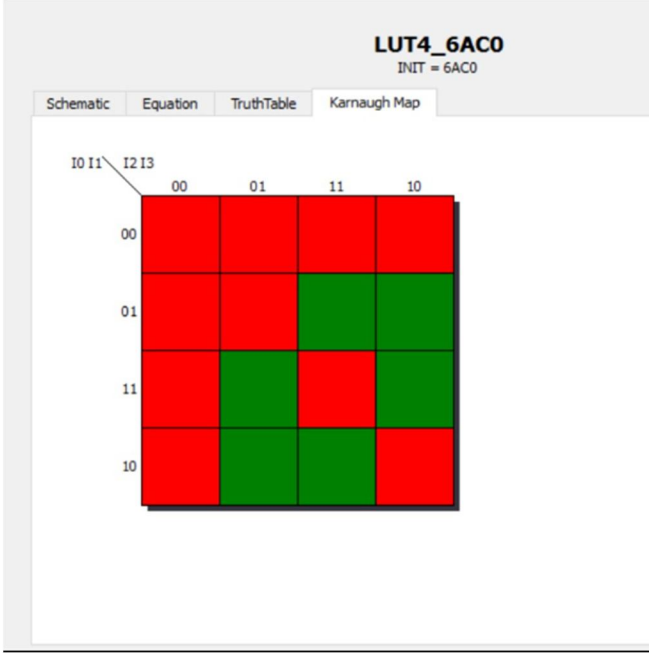


Figure 10: K Map of Half Adder

2) Full Adder

- *Synthesis Results of Full Adder*

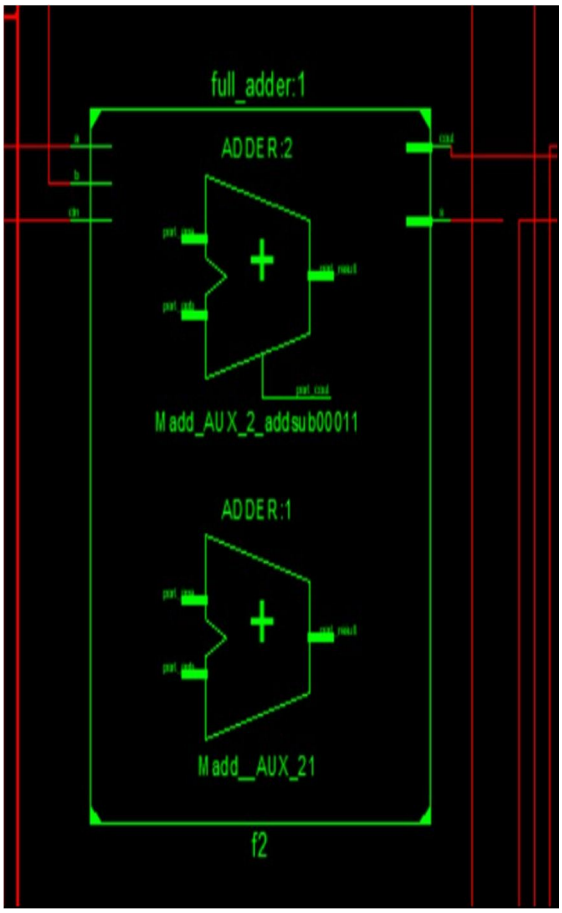


Figure 11: Layout of Full Adder

- *Schematic of Full Adder*

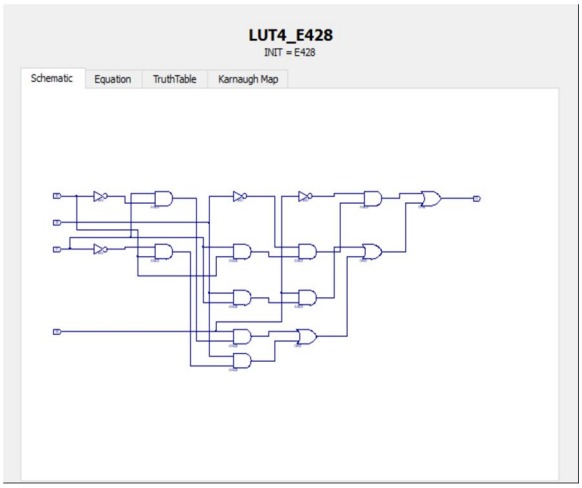
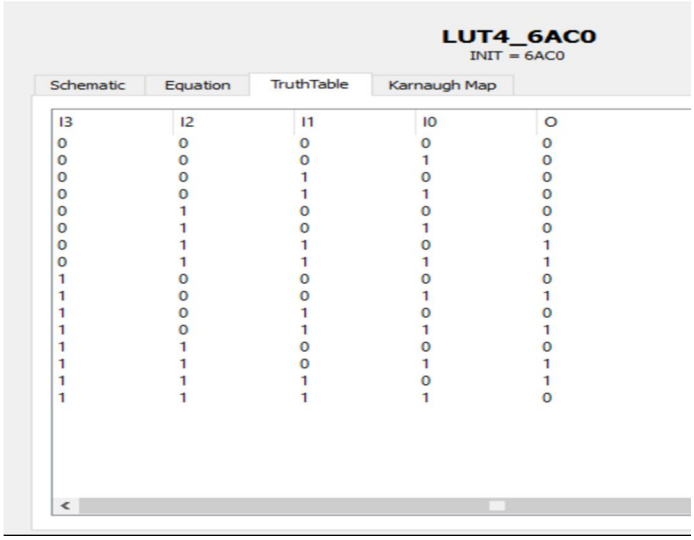


Figure 12: Schematic of Full Adder

- *Truth Table of 4 Input Full Adder*



I3	I2	I1	I0	O
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Figure 13: Truth Table of 4 Input Full Adder

- *K Map of Full Adder*

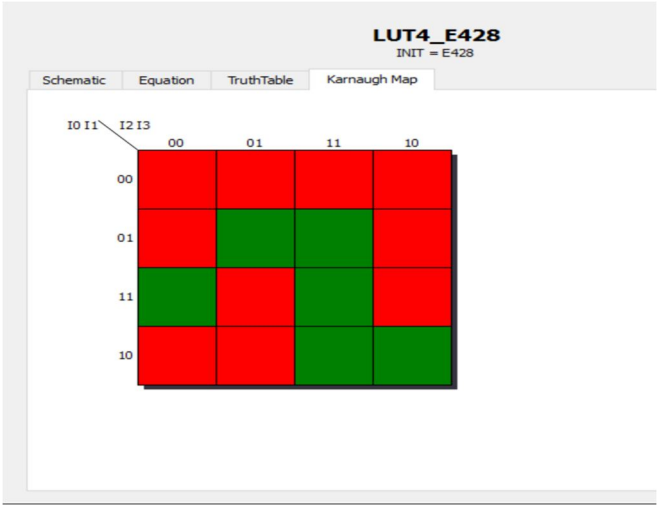


Figure 14: K Map of Full Adder

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C. Waveforms and Multiplication Results

One popular hardware for effectively multiplying two binary values is the Braun multiplier. In this project, we introduce the Braun multiplier, which is synthesized using FPGA and stimulated using the Xilinx ISE Webpack design suite 14.7. This project aims to implement a 4-bit Braun multiplier and verify its functionality through simulation and synthesis.

The purpose of the testbench is to supply inputs to the multiplier and confirm that the result is accurate. To verify that the multiplier functions properly for every possible combination of inputs, the simulation results are examined. According to the simulation findings, the multiplier generates the right output for every possible input combination.

The synthesis findings demonstrate that the design can be effectively programmed into an FPGA for real-time operation and that it satisfies the timing requirements. Here we have presented the output results of the Braun multiplier for various types of signals i.e. binary, hexadecimal, unsigned, signed, and octal.

The simulation results are shown below:

1) Unsigned Decimal

The base ten numbers or the decimal numbers are represented as a sequence of numbers, with each position having a value in terms of a power of ten. The base ten numbers are written using a sequence of numbers: (0), (1), (2), (3), (4), (5), (6), (7), (8), (9).

The following waveforms (Figure 7, Figure 8 and Figure 9) demonstrates the multiplication output for the same at different time stamps:

- *Time stamp (45.263 ns)*

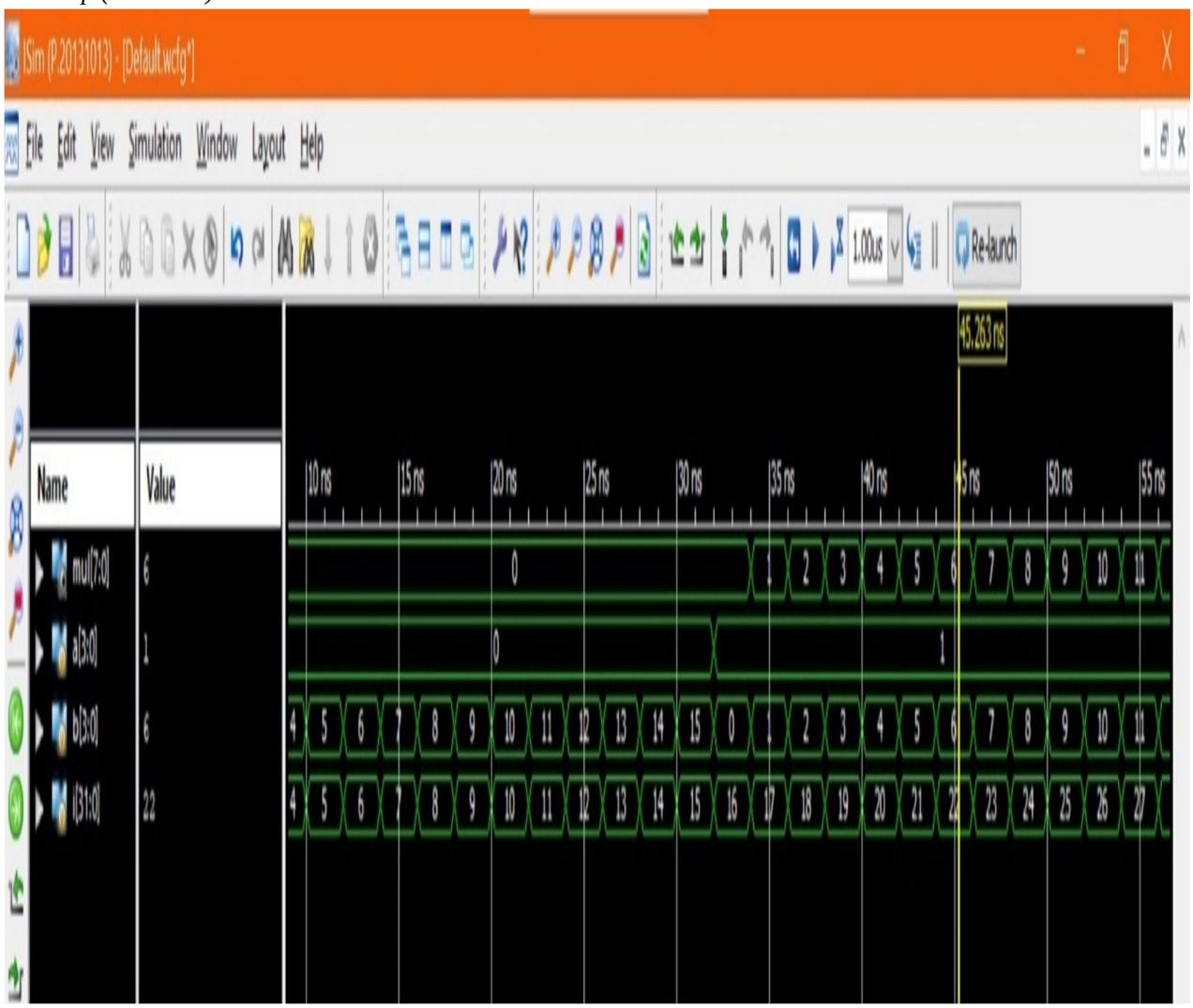


Figure 15: Unsigned Multiplication

- *Time stamp (246.623 ns)*

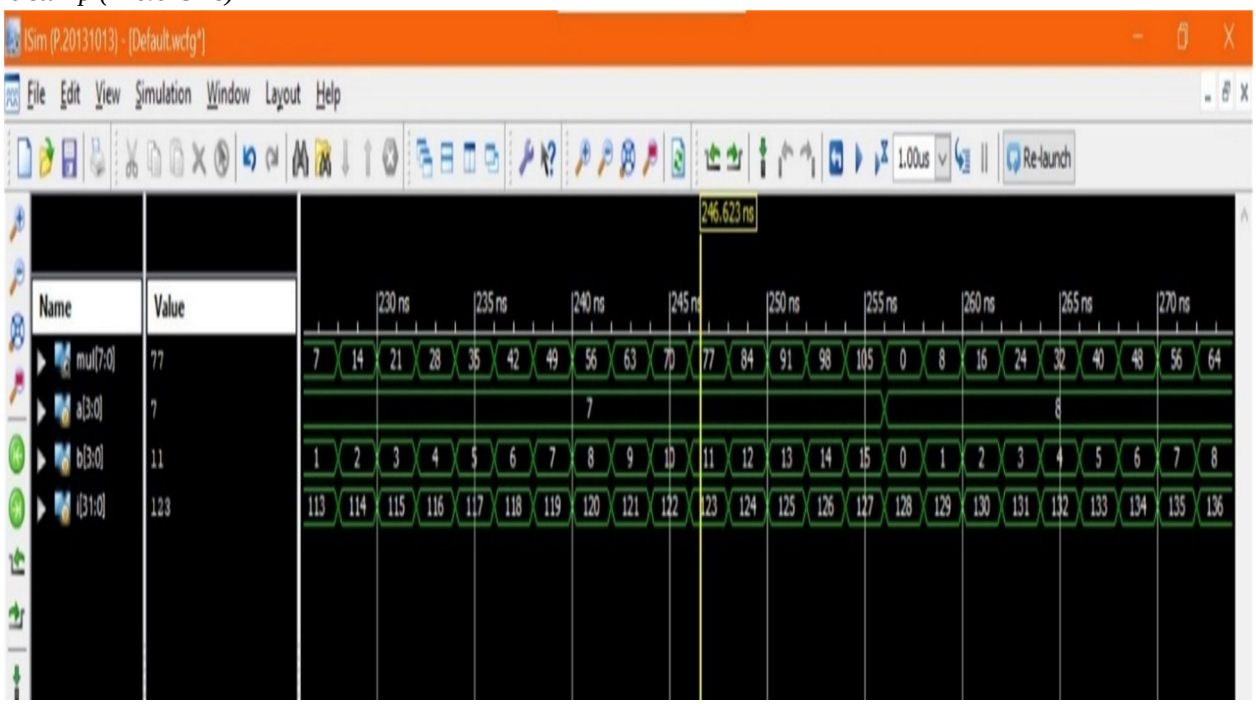


Figure 16: Unsigned Multiplication

- *Time stamp (510.257 ns)*

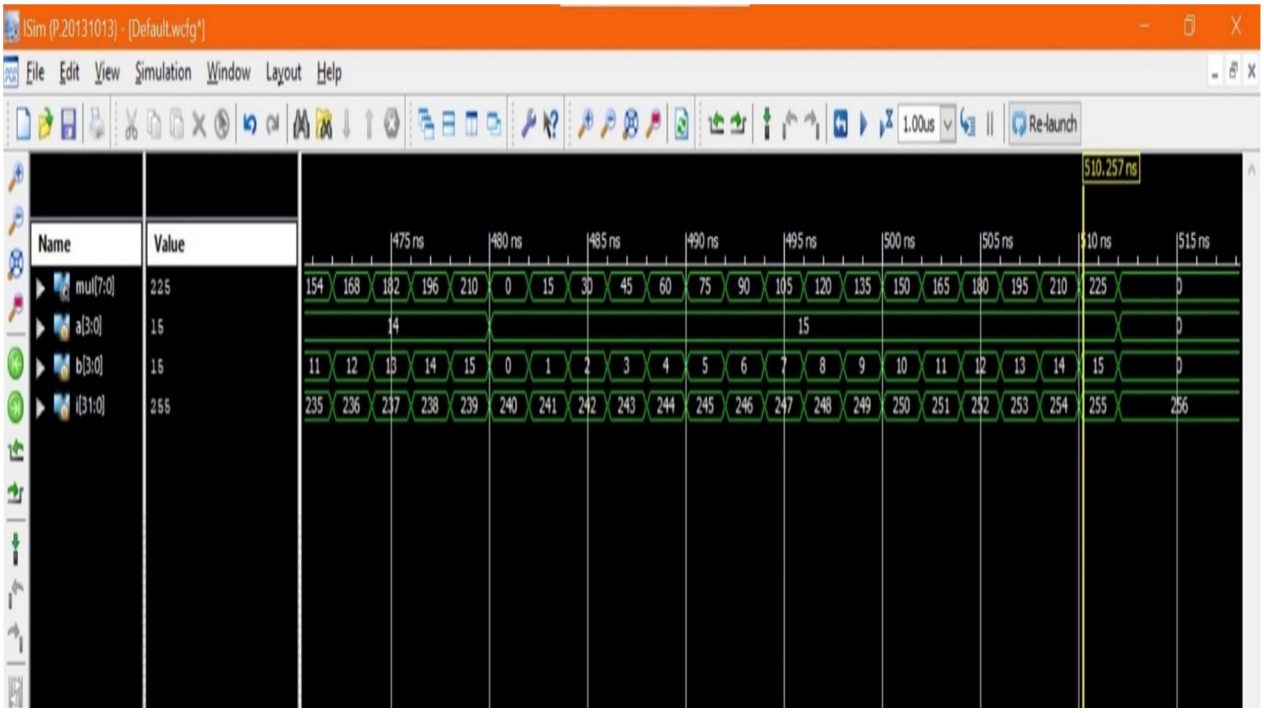


Figure 17: Unsigned Multiplication

2) Signed Decimal

When we multiply and divide signed numbers, we begin with the operation on the absolute value of the two numbers. If both numbers have equal sign, the result is positive. If they have opposite signs, the result is negative.

Signed numbers have sign flag. This symbol indicates the difference between a positive and negative number. This method includes sign bit and the size of the number. For instance, to represent a negative decimal number, we have to add a negative symbol before the decimal number.

The following waveforms (Figure 10, Figure 11 and Figure 12) demonstrates the multiplication output for the same at different time stamps:

- *Time stamp (39.667 ns)*

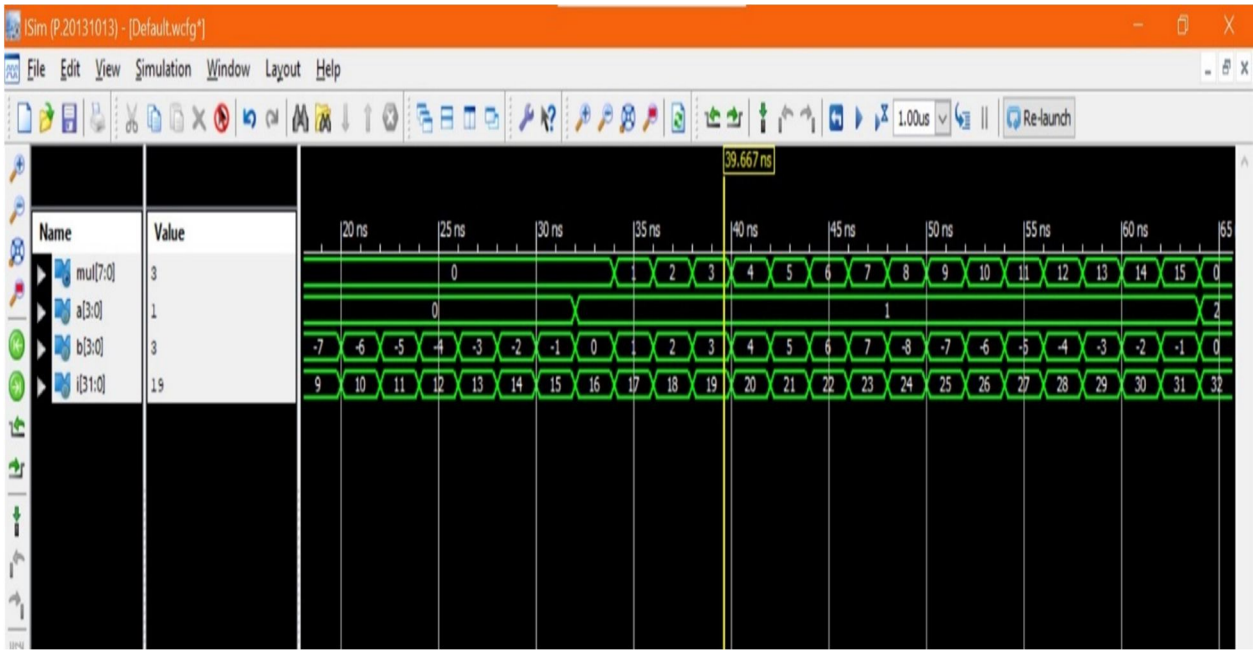


Figure 18: Signed Multiplication

- *Time stamp (350.757 ns)*

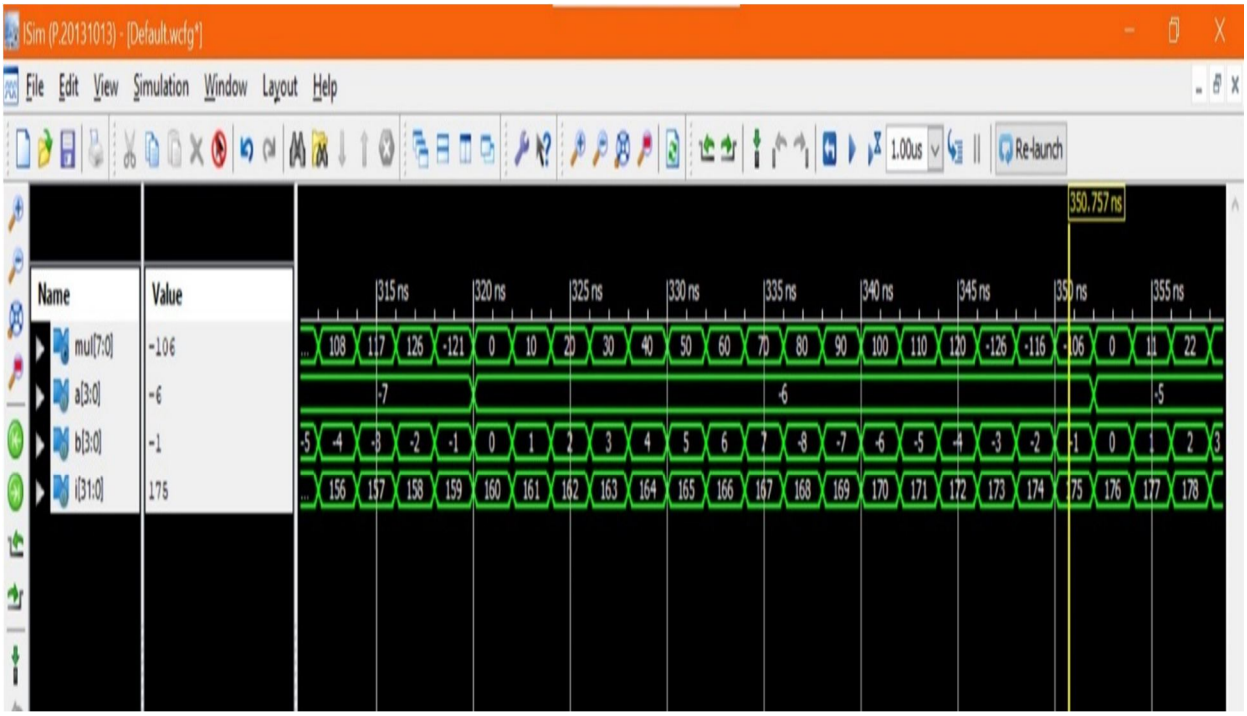


Figure 19: Signed Multiplication

- *Time stamp (498.740 ns)*

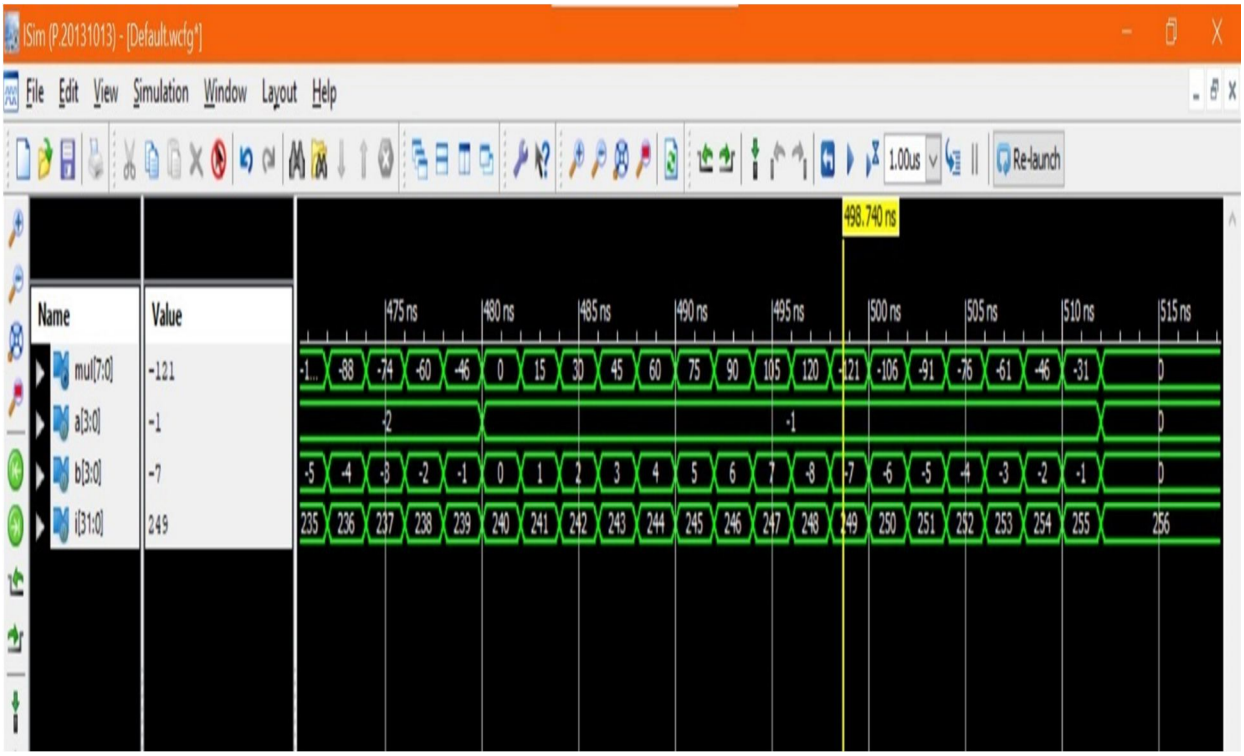


Figure 20: Signed Multiplication

D. FPGA Implementation

Field-programmable gate arrays (FPGAs) are a type of semiconductor device that consists of a number of programmable logical blocks and configurable interfaces. Unlike ASICs, which are designed for a particular purpose and fabricated as fixed-configuration devices, FPGAs can be programmed and reconfigured after manufacturing.

In the past, FPGAs were chosen for lower speed/ complexity/volume designs. Today, FPGAs can easily exceed 500 MHz performance. In addition to unprecedented logic density increases, FPGAs offer a wide range of other features such as embedded processor, DSP block, clocking, high-speed serial, and even lower price points. FPGAs are an attractive proposition for almost any design.

The FPGA (Field Programmable Gate Array) Implementation of Braun Array Multiplier is given in the following figure:

VI. CONCLUSION AND FUTURE SCOPE

In this paper we have presented a Braun multiplier using carry save adder and ripple carry adder. We have implemented it using Verilog language and design using Xilinx ISE Webpack design suite 14.7. We have designed this multiplier so that it can reduce the delay and hence it can give the best results in terms of speed, area and power as compared to the conventional multipliers. We have designed this multiplier for signed multiplication so that we can get more precise results. The conventional multiplier is designed using full adders and AND gate which uses more delay and power. This type of multiplier is widely used in applications like Digital Signal Processing and image processing where the response of the system is much more important than the cost.

Future Scope

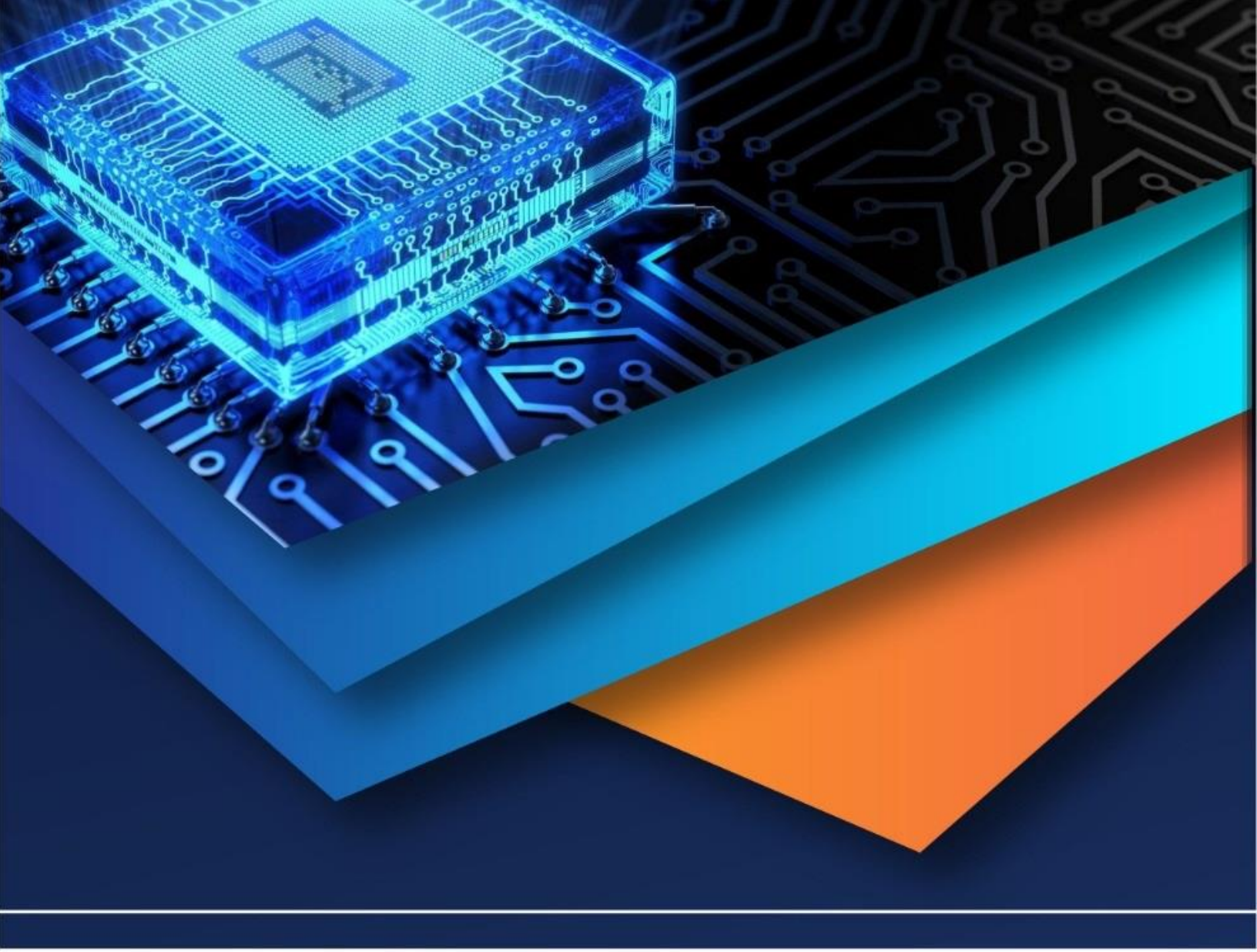
1) *Optimization*: There is always room for improvement in terms of area, power, and performance. Researchers might look at low-power design techniques, pipelining, and parallelism to increase the efficiency of the Braun Multiplier.
2) *Scalability*: Currently, the Braun Multiplier is used to perform 4x4 or 8x8 bit multiplication. In the future, the focus should be on increasing the Braun Multiplier's ability to handle inputs with larger bit widths, such as 16x16 or 32x32 bits.
3) *High-level synthesis*: High-level synthesis (HLS) tools can be used to automatically construct Braun Multiplier designs from a high-level description (like C/C++ code). This could help save design time and increase output.

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4) *Verification*: This is an important phase in the design of digital circuitry. Researchers may consider using advanced verification techniques such as hardware acceleration, limited random testing, and formal verification to ensure the accuracy of Brownian multiplier designs.
5) *FPGA implementation*: A field-programmable gate array (FPGA) can be used to house the Braun multiplier for hardware acceleration. In order to attain better performance, future research may focus on refining the architecture of FPGA implementations, exploring different architectural choices, and concentrating on certain FPGA families.

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