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# Design and Implementation of Efficient IIR Low Pass Filter Based On Vedic Multiplier Algorithm

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***Abstract:*** ***This article presents a state-of-the-art design for a limitless impulse response (IIR) filter that can be easily reconfigured for use in real-time software. Using a vedic multiplication strategy, this work demonstrates the excellent general performance of a recursive or Infinite Impulse Response (IIR) filter. The number of repeats may be kept to a minimum and the processor's overall performance is improved by the reduction of computational delay and hardware. This research investigates the impact of different filter architectures on the development process and overall performance. To enforce and evaluate the planned filter's functionality, simulation is used across three independent platforms. The first system is MATLAB/ SIMULINK, the software package utilised to implement the IIR filter. The second strategy is called "HDL - Cosimulation," and it involves using SIMULINK's already-present tools in order to translate the formulated filter-out method into VHDL, the language used to describe very fast integrated circuits. The third approach uses Xilinx System Generator's pre-existing building components to physically realise the filter design. The method shown here allows the proposed filter to be implemented locally inside the FPGA device of interest..***

***Keywords:*** ***IIR Filter, Vedic Multiplication, Urdhva Trigbhyam Sutra, Matlab, LUTs, delay.***

## I. INTRODUCTION

A multiplier is a crucial part of many high-performance systems, such as FIR filters, IIR filters, microprocessors, virtual signal processors, and so on. Because multipliers are often the machine's slowest component, their performance often determines the device's overall effectiveness.

It also takes up the most room on average. As a result, achieving the best possible balance between the multiplier's speed and its surrounding components is a challenging but worthwhile design challenge. Improving speed often only yields noticeable results across vast areas, however, since location and speed are typically competing restrictions. Therefore, a wide range of multipliers with varying area-speed requirements were developed using a fully parallel architecture.

When it comes to digital signal processing, digital filters are essential. The exceptional results they consistently provide are a major factor in DSP's meteoric rise to prominence. Filters may be used for a variety of purposes, including signal isolation and restoration. When the signal is contaminated by noise, other signals, or interference, signal separation is necessary. Take, as an example, an electrocardiogram (EKG) used to monitor foetal heart rate. The raw signal may be distorted by the mother's breathing and heartbeat. In order to evaluate each signal independently, a filter must first be utilised to separate them. Recovering a signal after it has been corrupted in many ways is called for in certain situations. In order to more accurately portray the sounds as they happened, filters may be applied to recordings created with low requirements. Filtering may improve the quality of a recording that was produced under subpar conditions since the sound is still audible. Deblurring a shot that was taken with a blurry or poorly focused lens, or a shaky digital camera, is another example.

## II. IMPLEMENTATION

Code is built in VHDL for IIR clear out using a specific multiplier set of rules, simulated, and then implemented on Xilinx and the target device, a Virtex5 xc5vlx50t, after filter out coefficients are generated using a MATLAB FDA device. The most popular multiplier set of rules for designing digital filters with a huge number of impulse reactions, taking into account hardware complexity, latency, LUTs, and IO characteristics. The ancient Vedic technique of India, which has been of pedagogical interest, was investigated and shown to be a competitive potential for both high and moderate filter orders. After generating coefficients in MATLAB's FDA device (for a low-pass filter with a direct-shape IIR that is stable), the code is written in VHDL, and the analysis is then implemented on Device- Virtex5 xc5vlx50t.

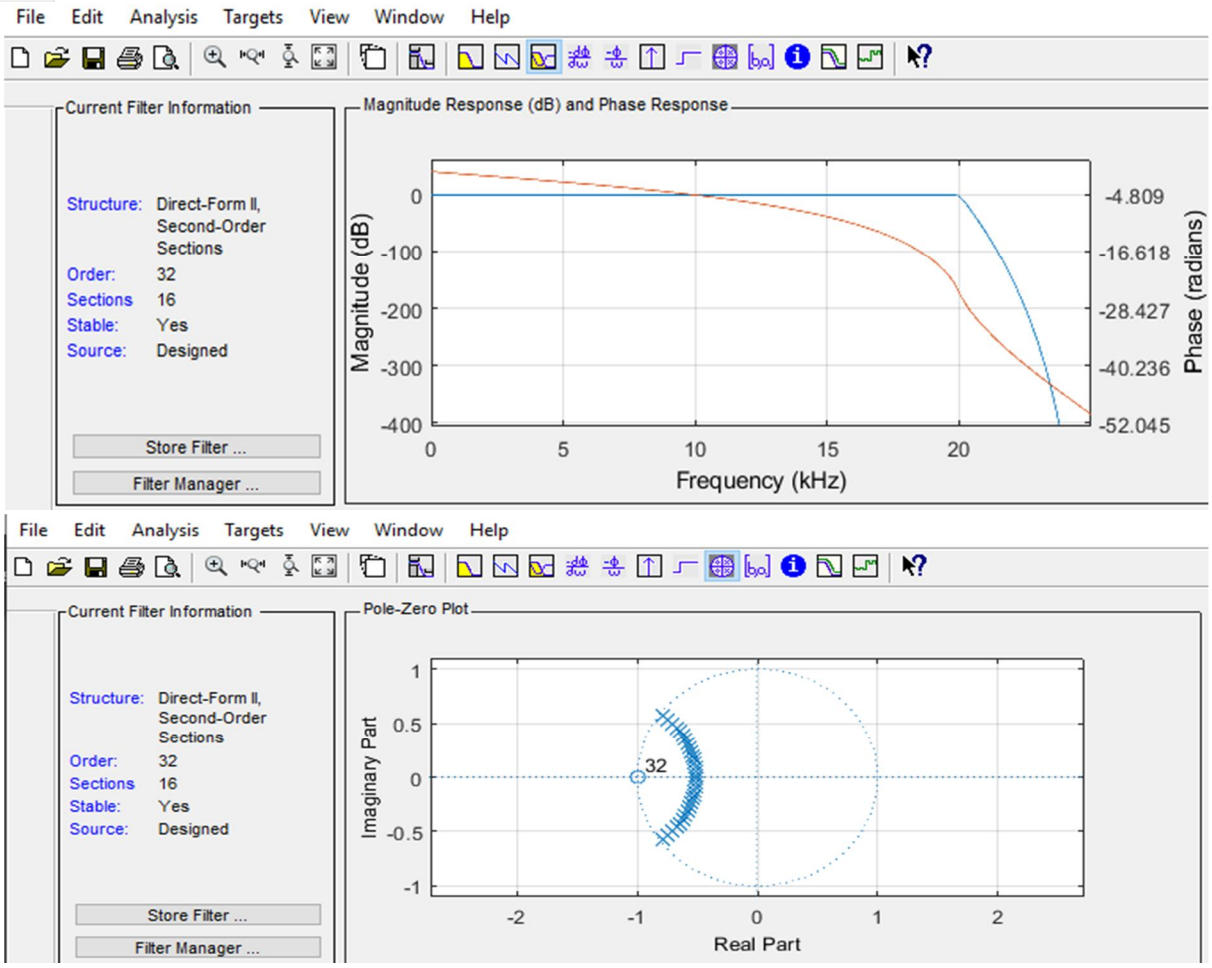



Fig 1. Magnitude and phase response of IIR filter of order 32.

## III. CONCLUSION

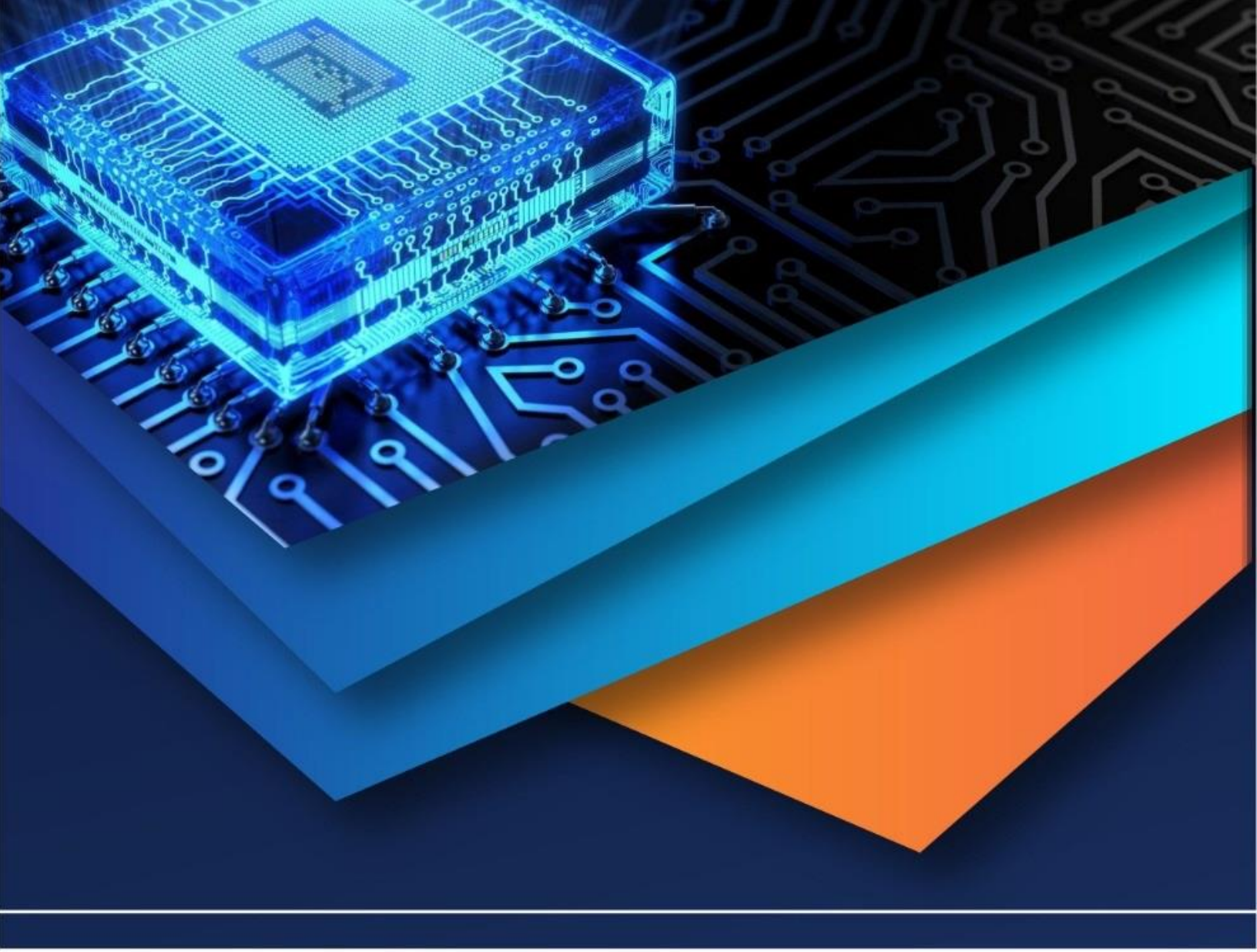
File Table I is structured after simulating, implementing, and evaluating. Vedic set of rules for high order low pass filter with delay of 194.692ns, if memory usage and tool complexity are the high issues, then vedic set of rules with memory 6963680 KB, for designing low pass IIR filter without using Xilinx Device- Virtex5 xc5vlx50t, for the coefficients from MATLAB FDA tool. Many integrated circuit applications are often employed in heat sinks to aid in the dispersion of heat. It has been shown that the higher the number of calculations taking place inside a tool, the more heat it will emit. In a mathematical sense, the Heat emission rises in proportion to the number of Look up Tables (LUTs) used in the filter. This is a higher-order IIR filter built using Vedic Logic with 15,203 look-up tables. It's safe to say that the Vedic criteria work well for the filter order, covering all the bases. Because of this, finding this collection of rules may also aid designer and fabricator in selecting set of rules as compatible with user and marking desires. In audio applications such as hearing aids, where the delay in response determines the counter reaction of the deaf character, the importance of effective IIR filters cannot be overstated. Delay and memory consumption on a device are crucial factors for video and audio applications.

TABLE 1 Implementation of IIR filter of order 4, 8, 16, 32 using vedic multiplier on device virtex 5 xc5vlx50t

| Filter order | Multiplier | Delay(ns) | Logic levels | No. of slice LUTs | Memory (in KB) |
|---|---|---|---|---|---|
| 4 | Vedic | 24.684 | 73 | 1321 | 4798312 |
| 8 | Vedic | 55.107 | 169 | 4737 | 5141960 |
| 16 | Vedic | 103.672 | 348 | 8224 | 5740636 |
| 32 | Vedic | 194.692 | 688 | 15203 | 6963680 |

## REFERENCES

[1] Aaquib Niyama, Sahil Ramane and Neil Chhadwa," Implementation of IIR and FIR filters in Simulink MATLAB and its application in ECG," Researchgate.net,2022.
[2] N. T. Gadawe, T. A. Fathi, S. L. Qaddoori and R. W. Hamad, "Synthesis and Implementation of IIR Filter using VHDL Language," 1st International Ninevah Conference on Engineering and Technology,2021.
[3] Debarshi Datta and Himadri Sekhar Dutta, " High performance IIR flter implementation on FPGA," Journal of Electrical Systems and Information Technology,2021.
[4] Raaed Faleh Hassan, "Performance Investigation of Digital Lowpass IIR Filter Based on Different Platforms," International Journal of Electrical and Computer Engineering Systems, 2021.
[5] K. Keshav Sai Chowdary, K. Mourya, S. Ravi Teja, et al., "Design of Efficient 16-bit Vedic Multiplier".International Conference on Signal Processing and Communication, pp. 214-218, 2021
[6] V.Naresh, G.Kalpana, "Design of 64 bit vedic multiplier using carry look ahead adder," JETIR JOURNAL ,March 2020.
[7] Shraddha Lad and Varsha S. Bendre "Design and Comparison of Multiplier using Vedic Sutras," 5th International Conference on Computing Communication Control and Automation (ICCUBEA), 2019.
[8] Divya, K Surya, K Uma Narayani, et al., "Design of 32 Bit Vedic Multiplier using Carry Look Ahead Adder". Global Research and Development Journal for Engineering, pp. 95-99, 2018.
[9] L Z Shinga,R Hussin, A Kamarudin, S N Mohyar, S Taking, M H A Aziz and N Ahmad, "16X16 Fast Signed Multiplier Using Booth and Vedic Architecture," 4th Electronic and Green Materials International Conference, December 2018.



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