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INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 13 **Issue:** VI **Month of publication:** June 2025

DOI: https://doi.org/10.22214/ijraset.2025.72211

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 13 Issue VI June 2025- Available at www.ijraset.com

Design and Implementation of FIR Filter for 5G OFDM Communication

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Abstract: ***The advent of fifth-generation (5G) wireless communication technology marks a transformative era characterized by unprecedented demands for high data rates, low latency, and enhanced signal integrity. This thesis presents the design and implementation of a Finite Impulse Response (FIR) filter optimized specifically for Orthogonal Frequency Division Multiplexing (OFDM) systems, a core technology underpinning 5G networks. Given the susceptibility of OFDM signals to inter-symbol interference (ISI) and out-of-band emissions, the need for effective filtering solutions is paramount. This work emphasizes the role of FIR filters in mitigating such impairments while maintaining system performance within the stringent requirements of 5G. Employing hardware description languages (HDLs), the FIR filter architecture is meticulously designed and simulated, allowing for an in-depth analysis of its performance under diverse operational scenarios. Innovations in filter coefficient generation and architectural optimization are explored, resulting in a design that not only achieves improved spectral efficiency but also optimizes resource utilization and processing speed. Rigorous testing and verification demonstrate the filter's effectiveness in enhancing signal quality, reducing noise, and supporting advanced features such as massive MIMO and beamforming. The findings underscore the feasibility of deploying hardware-efficient FIR filters in next-generation communication systems, thus contributing to the realization of high- performance 5G applications. Future research directions are suggested, aiming to investigate adaptive filtering techniques and the integration of emerging technologies to further elevate performance standards in dynamic wireless environments.***

Keywords: ***fifth-generation (5G) wireless communication technology, Finite Impulse Response (FIR), Orthogonal Frequency Division Multiplexing (OFDM), Inter-symbol interference (ISI).***

I. INTRODUCTIONS

The rapid evolution of wireless communication has led to the emergence of fifth-generation (5G) networks, which demand high data rates, low latency, and robust signal integrity. Among the various modulation techniques employed in 5G, Orthogonal Frequency Division Multiplexing (OFDM) has become a fundamental choice due to its high spectral efficiency and resilience to multipath fading. However, one of the key challenges in OFDM systems is managing inter-symbol interference (ISI) and out-of-band emissions, which can significantly degrade system performance. To address these issues, digital filters play a crucial role in shaping the signal spectrum and suppressing unwanted components. Finite Impulse Response (FIR) filters, in particular, are widely preferred in modern communication systems owing to their inherent stability, linear phase characteristics, and ease of implementation in hardware. The ability to precisely control the frequency response makes FIR filters especially suitable for filtering applications in OFDM-based systems.

This work focuses on the design and hardware implementation of an FIR filter optimized for 5G OFDM communication. The filter is intended to improve signal quality by reducing noise and interference while maintaining the integrity of the transmitted data. The implementation leverages hardware description languages (HDLs) to model the FIR filter architecture, with verification conducted through simulation and analysis of its performance under various input conditions. The goal is to develop a filter design that meets the stringent specifications of 5G systems while being efficient in terms of resource utilization and processing speed.

Despite its advantages, OFDM signals are prone to issues such as inter-symbol interference (ISI), inter-carrier interference (ICI), and spectral leakage, particularly in highly dynamic and noisy environments. These impairments can adversely affect the overall system performance if not properly mitigated. Filtering is therefore a critical component in the signal processing chain, especially for controlling out-of-band emissions and improving overall spectral confinement.

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As 5G systems operate in high-frequency bands with strict performance requirements, there is a growing need for efficient and optimized digital filter architectures that can be implemented on hardware platforms such as Field-Programmable Gate Arrays (FPGAs) or Application-Specific Integrated Circuits (ASICs). Designing an FIR filter that meets the performance constraints of 5G while minimizing resource utilization, latency, and power consumption is both a technical challenge and a practical necessity.

This thesis is motivated by the need to develop a reliable and hardware-efficient FIR filter tailored for 5G OFDM systems. The design process involves filter coefficient generation using MATLAB, followed by hardware description in Verilog HDL. Simulation and verification are carried out using industry-standard tools to evaluate the filter's performance in terms of accuracy, latency, and frequency response.

Application-Specific Integrated Circuit (ASIC) design for a FIR filter focuses on creating a tailored hardware block that delivers efficient arithmetic and logical computations. Unlike general-purpose implementations, an ASIC approach is optimized for specific performance goals, such as reduced power consumption, area efficiency, and higher speed. In the context of a FIR filter architecture, must support a limited but essential set of operations executed rapidly and reliably. As ASIC designs are meant for dedicated deployment, this implementation ensures the hardware is fine-tuned for real-world applications with minimal overhead. The ASIC flow begins with RTL design and simulation, typically using Verilog or VHDL, followed by synthesis using EDA tools like Cadence Genus. During synthesis, the design is mapped to a technology library, and various optimizations are applied to meet timing, power, and area targets. For a FIR filter, this step is crucial because it transforms the high-level logic into a silicon-realizable format.

A. Objectives of the Work

- To verify the functional correctness of the FIR filter architecture through simulation: Simulate the designed Verilog module to ensure accurate implementation of the filtering algorithm. This includes verifying proper behavior of the input shifting mechanism, coefficient multiplication, and accumulation logic under various input scenarios, including impulse and step responses.
- To evaluate the filter's time-domain performance using testbench stimuli: Apply known input sequences to observe and measure the output response characteristics such as latency, stability, and transient behavior. The goal is to validate the expected output waveform and confirm that the filter coefficients produce the intended response.
- To synthesize the FIR filter design using FPGA-targeted synthesis tools: Translate the behavioral Verilog description into a gate-level netlist optimized for FPGA implementation. Evaluate the resource utilization, such as slice registers, LUTs, and DSP blocks, and identify any timing violations or critical paths in the design.
- To analyze the timing and area efficiency of the FIR filter implementation: Assess the post-synthesis reports to ensure that the design meets the target timing constraints. Review the clock frequency, propagation delays, and maximum achievable throughput to confirm its suitability for real-time 5G communication applications.

II. METHODOLOGY OF THE WORK

The design and synthesis of an optimized FIR filter involves a structured approach comprising architectural planning, behavioural modeling, RTL implementation, functional simulation, and synthesis using industry-standard EDA tools. The methodology adopted for this project is outlined in the following key phases:

The initial phase involves identifying the functional requirements of the RISC-based FIR, including supported arithmetic and logical operations, operand width (typically 16-bit or 32- bit), and control signal interface. Based on these requirements, a modular architecture is defined, comprising operational blocks such as the adder/subtractor unit, logic unit, shift unit, and multiplexer-based control path.

1) RTL Design Using Verilog HDL: Each functional unit of the FIR is described using Verilog Hardware Description Language. The ALU control logic is implemented to decode operation select lines and generate control signals accordingly. The design adheres to synthesizable coding practices, ensuring compatibility with logic synthesis tools. Modules are designed hierarchically, allowing for improved readability and modular testing.

2) Functional Verification via Simulation: After RTL coding, each module is subjected to extensive simulation using testbenches written in Verilog. Behavioural simulations are performed to validate the correctness of the FIR filter under all possible input scenarios. The verification process includes checking the arithmetic overflow, zero flag, sign flag, and carry outputs, along with logic operation accuracy. Simulations are conducted using industry tools such as ModelSim or XSIM.

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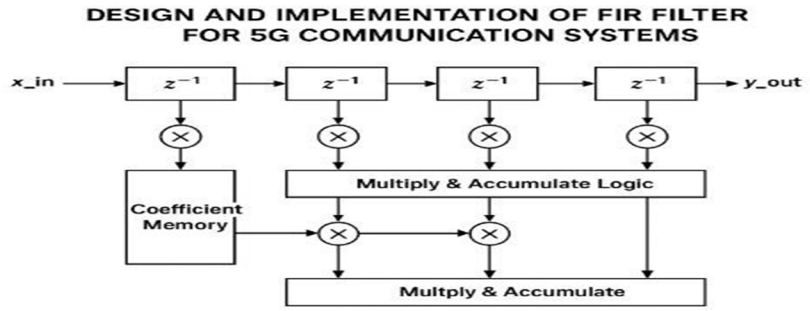
3) FIR filter design: The diagram represents a Finite Impulse Response (FIR) filter structure tailored for 5G communication systems, highlighting a typical tapped delay line architecture. The input signal x_in is passed through a series of delay elements, each represented by z−1z^{-1}z−1, which store previous input samples. These delayed signals are then multiplied by corresponding filter coefficients retrieved from the coefficient memory. The multiplication results reflect the contribution of each input sample to the overall filter output, which is critical in shaping the frequency response according to design specifications.



This study employs a systematic approach to design and evaluate low-power compressors, beginning with a critical review of existing architectures to identify optimization opportunities. Proposed designs are modeled at the gate and transistor levels, incorporating logic simplification, voltage scaling, and alternative logic styles to minimize power while preserving performance. Rigorous verification is conducted using industry-standard EDA tools, with power, delay, and area metrics benchmarked against conventional designs. The methodology further validates practical applicability by integrating optimized compressors into multiplier circuits, assessing their impact on real-world applications like AI acceleration and signal processing through standardized evaluation frameworks

III. FUNCTIONAL VERIFICATION OF FIR FILTER

Functional verification of low-power compressors involves rigorous testing to ensure correct arithmetic operations while meeting power efficiency targets. Testbenches are developed to apply exhaustive input combinations, including edge cases, to validate the compressor's behavior under typical and worst-case scenarios. Power-aware simulations track dynamic and leakage power consumption during operation, ensuring the design adheres to predefined energy budgets. Metrics such as error rate, propagation delay, and power-delay product are analyzed to verify compliance with both functional and low-power objectives. This step is critical to identify logic flaws or unintended power overheads before physical implementation.

To enhance verification coverage, advanced techniques like assertion-based checking and constrained random testing are employed. These methods systematically explore the compressor's response to diverse input patterns, including those specific to approximate computing applications where minor errors are permissible. Tools such as ModelSim or VCS correlate simulation results with RTL and gate-level models, while power analysis tools (e.g., PrimeTime) quantify energy savings. By cross-validating results against golden reference models, the verification process ensures the compressor maintains reliability in real-world deployments, such as AI accelerators or DSP units, where power efficiency and functional accuracy are equally critical. The main filtering logic is triggered on the positive edge of the clock or when a reset is asserted. On reset, the output and internal registers would typically be cleared (though that part isn't fully visible in the snippet). In regular operation, the filter shifts the new input into the `shift_reg` array, updating the internal state. The final output `y_out` is computed as a sum of products between the delayed inputs and their corresponding coefficients, implementing the FIR filtering operation. This approach is commonly used in DSP applications for noise reduction, signal smoothing, and other signal processing tasks in digital systems

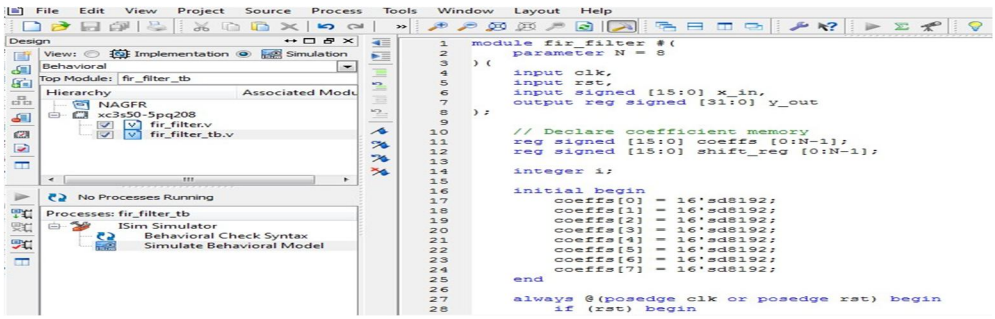


Figure 1: Verilog code Execution in Xilinx

1) RTL Schematic: The RTL schematic of the FIR filter showcases the internal structure of the design implemented in hardware. It consists of a sequence of flip-flops (labeled `fdc`) connected in series, which serve as delay elements forming the shift register. Each flip-flop holds a delayed version of the input signal `x_in`, which is critical for the tap structure of the FIR filter. The signal progresses from left to right, being delayed at each stage, allowing the filter to access past input samples simultaneously. This chain of flip-flops directly corresponds to the `shift_reg` array in the Verilog code.

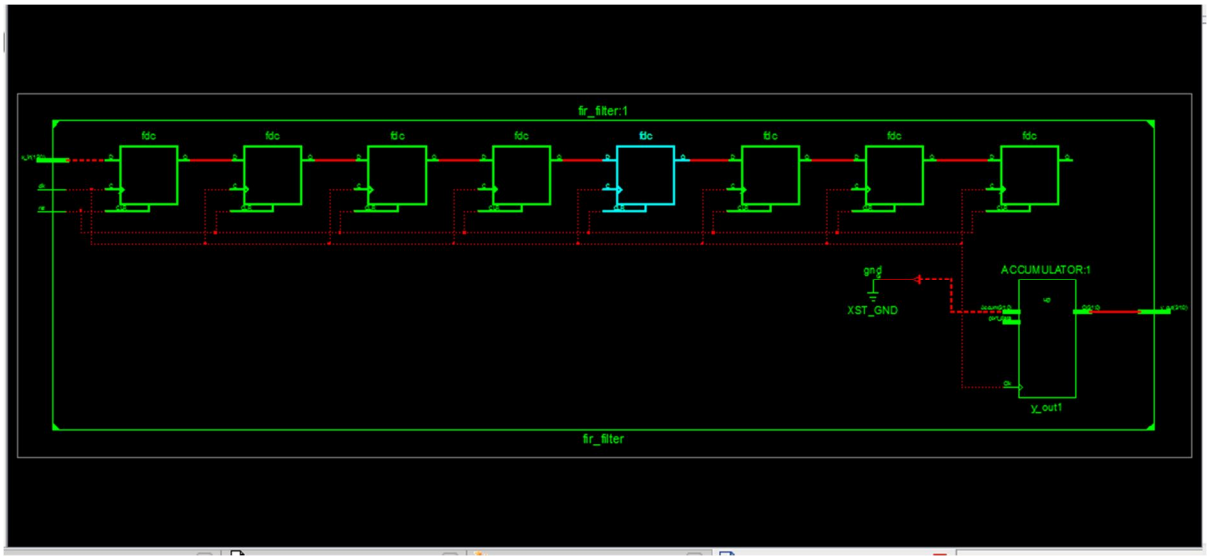


Figure 2: RTL Schematic

The RTL technology schematic of the FIR filter illustrates the gate-level implementation that is synthesized from the HDL description. This schematic shows a detailed network of logic gates and flip-flops that work together to execute the filtering operation. Each green symbol represents a logic element such as AND, OR, XOR, or flip-flops, while the red interconnects denote signal routing and data paths between these elements. The hierarchical structure highlights the underlying digital logic that realizes the arithmetic operations like multiplications and additions essential for computing the weighted sum of input samples.

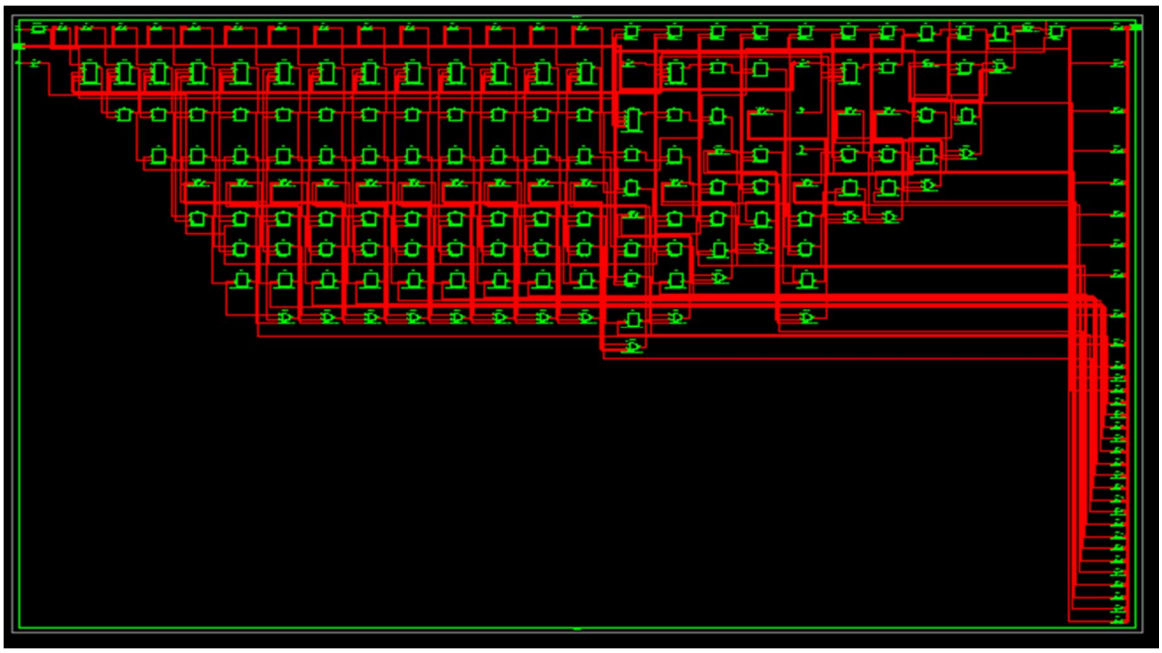


Figure 3: RTL technology Schematic

A. Simulation Results

The waveform shown represents the simulation result of a Finite Impulse Response (FIR) filter implemented in a digital system. In this simulation, the signals of interest include the input x_in[15:0], output y_out[31:0], clock (clk), and reset (rst). Initially, the reset signal is active low (0), holding the system in its initial state. During this time, the output remains at zero, indicating that the FIR filter is not processing any input data. At approximately 94 ns, the reset is deasserted (goes high), allowing the filter to begin operation. Shortly after, the output signal starts changing in response to the input signal.

Between 94 ns and 100 ns, the x_in input remains constant with a value of 0000000000000000, while the output y_out transitions from a sequence of zeros to a non- zero value followed by a pattern of ones (1111111111111111). This behavior demonstrates the FIR filter's response to a change in system state and indicates that it is producing an output based on past and present input samples, as per its designed coefficients. The simulation confirms the temporal behavior of the filter logic and validates the design's response to an input sequence under synchronous clock operation.

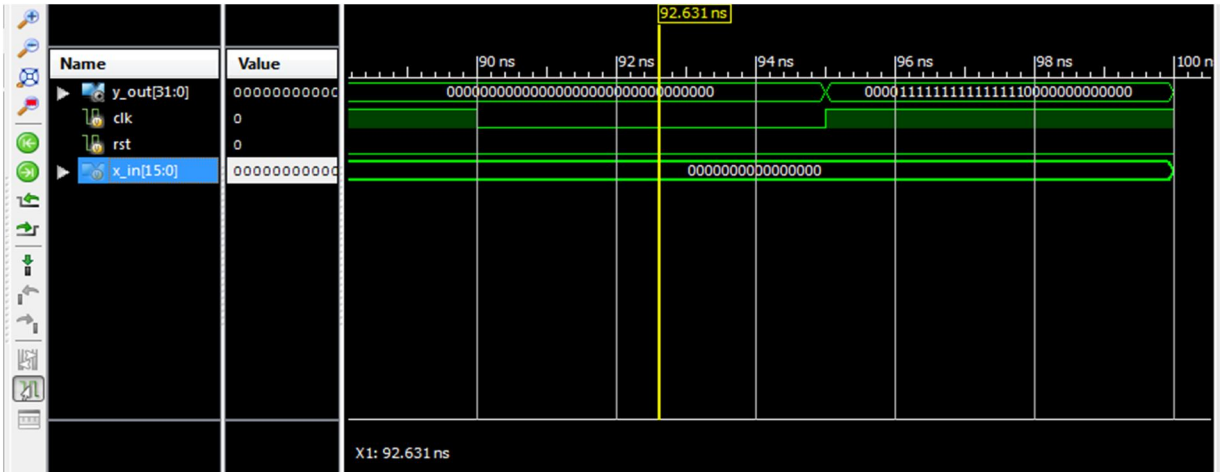


Figure 4: Functional verification of the results

The functional verification and implementation of a FIR filter design using in Verilog HDL. It emphasizes rigorous testing using simulation tools (e.g., ModelSim) to ensure functional correctness, low power consumption, and reliability for real-world applications. The synthesis enhances multiplication efficiency by reducing logic levels and power usage. The RTL schematic demonstrates a modular FIR architecture with separate filter components. Simulation waveforms confirm proper instruction decoding and operation execution across clock cycles, validating the design's functionality and synchronization.

IV. SYNTHESIS OF LOW POWER COMPRESSOR

The synthesis of FIR filter using the Cadence Genus tool involves optimizing the RTL design for reduced power consumption while maintaining functional accuracy and timing performance. Genus performs logic mapping, gate-level optimization, and technology-specific cell selection to minimize dynamic and static power. During synthesis, techniques such as clock gating, logic restructuring, and low-power cell insertion are employed to achieve energy-efficient operation. The tool also generates detailed power analysis reports, enabling designers to identify and eliminate power-hungry paths within the compressor structure.

Simulation following synthesis is essential to verify that the low-power optimizations do not affect the intended behavior of the design. Post-synthesis simulation uses the gate-level netlist generated by Genus and includes switching activity to reflect real power usage scenarios. The waveform outputs confirm that the compressed partial product generation logic remains intact, and the timing requirements are satisfied. This step ensures the compressor is not only functionally correct but also optimized for deployment in power- sensitive applications such as portable communication devices or battery-operated systems.

The synthesis procedure involves converting the RTL (Register Transfer Level) Verilog code into a gate-level netlist using a synthesis tool like Cadence Genus. The process begins by importing the RTL design and setting up the design constraints, including timing, area, and power requirements. The tool then analyzes the design, performs optimization, and maps the logic to technology-specific standard cells. During this step, techniques such as logic minimization, retiming, and resource sharing are applied to improve performance and reduce power consumption. Finally, the tool generates reports detailing timing, area, and power estimates, and outputs a gate-level netlist ready for further verification or physical implementation.

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In this layout, it can observe the orderly placement of logic blocks on the left and routing congestion toward the right where outputs are funneled. The synthesis process ensures that the design meets timing requirements by analyzing the critical paths and adjusting gate sizes or adding buffers accordingly. This synthesized design serves as the foundation for further stages such as placement and routing, followed by physical verification. The process ensures that the functional behavior of the original RTL is preserved while optimizing for real-world silicon implementation.

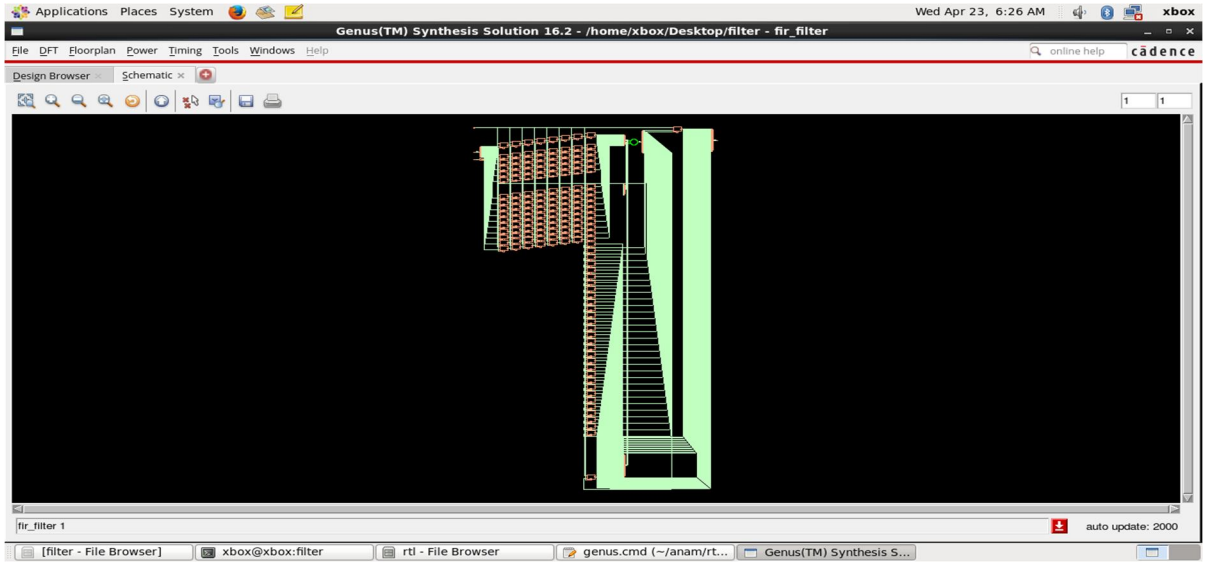

Figure 5: Synthesis

Power Report: The power report for the FIR filter, generated using Cadence Genus Synthesis Solution, outlines the power consumption metrics of the synthesized design under specified operating conditions. The report distinguishes between leakage, internal, net, and switching power components. The top-level module, labeled fir_filter, comprises 677 standard cells and exhibits a total switching power of approximately 32,603.225 nW, which reflects the dynamic power usage during signal transitions. Additionally, the internal power—arising from short-circuit currents and internal capacitances—is reported to be around 26,036.454 nW. These values are influenced by the underlying technology library (fast_vdd1v0 1.0) and the operating condition (PVT_1P1V_0C), which simulate typical voltage and temperature scenarios.

Also detailed in the report is a submodule or grouped instance, fir_filt...8_groupi, consisting of 516 cells. This sub-block consumes notably less power, with a switching power of 9241.425 nW and internal power at 6318.834 nW. The leakage power, which results from sub-threshold currents even when the circuit is idle, is measured at 78.494 nW for this group and 138.996 nW for the complete design. These figures are crucial for low-power design

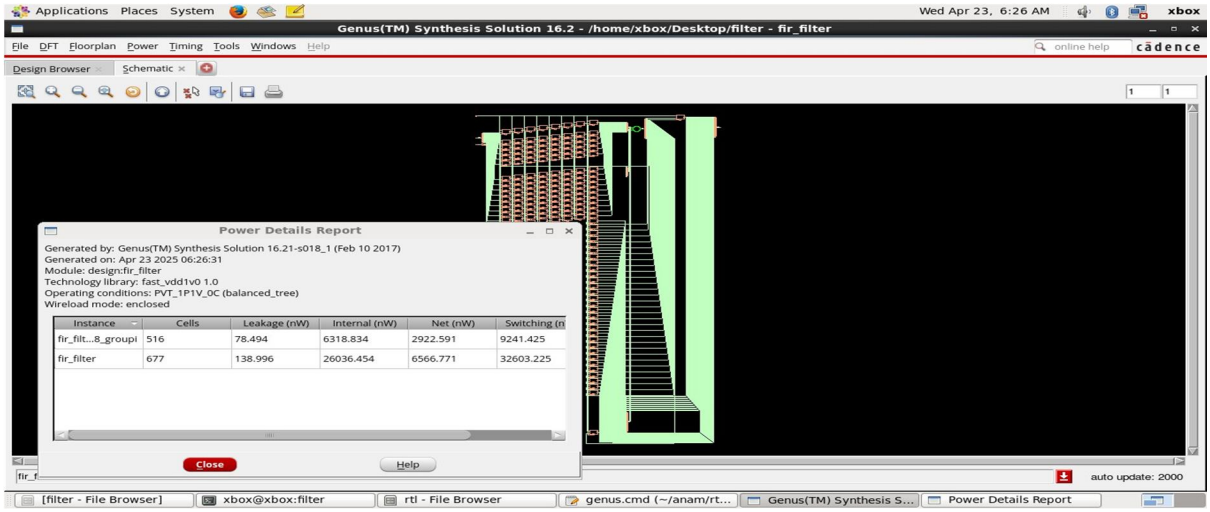

Figure 6: Power report

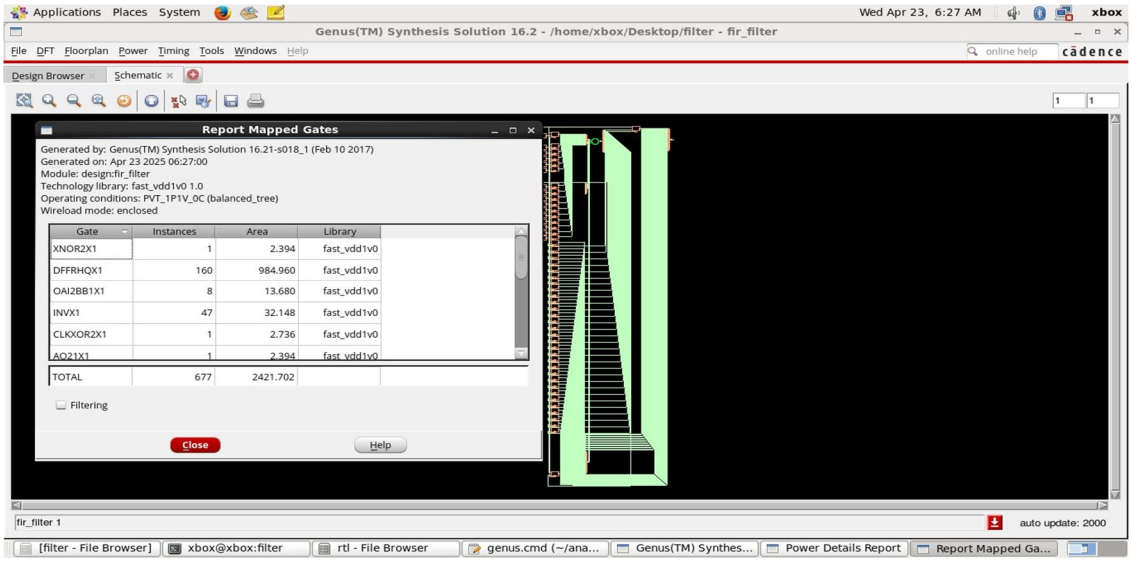

Figure 7: Area report

Discusses the synthesis of a low-power FIR filter using the Cadence Genus tool, emphasizing optimization for power, timing, and area. The process involves RTL-to-gate- level conversion using techniques like clock gating and logic restructuring to minimize power without affecting functionality. Post-synthesis simulations verify the accuracy of the gate- level netlist. The modular design—featuring separate control and datapath logic—supports hierarchical synthesis and efficient verification. Detailed reports from Genus provide insights into power usage, area consumption by standard cells, and timing paths, enabling thorough analysis and optimization for low-power embedded system applications.

V. CONCLUSIONS

The design and synthesis of a FIR filter design presented in this work highlight the critical role of optimization in enhancing performance, power efficiency, and area utilization in modern digital systems. By leveraging advanced EDA tools, particularly Cadence Genus, the project demonstrates a structured approach that encompasses architectural modeling, RTL implementation, and rigorous functional verification. The optimized Filter not only fulfills the fundamental functionality expected in FIR architectures but also ensures that it adheres to stringent timing and power constraints. This dual focus on functionality and optimization underlines the importance of integrating cutting-edge design methodologies in developing efficient computational units.

Furthermore, the work emphasizes the significance of adopting a modular and scalable approach in filter design, which aligns well with the principles of filter architecture. The findings illustrate that through careful design choices and synthesis techniques, it is possible to achieve a compact yet robust filter that performs efficiently across various operational scenarios. Future improvements may involve exploring adaptive optimization techniques and the integration of emerging technologies to further enhance performance and resource utilization in next-generation digital systems. The project sets a benchmark for subsequent research in filter design and offers insights that could assist in addressing the evolving demands of embedded and application-specific environments.

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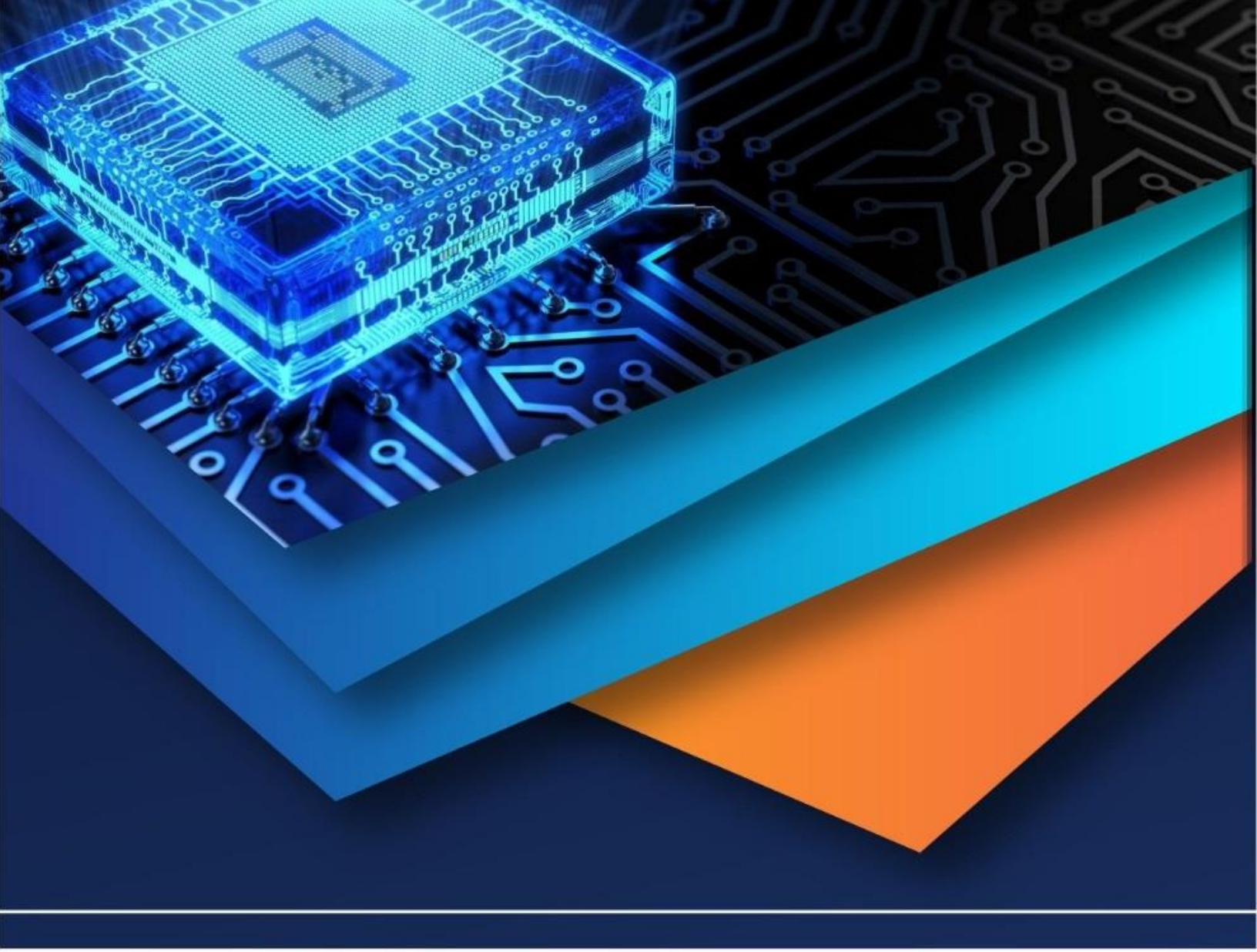

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