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Designand Implementation of Low Power 4:2 Compressor using GDI Technique

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Abstract: ***The objective is to develop a 4:2 compressor with GDI technique (Gate Diffusion Input). This is specifically aimed at reducing power consumption and digital circuit delays. The proposed GDI-based 4:2 compressor is compared to two existing designs: traditional CMOS design and 8T XOR-XNOR design. The results show that the GDI design saves 75.34% of the power consumptioncompared to traditional CMOS designs and 48.81% compared to the 8T XOR- XNOR designs. One of the main applications of this compressor is the design of multipliers, which is essentially important for efficient arithmetic operations in digital systems.The implementation of a GDI based 4:2 compressor in multiplier design improves the overall performance of the multiplier, achieving both faster calculations and lower energy consumption. When integrating the compressor with the 4x4 multiplier. The proposed design saves 51.24% of power supply compared to traditional CMOS design and 31.42% of power supply compared to 8T XOR-XNOR designs.***

Keywords: VLSI, Compressor,Array Multiplier,GDI technique,Power consumption,Delay.

I. INTRODUCTION

The design and implementation of low performance digital circuits is extremely important for modern VLSI (Very Large Scale Integration) systems, where energy efficiency is important, especially for portable and powerful applications. A key component of many arithmetic and signal processing processes is the 4:2 compressor. This is often used in digital systems such as multipliers, adders, and DSP systems (digital signal processing). The 4:2 compressor occupies four input bits and compresses it into two output bits and a support bit. This effectively reduces the number of bits to process. This is essential for optimizing the performance of complex systems. Traditional designs, such as those based on CMOS technology, often suffer from high power consumption and increased region due to the numerous transistors involved in implementing logic functions. In response to these challenges, this project focuses on designing and implementing low-performance 4:2 compressors using advanced techniques such as Gate Diffusion Input (GDI). GDI technology is a promising way to significantly reduce the number of transistors, reducing power consumption and faster switching speeds. This is especially important for high- performance VLSI applications where speed and performance efficiency are the most important. The proposed GDI-based 4:2 compressor is optimized for low power and high speed. This makes it an ideal design for use in multipliers, DSP systems, and other powerful arithmetic circles. By reducing the number of transistors, this design not only saves electricity, but also accelerates calculations and leads to general improvements in the performance of the system being implemented. This project examines design principles, implementation strategies, and performance evaluations for low performance 4:2 compressors, and presents the advantages over traditional designs in terms of power consumption, area and latency. The simulation is performed using the Cadence Virtuoso tool in 90nm CMOS technology to verify the effectiveness of the proposed design.

II. RELATED WORK

The related work of the GDI-based 4:2 compressor works to improve speed compared to traditional CMOS-based designs using the Gate Diffusion Input (GDI) technology. In this way, like with other compressors, four input bits are compressed with two start bits and one wear bit. However, the important difference is how logic gates are implemented. Instead of using multiple transistors for each logic gate, GDI technology uses fewer transistors to optimize the design. This is achieved by dividing the diffusion region into the entrance and output within the gate, leading to a more efficient circuit that requires less power to be switched. This reduces the total number of transistors and reduces power consumption. The logic gate is carefully designed to ensure the correct output and support bits of the two compression bits. This is used for higher order calculations such as repeated multiplications. Reducing transistor numbers not only saves power, but also enables faster switching speeds. In other words, GDI-based 4:2 compressors are ideal for high performance.

By optimizing performance and speed, GDI-based designs offer significant improvements compared to traditional CMOS compressors, making them suitable for modern VLSI systems where energy efficiency and performance are of paramount important.

III. METHODOLOGY

The methodology for designing and implementing the low-power 4:2 compressor using the GDI technique at 90nm technology in a 4×4 multiplier follows a structured approach. Initially, a thorough literature review is conducted to analyze existing compressor architectures and identify their limitations in terms of power consumption, speed, and transistor count. The design phase involves implementing the 4:2 compressor using the Gate Diffusion Input (GDI) technique, which enables a significant reduction in transistor count, power dissipation, and propagation delay compared to conventional CMOS logic. The designed compressor is then integrated into the partial product reduction stage of a 4×4 multiplier, ensuring minimal propagation delay and improved computational efficiency. Simulation and analysis are performed using Cadence Virtuoso EDA tool, where key performance metrics like power consumption, delay, and area are evaluated and compared against conventional designs. The working principle of the 4:2 compressor involves processing four input bits and a carry-in bit to generate sum and carry outputs, which are further used in subsequent stages of multiplication. The GDI technique enhances efficiency by reducing power dissipation through direct diffusion of inputs into transistors, which minimizes switching power. This approach results in a faster and more energy-efficient computation by reducing the logic depth and propagation delay. When integrated into the 4×4 multiplier, the compressor accelerates multiplication by optimizing partial product addition, making the circuit suitable for low-power VLSI applications such as digital signal processing (DSP) and embedded systems. The proposed methodology ensures an optimized balance of power, delay, and area, making it a viable solution for energy-efficient arithmetic processors.

IV. WORKING

CMOS based 4:2 compressor work involves absorption of four input bits and compression of two starting and carrying bits. This is useful for operations such as addition and multiplication, and should reduce the bit width of intermediate results. In CMOS design, the compressor is created using CMOS logic with AND, OR and XOR gates. Each of these gates is made up of transistors, which toggles two conditions (on or off) toggle logic operations on the inlet bits. Carry bits are used to take overflow into account in the additional process. The CMOS design ensures that the output is correct using a combination of PMOS and NMOS transistor. Slows the switching speed. This is because all transistors need to switch electricity, and the more transistors there are, the more electricity will use the circuit. Despite these disadvantages, CMOS designs are still used in digital systems due to their reliable and well- understood behavior.

V. RESULTS AND DISCUSSION

The circuit implementation of the 4:2 compressor using the GDI technique involves designing basic logic modules such as XOR, AND, and OR gates using GDI cells instead of conventional CMOS logic. GDI allows the realization of these gates with fewer transistors, significantly reducing power and delay. The circuits are simulated in 90nm technology using Cadence Virtuosa EDA tool and are compared in terms of power consumption and delay.

A. Cadence Simulation Output of 4:2 Compressor

Fig.1 shows the schematic of proposed GDI based 4:2 compressor. Fig.2 and Fig.3shows the simulation output waveforms of voltage and power respectively.

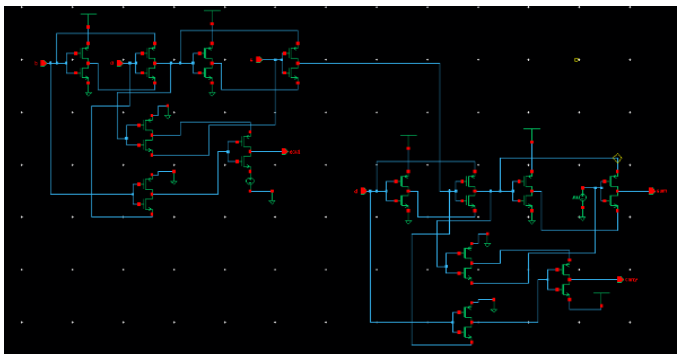

Fig.1.Schematic of GDI based 4:2 Compressor in Cadence Virtuoso

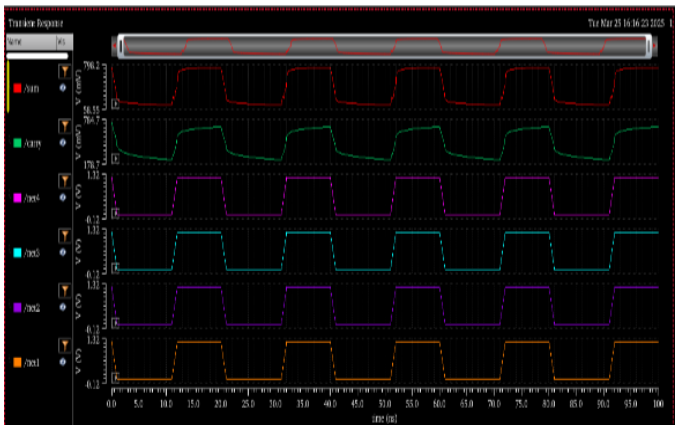

Fig.2.Voltage Waveform of GDI based 4:2 Compressor

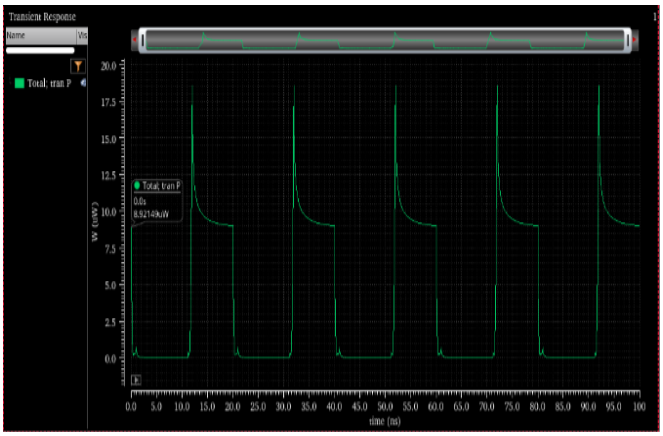

Fig.3.Power Waveform of GDI based 4:2 Compressor

The power consumption and delay values of the three 4:2 compressor designs are listed in Table I. It can be observed that the proposed GDI based compressor provides low power and high speed.

TABLEI
PERFORMANCE COMPARISON OF
COMPRESSOR DESIGNS

4:2 Compressor	Power Consumption (µw)	Delay (ps)	
		Sum	Carry
Conventional CMOS	36.19	635.2	604.4
8T XOR-XNOR	17.43	633.9	505.9
GDI based	8.92	598.2	357.4

B. 4X4 Array Multiplier Using 4:2 Compressor

A 4x4 multiplier is a digital circuit designed to multiply two 4-bit binary numbers, resulting in an 8-bit product. The design involves generating partial products (each bit of one multiplier is ANDed with each bit of the other) and then summing these partial products. A 4:2 compressor is a specialized circuit used in arithmetic operations, especially in multipliers. It takes four input bits plus an additional carry-in and compresses them into two outputs (a sum and a carry).

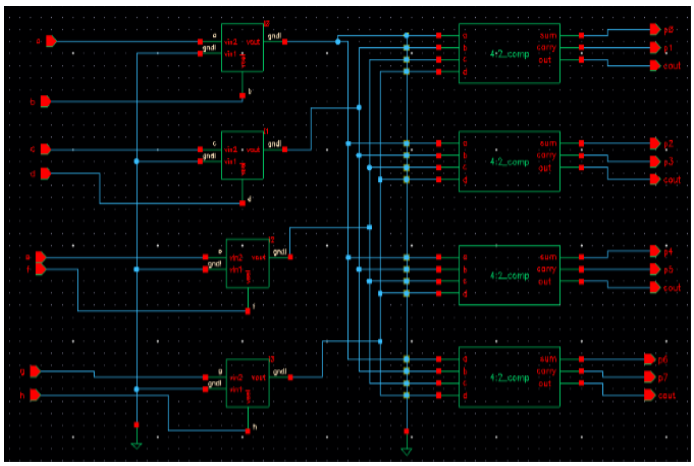

Fig.4.Schematic Diagram of 4x4 Multiplier using GDI based 4:2 Compressor

In this work, a 4x4 multiplier is designed using the three designs of 4:2 compressor and are compared in terms of power consumption. Fig.4.shows the schematic and Fig.5 shows the power waveform of 4x4 multiplier using GDI based 4:2 compressor. Table II lists the values of power consumption of the three multiplier designs.

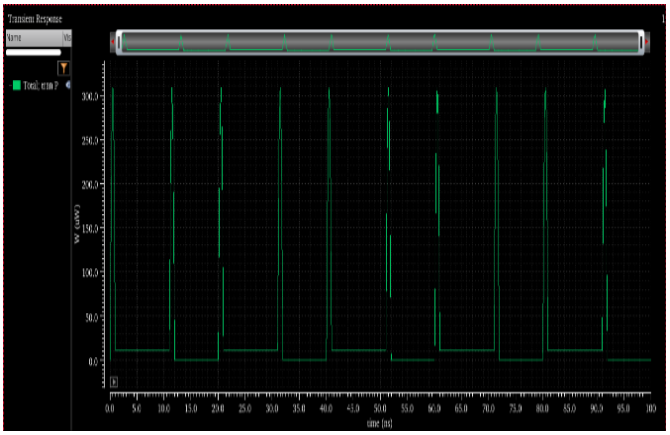

Fig.5 Power Waveform of 4x4 Multiplier using GDI based 4:2 Compressor

TABLEII
MULTIPLIER DESIGNCOMPARISON

4x4 multiplier with 4:2 compressor designs based on	Power Consumption (mW)
Conventional CMOS	3.5
8T XOR-XNOR	1.8
GDI based	1.1

VI. CONCLUSION

The 4:2 compressor designed using the GDI technique achieves low power consumption and minimal delay by reducing the number of transistors and logic complexity. This results in improved efficiency, making it ideal for high-performance and low-power VLSI applications, such as multipliers and DSP systems.This GDI based 4:2 compressor is compared with two existing designs. By comparing it with conventional CMOS design, it saves 75.34% of power and with 8T XOR-XNOR design, it saves 48.81% of power. This GDI design results in faster switching speed and reduced power consumption, making it ideal for high-performance and low-power VLSI applications, such as multipliers and DSP systems.

To appreciate the performance of the proposed GDI based compressor, a 4x4 array multiplier is implemented using the proposed compressor. This provides a saving of 51.24% of power consumption compared to conventional CMOS based multiplier and 31.42% of power consumption compared to the 8T XOR-XNOR module based multiplier.

VII.FUTURE WORK

Future enhancements in designing low-power 4:2 compressors using GDI (Gate Diffusion Input) techniques within 4x4 multipliers could focus on exploring novel architectures, optimizing GDI cell designs, and investigating approximate computing techniques for energy efficiency and performance..

VIII. ACKNOWLEDGEMENT

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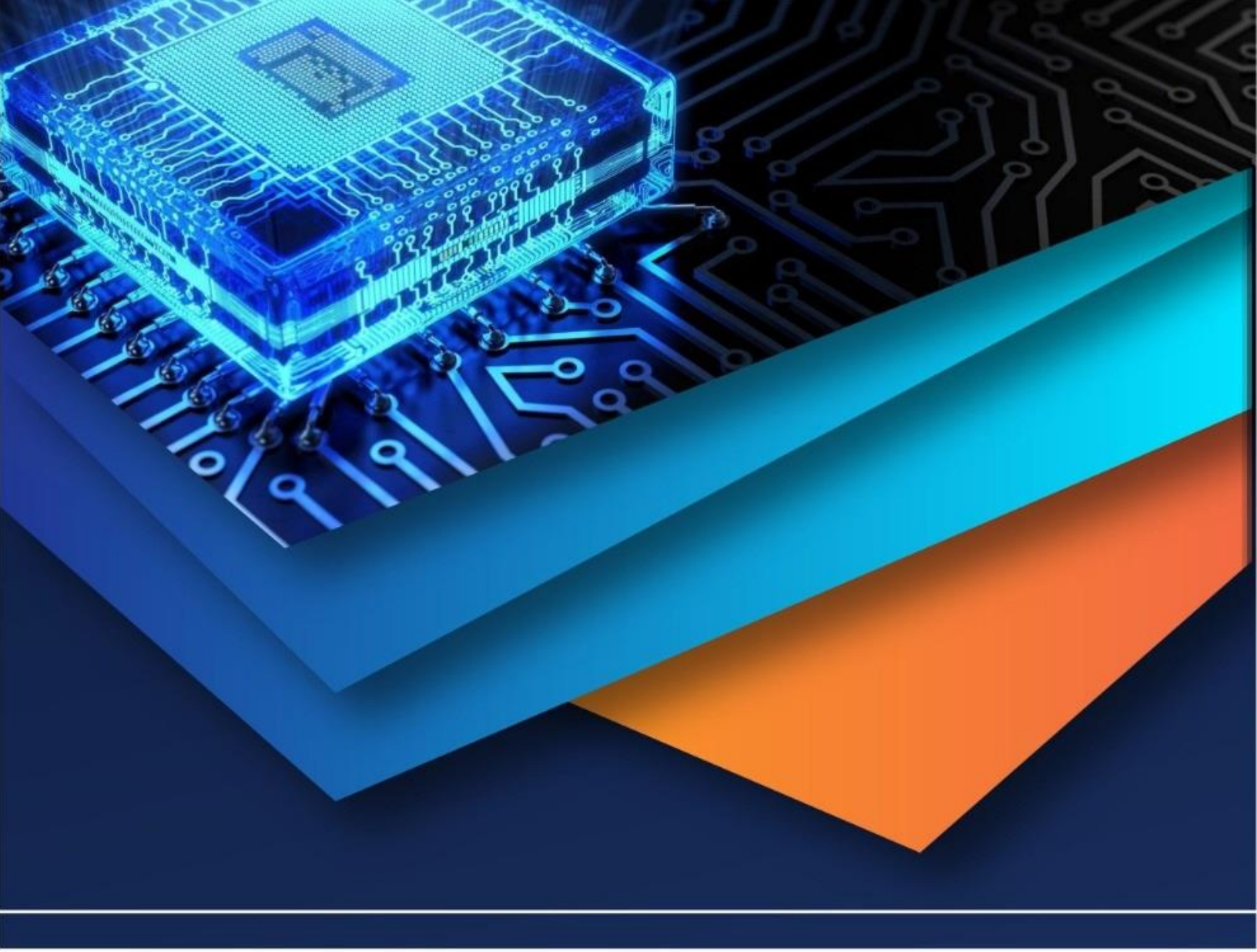
REFERENCES

[1] L. Hemanth Krishna, Ayesha Sk, J. Bhaskara Rao, Sreehari Veeramachaneni, and Noor Mahammad Sk,"Energy-Efficient Approximate Multiplier Design With Lesser Error Rate Using the Probability-Based Approximate 4:2 Compressor," IEEE embedded syst., vol. 16, no. 2,pp. Jun 2024.
[2] Antonio Giuseppe Maria Strollo, Ettore Napoli, Davide De Caro, Nicola Petra, and Gennaro Di Meo," Comparison and Extension of Approximate 4-2 Compressors for Low-Power Approximate Multipliers," IEEE Trans on circuits and syst., vol. 67, no. 9, Sep 2020.
[3] A. G. M. Strollo, E. Napoli, D. De Caro, N. Petra, and G. D. Meo, "Comparison and extension of approximate 4-2 compressors for low power approximate multipliers," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 9, pp., Sep. 2020.
[4] W. Guo and S. Li, "Fast binary counters and compressors generated by sorting network," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 29, no. 6, pp., Jun. 2021.
[5] T. Kong and S. Li, "Design and analysis of approximate 4–2 compressors for high-accuracy multipliers," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 29, no. 10, pp., Oct. 2021.
[6] Hema C, Shravani G, P Sivaphaneendra, Sinchana, Soundarya L," Implementation of Hardware and Energy Efficient Approximate Multiplier Architectures Using 4-2 Compressor for Images," IEEE Trans. Very Large Scale Integr. (VLSI) Syst.,vol11,April 2023.
[7] Pandiri Padma, Sanga Ramya, "Area Efficient Approximate Multiplier Using 4:2 compressor with Improved Accuracy" IEEE Trans. Very Large Scale Integr. (VLSI) Syst.,vol11,September 2023.
[8] Mingtao Zhang, Shinichi Nishizawa, Shinji Kimura," Area Efficient Approximate 4–2 Compressor and Probability-Based Error Adjustment for Approximate Multiplier," IEEE Trans on Circuits and Syst., vol. 70, May 2023.
[9] E.Rama Krishna Reddy, Bandaru Usha Sri , Reddy Syam Sundhar and Gudepu Kiran Mahesh Kumar,"Probability-based error adjustment and area-efficient approximate 4-2 compressor for approximate multiplier," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., March 2024.



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