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Design and Implementation of UART Using FPGA Board

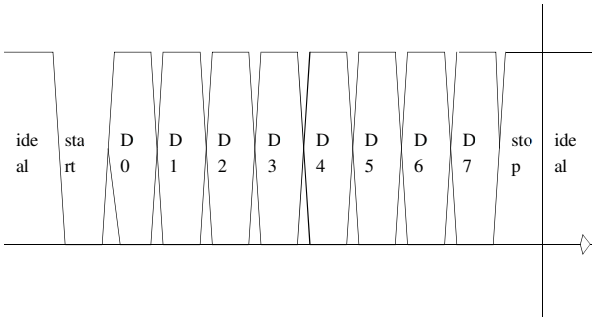
Anchal Govil[1], Anmol Karnwal[2], Govinda Sindhu[3], Ayush Singh[4], Dr. Shubham Shukla[5]
[1, 2, 3, 4]*KIET Group of Institution*
[5]*Guide- Sir (Assistant Professor)*

Abstract: ***This paper introduces the implementation of the Universal Asynchronous Receiver- Transmitter Controller (UART) based on Microprogrammed Controller on Field Programmable***
Gate Array (FPGA. Our UART design is fully functional and built-in. Coded using the Verilog design from top to bottom and visible in Spartan-3E FPGA using Xilinx ISE Webpack 14.7. Use results show that the design can work Spartan-3E FPGA maximum clock frequency of 218.248 MHz. The maximum frequent use of the UART controller is 192.773 MHz. of bits and hence this is why with a small amount of storage.
Keywords: Receiver, Transmitter, Microprogrammed Controller and Field Programmable Gate Array (FPGA).

I. INTRODUCTION

UART (Universal Asynchronous Receiver Transmitter) controller could be a serial communication device. In several control systems, serial communication circuit is employed largely .A universal asynchronous receive/transmit (UART) is an microcircuit which plays the foremost important role in serial communication. Serial communication is differently of communication used widely thanks to its simple structure and long transmission distance. Serial communication is significant to computers and allows them to speak with the low speed devices like keyboard, mouse, modems etc. UARTs are used for serial communication between two devices with minimum wires. the info is shipped serially, and no clock signal is distributed together with it. the first function of a UART is parallel-to-serial conversion when transmitting, and serial to-parallel conversion when receiving. The sender and receiver have separate, unsynchronized, clock signals. so as to synchronize the asynchronous serial data and to insure the information integrity, Start and Stop bits are added to the serial data. The transmitted character consists of an 8-bit data byte, sent LSB (least significant bit) first, preceded by a start bit (active low) and followed by a stop bit (active high). When no character is being transmitted, the road is idle (active high). the road needn't go idle between characters, because it is feasible for the beginning little {bit of} a transmission to right away follow the stop bit of the previous transmission. A field programmable gate array (FPGA) may be a logic device that contains a two dimensional array of generic logic cells and programmable switches. A logic cell will be configured (i.e., programmed) to perform an easy function, and a programmable switch is customized to supply interconnections among the logic cells. A custom design will be implemented by specifying the function of every logic cell and selectively setting the connection of every programmable switch. Once the planning and synthesis are completed, we are able to use a straightforward adaptor cable to download the specified logic cell and switch configuration to the FPGA device and procure the custom circuit.

Transmission Frame

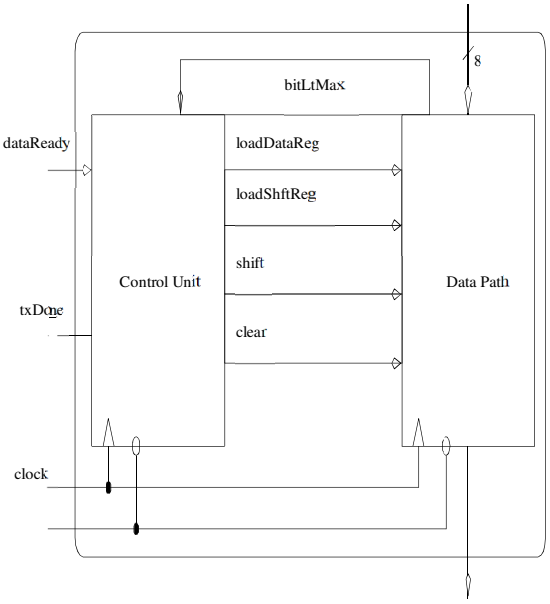


II. LITERATURE SURVEY

A. *UART Transmitter*

The proposed UART transmitter architecture comprises of two main building blocks which are data path unit and control unit, Figure 4. The architecture of the transmitter data path unit consists of **an information** register, **an information register**, and **a standing** register, which counts the bits that are transmitted. The figure shows the input- output signals of the transmitter. The input signals are provided by the host device, **and therefore the** output signals are the serial data stream and **a standing** signal. Data is transmitted serially on the serial Output put. The transmitter **is prepared** transmit when the status signal txDoneis asserted high. When data Readyis asserted high, the transmitter loads the content of the dataIn into data Register. bitCnt Max indicates the status of the bit counter **within the** datapath unit.

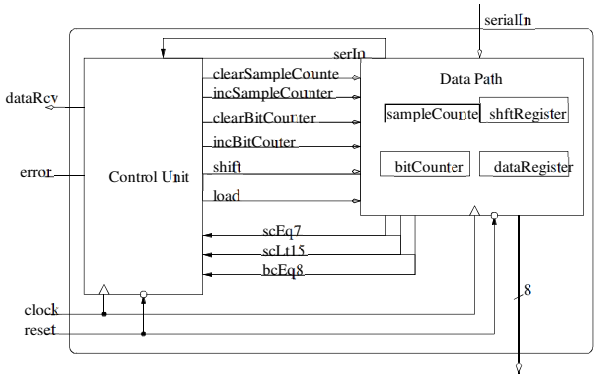
Functional Block Diagram of the Transmitter



B. *UART Receiver*

Figure 7 shows a functional diagram of the UART receiver. Data is received serially on the serialIn input. When one byte of knowledge has been received, it's output to the dataOut output bus, and therefore the output control signal dataRcvd is asserted high for one clock period. The block is clocked with a frequency 16 times the information measure.

Functional Block Diagram of the Receiver



C. UART Clock Generator

The UART Clock Generator in Figure is accustomed generate UART transmitter clock and receiver sample clock supported the subsequent calculation. the subsequent table shows the baud rate divisor and also the minimum number of bits that are required to store the baud divisor for sample clock.

Baud Rate	Baud Rate Divisor	# bits
9600	325.5208333	9
19200	162.7604167	8
38400	81.38020833	7
57600	54.25347222	6
115200	27.12673611	5
230400	13.56336806	4
460800	6.781684028	3
921600	3.390842014	2

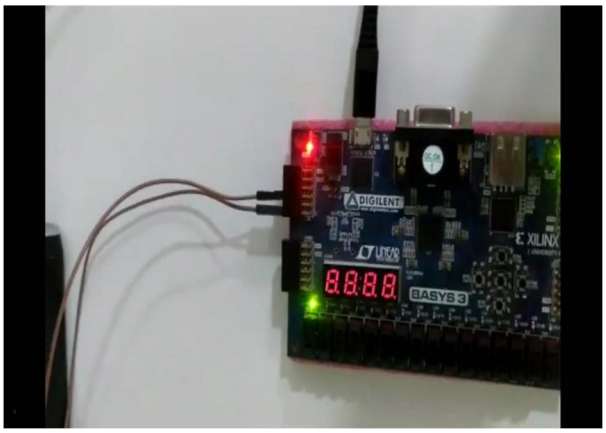
If, for example, the system clock = 50 MHZ and baud rate is 115200 bps, then the Baud Rate Divisor (BRD) for Sample clock is 27.12673611. If the scaling factor is 2^5, then the fixed-point representation of BDR

$= 27.12673611 * 2^5 \approx 868$. Therefore, the generated baud rate divisor = $868/2^5 = 27.15625$.

The generated baud rate =
50MHA/27.15625)/16 = 115075. Hence, the error is
$\frac{115075 - 115200}{115200} * 100 =$ 0.1085%.

III. RESULTS AND EVALUATION

The design of UART is coded using Verilog based top-down hierarchical design methodology and realized in Spartan-3E FPGA using Xilinx ISE Webpack 14.7. Table shows the FPGA utilization for the Microprogrammed implementation of the UART controller compared to the Hardwired implementation. Both implementations use almost the same amount of FPGA resources. However, Microprogrammed implementation operates faster: the minimum clock period of the Microprogrammed implementation is 4.582ns (Maximum Frequency is 218.248MHz) and is 5.187ns (Maximum Frequency is 192.773MHz) for Hardwired implementation. To prove the functionality of our design of UART, we implemented our design in Digilent Basys2 Spartan3E FPGA Board [5]. We then connect the FPGA board to a PC that runs a program that transmits and receives large-size (50 MB to 100 MB) of plain text and binary files. The program then compares the sent bytes to the received bytes. All the bytes that are sent are received correctly.



Comparison of Different Implementations of UART Controller

Method	ROM Size of the transmitter Controller	
	Size	No. of bits
ROM method with original SM chart	16×6	96
Microprogram med implementations	4×8	32
Method	ROM Size of the receiver Controller	
	Size	No. of bits
ROM method with original SM chart	128×10	1280
Microprogrammed implementations	7×13	91

IV. CONCLUSION AND FUTURE WORKS

In this paper, we have presented FPGA realization of micro programmed implementation of UART controllers. Our design is fully functional and synthesizable and can operate at a maximum clock frequency of 218.248 MHz. The design uses less number of FPGA resources compared to the ROMbased method. In this paper, we have presented FPGA realization of micro programmed implementation of UART controllers. Our design is fully functional and synthesizable on both receiver and transmitting side. We learnt about various new concepts.

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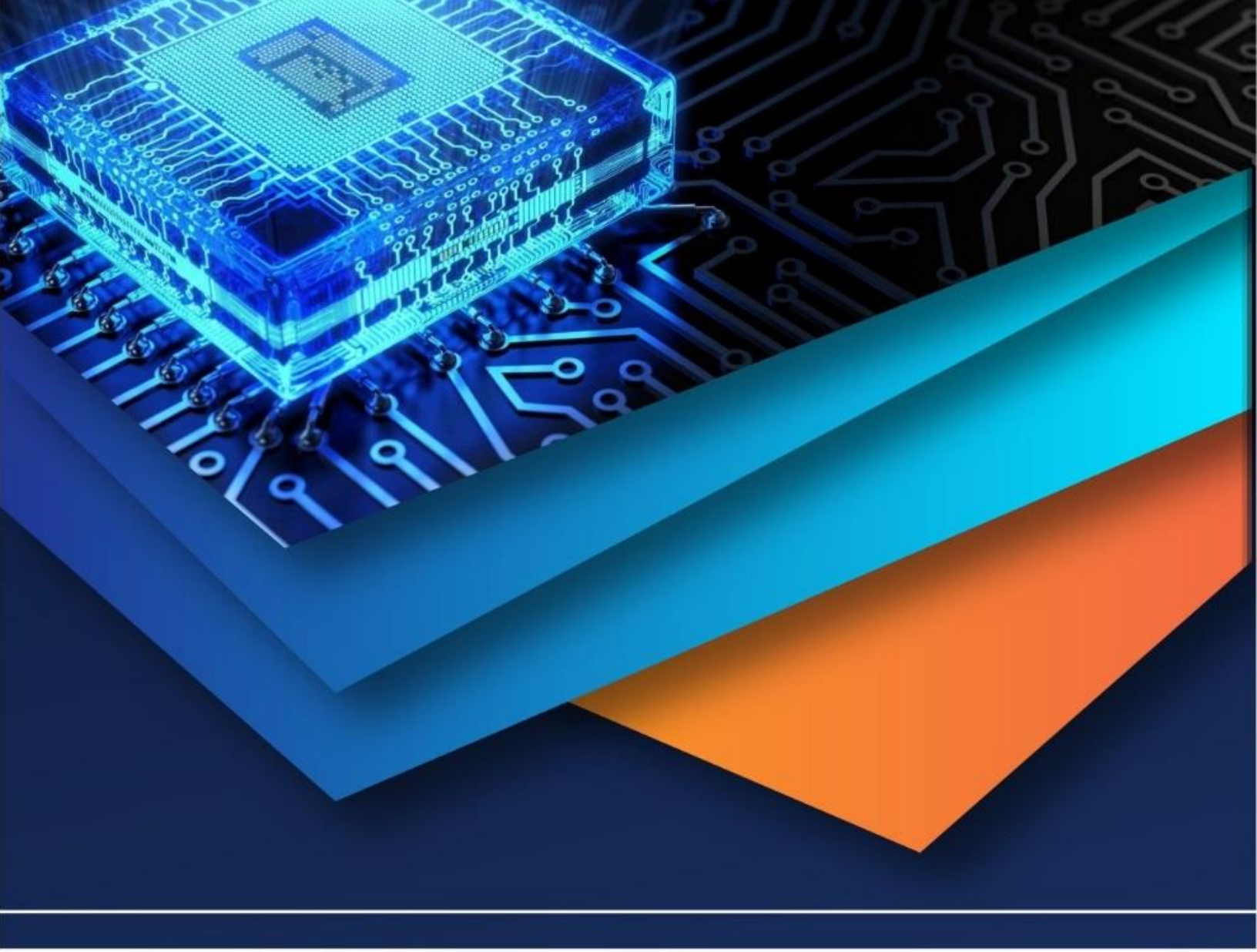

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