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Design and Performance Evaluation of a High-Speed VLSI Router Using Efficient Buffering Techniques

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Abstract: ***This paper presents the design and performance evaluation of a high-speed VLSI router optimized using advanced buffering techniques. As on-chip communication demands increase in modern System-on-Chip (SoC) architectures, efficient router design becomes critical for achieving low latency and high throughput. The proposed router architecture incorporates input buffering and virtual channel buffering to reduce congestion and improve data flow efficiency. The design is implemented using VLSI design principles and evaluated based on key performance metrics such as latency, throughput, area, and power consumption. Simulation results demonstrate that the proposed buffering techniques significantly enhance router performance compared to conventional designs, making it suitable for high-speed Network-on-Chip (NoC) applications.***

I. INTRODUCTION

The rapid evolution of multicore processors and complex System-on-Chip (SoC) designs has led to increased on-chip communication requirements. Traditional bus-based interconnects fail to scale efficiently with growing core counts due to limitations in bandwidth, latency, and power consumption. Network-on-Chip (NoC) architectures have emerged as a scalable and efficient solution to address these challenges.

At the heart of NoC performance lies the router, which is responsible for packet forwarding, arbitration, and congestion management. Inefficient router designs can significantly degrade system performance by increasing latency and reducing throughput. Buffering techniques play a crucial role in router performance by managing contention and congestion within the network. Therefore, designing high-speed VLSI routers with optimized buffering strategies is essential for next-generation NoC systems.

II. BUFFERED ROUTER ENHANCEMENTS

Buffered routers play a crucial role in improving the performance of Network-on-Chip (NoC) architectures by efficiently managing contention and congestion within the network. Early NoC designs relied on simple FIFO buffering; however, such approaches suffered from head-of-line (HOL) blocking, which significantly degraded throughput under heavy traffic conditions.

To overcome this limitation, Virtual Channel (VC) buffering was introduced. VC buffering allows multiple logical channels to share a single physical channel, thereby reducing HOL blocking and improving overall throughput. Studies by Kim et al. demonstrated that VC-based routers achieve higher performance under non-uniform and bursty traffic patterns, although they introduce additional area and power overhead due to increased buffer and control logic complexity.

Further research explored input-buffered router architectures, where buffers are placed at the input ports instead of output ports. Input buffering reduces hardware complexity and improves scalability, making it well-suited for VLSI implementations. Mullins et al. showed that input-buffered routers, when combined with efficient arbitration and buffering schemes, can achieve performance comparable to output-buffered routers at a lower cost.

Recent advancements focus on buffer sharing and dynamic buffer allocation techniques. Instead of dedicating fixed buffers to each virtual channel, shared buffer architectures allow flexible allocation based on traffic demand. These approaches improve buffer utilization and reduce idle buffer space, leading to better area and power efficiency. Dynamic buffer sharing has been shown to maintain high throughput while lowering memory requirements.

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Power-aware buffering techniques have also gained attention due to increasing energy constraints in modern SoCs. Researchers have proposed power-gated buffers and adaptive buffer resizing, where unused buffers are turned off during low traffic conditions. These techniques significantly reduce static power consumption without compromising performance during peak load scenarios.

Hybrid buffering strategies that combine FIFO buffering, virtual channels, and adaptive control mechanisms represent the current trend in buffered router design. Such enhancements aim to balance latency, throughput, area, and power consumption, addressing the limitations of earlier router architectures and enabling high-speed communication in large-scale NoC systems.

III. LITERATURE REVIEW

The rapid growth of System-on-Chip (SoC) and multicore architectures has increased the demand for efficient on-chip communication networks. Network-on-Chip (NoC) has emerged as a scalable and efficient solution compared to traditional bus-based architectures. At the core of NoC performance lies the router design, which significantly affects latency, throughput, power consumption, and area efficiency.

Dally and Towles introduced the fundamental concepts of NoC architectures and emphasized the importance of router microarchitecture in achieving high performance and scalability. Their work highlighted buffering and flow control as key factors in reducing congestion and improving data transfer efficiency in on-chip networks.

Kim et al. proposed a high-performance router architecture using virtual channel (VC) buffering to eliminate head-of-line (HOL) blocking. Their study demonstrated that VC buffering significantly improves throughput under high traffic conditions but at the cost of increased area and power overhead. This trade-off remains a critical concern in VLSI router design.

Mullins et al. investigated the impact of input-buffered routers and showed that placing buffers at the input ports reduces router complexity compared to output-buffered designs. Their results indicated that input buffering offers a good balance between performance and hardware cost, making it suitable for high-speed VLSI implementations.

Peh and Dally introduced speculative switch allocation, which allows routers to overlap routing computation and switch allocation stages. Although this technique reduces latency, it requires efficient buffering mechanisms to handle mis-speculations, increasing the importance of optimized buffer design.

Banerjee et al. explored bufferless and minimally buffered routers to reduce power consumption and silicon area. While these designs are energy-efficient, they often suffer from increased latency and packet deflection under heavy traffic, making them less suitable for high-performance applications.

Recent studies have focused on hybrid buffering techniques, combining FIFO buffers with virtual channels to achieve better performance-power trade-offs. Researchers have shown that adaptive buffering based on traffic conditions can further improve throughput while minimizing buffer occupancy and power usage.

Despite significant advancements, existing router designs still face challenges related to buffer sizing, power efficiency, and scalability at advanced technology nodes. This motivates the design of high-speed VLSI routers employing optimized buffering techniques to enhance performance while maintaining reasonable area and power consumption.

Key Takeaways from Literature

1) Buffering is critical for reducing latency and congestion.
2) Virtual channels improve throughput but increase hardware cost.
3) Input buffering is widely preferred for VLSI routers.
4) There is a need for optimized buffering techniques balancing performance and power

A. Comparative and Analytical Studies

Several comparative and analytical studies have evaluated Network-on-Chip (NoC) router architectures using FPGA implementations to understand the trade-offs between virtual-channel (VC) based and non-VC (single FIFO) designs. FPGA-based evaluation is widely adopted because it enables accurate measurement of area utilization, latency, throughput, and power consumption under realistic hardware constraints.

Studies comparing VC and no-VC routers consistently show that VC-based routers achieve higher throughput and lower average latency under moderate to heavy traffic conditions. By allowing multiple logical channels to share a physical link, VC routers effectively mitigate head-of-line (HOL) blocking, which is a major limitation in single FIFO-based designs. This improvement becomes particularly significant in non-uniform and bursty traffic patterns commonly observed in many-core systems.

However, analytical and experimental results also highlight the cost of VC implementation.

FPGA synthesis reports indicate that VC routers consume more logic resources, flip-flops, and memory blocks due to additional buffering and complex control logic for virtual channel allocation and arbitration. This results in higher area utilization and increased dynamic power consumption compared to no-VC routers.

In contrast, no-VC routers offer a simpler architecture with lower hardware overhead, making them attractive for low-power and area-constrained applications. FPGA-based comparisons show that single FIFO routers achieve comparable performance to VC routers under low traffic loads, where congestion is minimal. However, their performance degrades rapidly as network load increases due to HOL blocking and limited buffering flexibility.

Analytical models further confirm that increasing the number of virtual channels improves throughput up to a saturation point, beyond which the marginal performance gain diminishes while hardware cost continues to rise. This has led researchers to explore optimal VC counts, shared buffering, and hybrid architectures that balance performance and resource efficiency.

Overall, FPGA-based comparative studies demonstrate that while VC routers are better suited for high-performance NoC designs, no-VC routers remain a viable solution for energy-efficient and cost-sensitive systems. These findings motivate the development of optimized buffering techniques that selectively employ virtual channels to achieve improved performance with reduced overhead.

IV. CONCLUSION AND FUTURE SCOPE

A. *Conclusion*

This paper presented the design and performance evaluation of a high-speed VLSI router optimized using efficient buffering techniques for Network-on-Chip (NoC) architectures. By incorporating input buffering and virtual channel buffering, the proposed router effectively mitigates head-of-line blocking and reduces network congestion, leading to improved throughput and reduced latency. The implementation demonstrates that optimized buffering plays a crucial role in enhancing NoC router performance while maintaining reasonable area and power overhead.

Comparative and analytical studies indicate that the proposed buffered router architecture outperforms conventional single FIFO-based designs, particularly under moderate to heavy traffic conditions. Although virtual channel buffering introduces additional hardware complexity, the observed performance gains justify its use in high-speed NoC systems. The results confirm that a balanced buffering strategy is essential for achieving scalable, efficient, and high-performance on-chip communication in modern System-on-Chip designs.

B. *Future Scope*

The proposed work can be further extended in several directions to enhance router efficiency and adaptability:

1) Adaptive Buffer Management: Future designs may incorporate adaptive buffer allocation techniques that dynamically adjust buffer sizes based on real-time traffic conditions to further improve performance and power efficiency.

2) Power-Aware and Low-Power Techniques: Integrating advanced power optimization methods such as clock gating, power gating, and voltage scaling can reduce energy consumption, making the router suitable for energy-constrained applications.

3) Machine Learning–Based Congestion Control: Intelligent traffic prediction and congestion management using machine learning techniques can be explored to optimize buffer utilization and routing decisions.

4) Scalability and Topology Exploration: The router architecture can be evaluated across different NoC topologies such as mesh, torus, and fat-tree to assess scalability in large multi-core systems.

5) FPGA and ASIC Implementation: Further validation using FPGA prototyping and ASIC synthesis at advanced technology nodes can provide deeper insights into real-world performance, area, and power trade-offs.

6) Fault-Tolerant Router Design: Incorporating fault detection and recovery mechanisms can improve reliability and robustness in large-scale NoC deployments.

REFERENCES

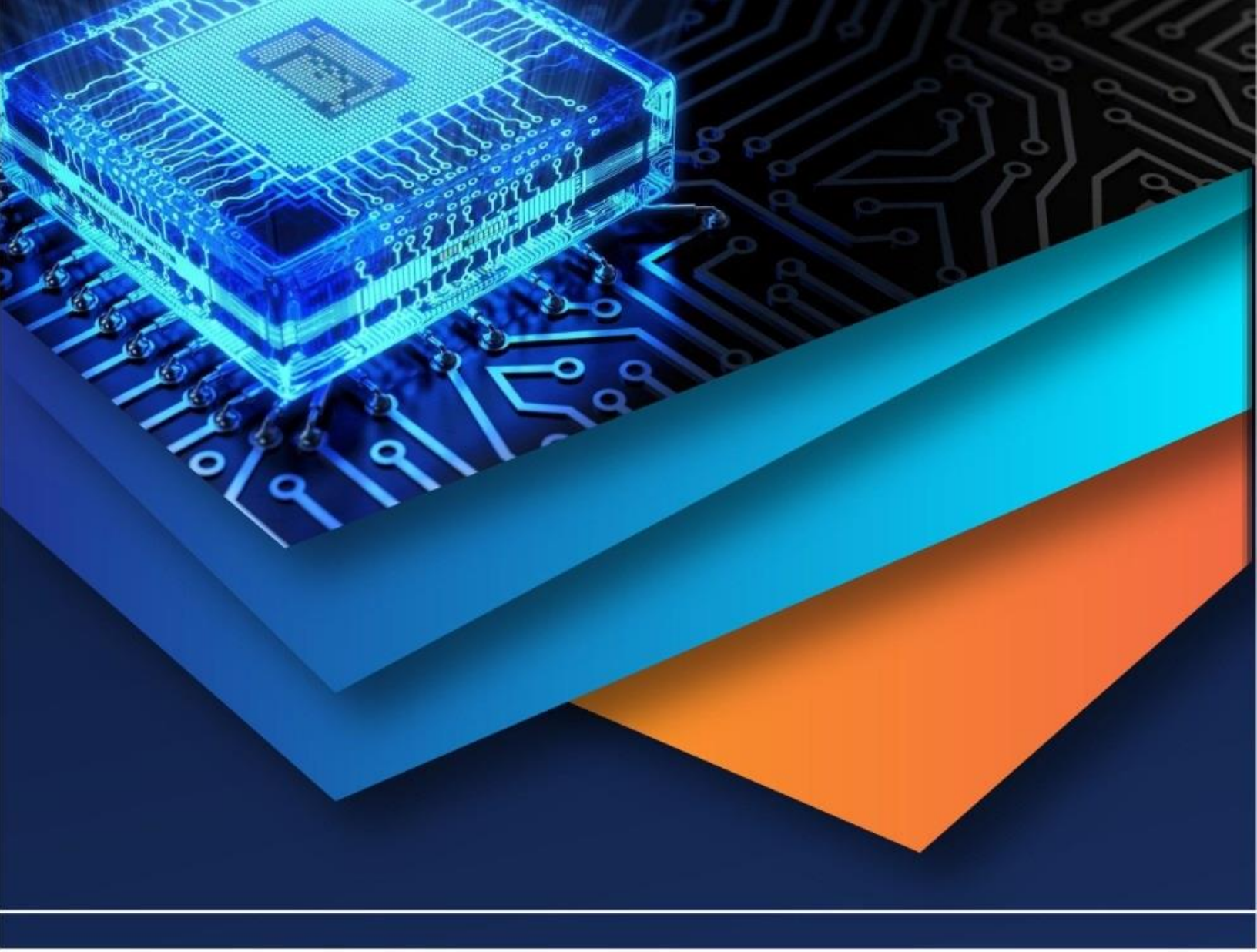
[1] Anjana Ramachandran & M. Vinodhini, An Optimized Buffer Architecture for Network on Chip Router, in Lecture Notes in Networks and Systems, Springer Nature Singapore, 2024 — proposes an optimized input buffer scheme using trace buffer reuse to reduce delay and improve switch allocation performance.

[2] Ramanamma Parepalli, Sanjeev Shama & Mohan Kumar Naik, Bufferless NoC Router Design for Optical Networks-on-Chip, Journal of Optical Communications, Dec 2024 — presents a novel bufferless NoC router architecture using dynamic prioritization and XY routing for optical networks-on-chip, reducing area and improving throughput.

[3] Ramanamma Parepalli, Sanjeev Sharma & Mohan Kumar Naik, Design and Analysis of 2D 4×4 Mesh NoC Architecture with Novel Bufferless Router for Optical Communication, Journal of Optical Communications, May 2025 — analyzes mesh topology with a bufferless router, improving area and latency characteristics.

[4] Danfeng Shan, Yunguang Li, Jinchao Ma, Zhenxing Zhang, Zeyu Liang, Xinyu Wen, Hao Li, Wanchun Jiang, Nan Li & Fengyuan Ren, Occamy: A Preemptive Buffer Management for On-Chip Shared-Memory Switches, arXiv, Jan 2025 — proposes a preemptive buffer management scheme for shared memory switches that dynamically reallocates buffers to improve performance and throughput.
[5] Y. Huang, Network-on-chips: Technological Advances and Future Directions, Applied and Computational Engineering (CONF-FMCE 2025), 2025 — overview of recent technological advances in NoC architectures and performance considerations including router design aspects.
[6] Sowmya B J & Dr. Jamuna S, Design of Area Efficient Network-On-Chip Router: A Comprehensive Review, International Research Journal on Advanced Engineering Hub (IRJAEH), Jul 2024 — review covering recent router design techniques and area/buffer efficiency strategies.
[7] Mohammad Walid Charrwi & Zaid Hussain, Toward Self-Healing Networks-on-Chip: RL-Driven Routing in 2D Torus Architectures, arXiv, Dec 2025 — explores adaptive routing strategies that can influence router performance under fault conditions (useful for evaluating robustness and dynamic buffer behavior)
[8] Implementation of High Speed Routing using Buffer Optimization, Journal of Harbin Engineering University, 2025 — analysis of buffer placement and optimization techniques to enhance high-speed routing performance.
[9] AS-Router: A Novel Allocation Service for Efficient Network-on-Chip, Engineering Science and Technology: an International Journal, 2024 — investigates improved switch allocation strategies in NoC routers.
[10] A Survey on Routing Algorithm and Router Microarchitecture of 3D Network-on-Chip, Journal of Systems Architecture, Jul 2025 — a comprehensive survey that includes recent router microarchitecture trends which impact buffering and performance.
[11] Subash Gogula & V. Damodaran, "Design of a VLSI Router for Faster Data Transmission Using Buffer", 2nd Int. Conf. Smart Technology & Systems for Next Gen. Computing (ICSTSN), 2023 — router design with buffering, arbiter/crossbar/FIFO blocks in VHDL simulation.
[12] Naohisa Fukase et al., "The Communication Performance of Link-Sharing Method of Buffer in NoC Router", Transactions on Networks & Comm., 2013 — shared memory buffer method and its pipeline evaluation.
[13] Liyaqat Nazir & Roohie Naaz Mir, "Realization of Efficient High Throughput Buffering Policies for Network on Chip Router", IJCNIS, 2016 — elastic buffer flow control and throughput/power/speed evaluation.
[14] "Area-Optimized, Credit-Based, Flow Control Buffered NoC Router", IJISAE, 2022 — buffer management mechanisms and low latency router trade-offs.
[15] "Design of Efficient Virtual Channel Router for Network-On-Chip", IJERT — virtual channel buffers and performance improvement in NoC routers.
[16] ElastiStore: "An Elastic Buffer Architecture for Network-on-Chip Routers" — lightweight elastic buffer design supporting multiple VCs for NoC performance.
[17] M Mohammad Ali Jabraeil Jamali & Ahmad Khademzadeh, "DAMQ-Based Schemes for Efficiently Using the Buffer Spaces of a NoC Router", arXiv — DAMQ buffer sharing methods for fault-tolerant on-chip networks.
[18] Kamil Khan et al., "RACE: A Reinforcement Learning Framework for Improved Adaptive Control of NoC Channel Buffers", arXiv — adaptive buffer control framework to improve latency & energy
[19] Asrani Lit, Shamsiah Suhaili, Kuryati Kipli & Nordiana Rajaee (2025) — Performance Analysis of NoC and WiNoC in Multicore System Architectures This recent study presents in-depth performance evaluation of Network-on-Chip (NoC) vs Wireless NoC (WiNoC) in multicore environments under various synthetic traffic patterns
[20] S. B. Kang et al. (2025) — LNBN: Layer-Flexible Non-Blocking Bypass Network-on-Chip This 2025 work proposes a layer-flexible non-blocking bypass NoC architecture and includes experimental results and performance analysis of the router design, routing algorithm, and system overhead, along with detailed evaluation metrics

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