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Design and Simulation of 16 Bit ADC

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Abstract: ***In this study, it was looked into how a 16-bit architecture might be used to develop an Analog-to-Digital Converter (ADC) Successive Approximation Register (SAR). The SAR ADC architecture is widely adopted for high-resolution applications because to its ease of use and minimal power requirements. The design also includes a voltage reference, a comparator, a successive approximation register, a sample-and-hold circuit, an analog-to-digital converter (DAC), and other components. A range of design approaches and circuit topologies are employed to maximize performance and satisfy the required criteria. The comparator is intended to properly detect the analogue input voltage and operate at high speeds. A binary search technique is used by the successive approximation register to find the input voltage's digital representation. The design is implemented using 250nm Gate Diffusion Input [GDI] Technology. Simulation and verification are performed using Tanner EDA tool. The results indicate that the proposed 16-bit SAR ADC achieves the desired resolution and meets the specified performance requirements. The ADC exhibits low power consumption, and satisfactory performance. This architecture its applications span across multiple disciplines, encompassing communication systems, scientific instrumentation, and medical imaging, where there is a requirement for accurate ADC conversion.***

Keywords: SAR ADC, ADC, power consumption, D-flip flop.

I. INTRODUCTION

ADC's plays a crucial role in transforming continuous analog signals into discrete digital representations essential components of contemporary electronic systems. With the increasing demand for higher resolution and accuracy in signal processing High-resolution ADC design has grown to be a key field of study and development for several applications.

The SAR ADC architecture was selected because it can provide excellent resolution with a manageable level of complexity. In order to provide an accurate digital representation, the SAR ADC performs the conversion process utilizing the binary search approach [5]. A critical component of the sequential approximation register (SAR) ADC design are digital-to-analog converters (DACs). An analogue device called a sample and hold circuit, often referred to as a sample and follow circuit, samples (captures, takes) the voltage of an analogue signal that is continuously changing and holds (locks, freezes) it at a constant level for a predetermined minimum amount of time[8]. A benchmark for comparing the input voltage is provided by the voltage reference, which provides a constant and precise reference voltage. The comparator chooses whether to increase or decrease the DAC output by comparing the input voltage to the reference value. High precision and linearity are attained in the DAC by using a variety of methods, including binary-weighted capacitor arrays.

A. Analog To Digital Converter

Analog-to-Digital Converters (ADCs), which are electrical components, can calculate, process, and convert the numerous analogue signals encountered in the real world into a quantized or binary format. An ADC is a fundamental component of every system that conducts digital signal processing (DSP) or digital image processing (DIP). Analog-to-Digital Converters (ADCs) are necessary since computers can only process binary signals. There are several various kinds of ADCs that are available, including Flash ADCs, Pipeline ADCs, Counter-type ADCs, Delta-Sigma ADCs, and Dual Slope ADCs.

The conversion of analogue input values occurs more quickly with the SAR ADC, despite its slower speed as compared to a Flash-type device. An analogue input's binary equivalent can be produced by the ADC in just 4 clock cycles (or conversion cycles). We benefit from accuracy using ADC.

Analogue computers of yesteryear are a thing of the past; modern technology is entirely digital. We still live in an analogue world with plenty of color rather than it is unfortunate that digital systems can only handle binary signals, limiting them to just black and white representations.

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For instance, temperature sensors like the LM35 produce a voltage that varies in proportion to the temperature, with a 10mV increase per degree. This voltage would only register as high or low based on input thresholds if we connected it straight to a digital input, providing no useful information [9].

To overcome this limitation, the analogue voltage input signal is converted by an ADC into a digital representation consisting of a number of bits. The CPU's data bus can therefore be directly attached to this digital representation, which can subsequently be used for calculation.

II. PREVIOUS WORK

The SAR is a type of analog-to-digital converter (ADC), which transforms analogue input signals into digital representations. This technique has been widely used in previous research and developments representation. Due to their versatility and widespread use, SAR ADCs are moderate speed, low power consumption, and relatively simple architecture.

Successive Approximation ADCs (SAR ADCs) have resolutions ranging. They are the preferred SAR ADCs, favored for their cost and appropriate for medium- to high-resolution applications. This kind of ADC is because due to its compact size and low power consumption, SAR ADCs are commonly employed in portable battery-powered devices.

Despite the possibility of inside circuitry, the real sample rate is still used because of the Successive Approximation approach substantially lower. This is due to the fact that, as implied by the ADC's name, the data conversion mechanism used by the internal circuitry of the device is a binary search operation. We talk about it in more detail later on in this essay.

The SAR ADC consists of a comparator that evaluates the analogue input signal, a sample-and-hold circuit (S/H), a DAC that samples the reference signal, a DAC that retrieves the analogue value of the SAR result, and a SAR logic that determines each bit.

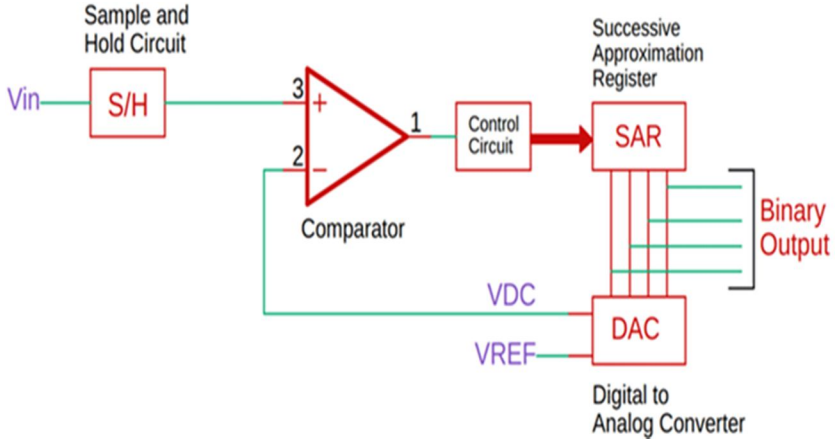


Fig: 1 SAR ADC

A. Sample & Hold Circuit

A sample and hold circuit uses a predefined span to receive continuously varying voltage analogue signals while locking at a predetermined constant voltage value [10].

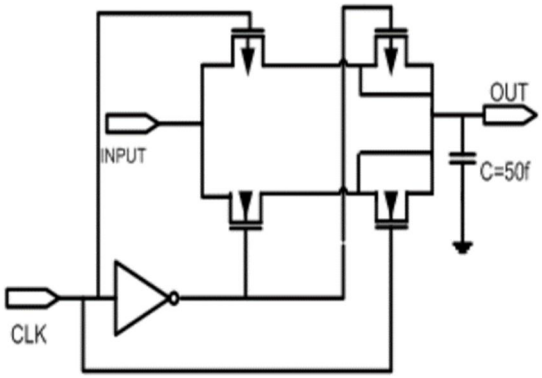


Fig: 1.1 Circuit for sampling and holding

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In this sample and hold circuit, a condenser maintains an electrical charge. One switching component—such as an active amplifier or a transistor with a field effect—is all that needs to sample and store the input data before passing it to the comparator.

B. Comparator

The electrical circuit known as a comparator or component that compares two input voltages and provides an output based on the comparison result. SAR ADCs are frequently employed in a wide range of applications, including analog-to-digital converters, voltage level detection circuits, threshold detection circuits.

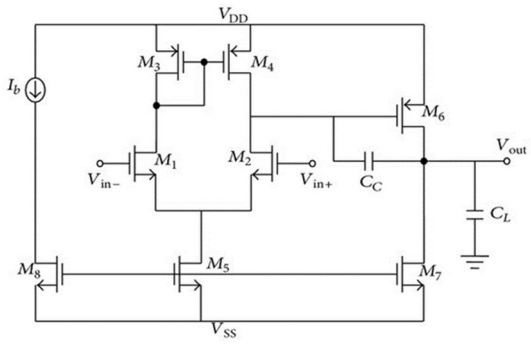


Figure 1.2 illustrates two-stage op-amp.

The two-stage op-amp consists of one differential amplifier & common source is connected in series. Each stage typically consists of a differential amplifier followed by a gain stage. This configuration is commonly used in op-amp designs to achieve high gain with improved linearity, and increased bandwidth compared to single-stage op-amps [7].

C. SAR Logic

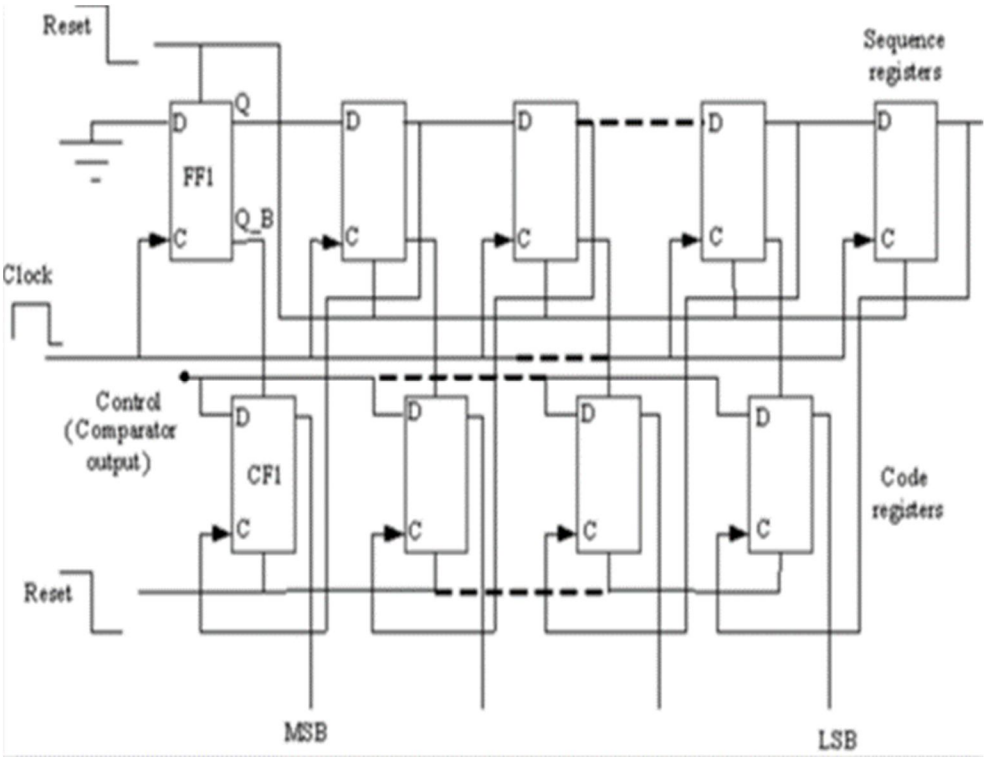


Fig: 1.3 SAR logic

Analog-to-digital converters (ADCs) frequently employ the Successive Approximation Register (SAR) design. It implements the SAR algorithm's logic using a series of D flip-flops [11]. Using D flip-flops, a SAR logic can be described in the following high-level manner:

SAR Operation: The SAR algorithm compares an analogue input signal to a reference voltage in an iterative process to determine the digital representation of the signal. In order to find the most accurate digital representation, SAR logic employs a binary search technique.

D Flip-Flop Setup: The SAR logic is made up of a chain of D flip-flops, usually in an amount that corresponds to the necessary ADC resolution. The digital output is represented by one bit per flip-flop.

Initialization: The SAR logic is initialized at the start of every conversion cycle. The remaining flip-flops are cleared to 0, while the output's most significant bit (MSB) is set to 0.

Comparatively, the SAR logic starts the iterative process by setting the output's MSB to 1. This generates a transient digital code that is later transformed into an analogue voltage by a digital-to-analog converter (DAC). A comparator is used to compare the signal from the analogue input and the DAC output.

The SAR logic makes a determination using the comparator's output as a foundation. The equivalent flip-flop is set to zero if the DAC output is greater than the analogue input. It remains at 1 in all other respects. The SAR logic loops to the next bit by shifting to the chain's next flip-flop. The process repeatedly loops back to the previous stage until all of the bits have been processed.

Final Digital Output: After each bit has been processed, the flip-flop chain has a digital output that represents the digital representation of each analogue input.

III. PROPOSED WORK

The advantages of both static CMOS (Complementary Metal-Oxide Semiconductor) and dynamic logic are combined in the logic style known as GDI (Gate-Diffusion Input), which is employed in the construction of digital circuits. Comparing GDI logic to traditional CMOS logic designs, the former offers better power efficiency, less area overhead, and easier circuit design.

An explanation of GDI logic is provided below:

1) *Basic Components:* A GDI cell, or P-type metal-oxide semiconductor (PMOS) transistor and N-type metal-oxide semiconductor (NMOS) transistor coupled in series, is the fundamental component of GDI logic. When the source and gate of the PMOS transistor are connected, a "diffusion" input is produced. The NMOS transistor's drain is its output. Contrary to conventional CMOS, GDI logic does not directly use the input signal to regulate the transistors' gate voltages. Instead, it uses a gate-input structure. The diffusion input of the GDI cell is instead controlled by a binary-encoded input signal. The number of stacked transistors in the diffusion input determines how many bits are encoded in binary. Operation:
2) *Pull-Down Operation:* The NMOS transistor is off when the input signal is "0," while the PMOS transistor is switched on. This enables the output to be pushed down to the low voltage level (ground), with the PMOS transistor acting as a switch between the output and the high voltage supply.
3) *Pull-Up Operation:* The NMOS transistor is switched on when the input signal is "1," while the PMOS transistor is off. As a result, the output can be switched between the low voltage level (Vdd) and ground using the NMOS transistor, which also serves as a switch.

A. GDI Logic's Benefits Include

Reduced Area Overhead: GDI logic has a reduced area footprint than traditional CMOS logic since fewer transistors are needed.

Power Efficiency: By GDI logic's reduced switching activities and the amount of transistors actively engaged in logic operations, power efficiency is improved.

Circuit design is made easier by GDI logic's use of a consistent GDI cell structure, which makes it simpler to build and optimize complex digital circuits.

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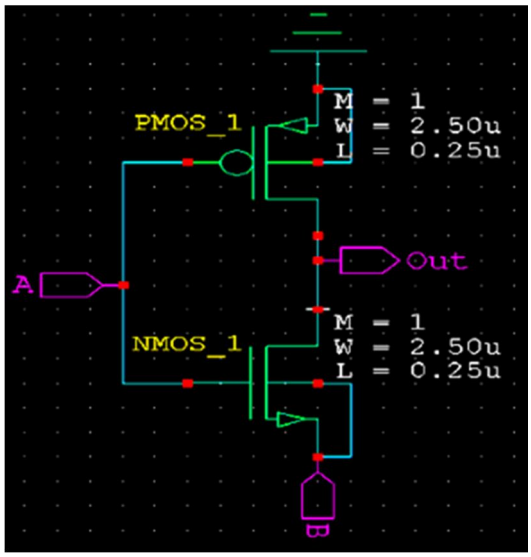


Fig: GDI for NOR gate

B. Operation

The NOR (NOT OR) action is carried out via the NOR gate, a logic gate. It has either one output or several inputs. When all of the inputs of a NOR gate are low (logical 0), the output of the device is high (logical 1).

The GDI technique is a design approach used to implement logic gates using transistors with NMOS and PMOS technology. Compared to previous transistor-level design approaches, it offers a low-cost and space-efficient solution.

We can utilize a mixture of NMOS and PMOS transistors to construct a NOR gate utilizing the GDI approach.

Here's the step-by-step explanation

Start with a PMOS transistor connected in series with a ground (GND) node. As a pull-up resistor, this transistor serves. To offer a default logic high (1) output, its gate is coupled to a common voltage source (VDD).

The PMOS transistor serves as the pull-up resistor and the NMOS transistors are used as the switching components in the GDI NOR gate. If any of the input signals are high (1), the analogous NMOS transistor conducts and pulls down the output node, forcing the output to be low (0). When all of the input signals are low (0), the PMOS transistor will continue to have a high output (1) and the NMOS transistors won't switch on until then. When a NOR gate has more than two inputs, its output is only 1 when all inputs are 0. However, if any input is 1, the output will be 0.

The GDI technique provides a compact layout and reduces the number of transistors required compared to other implementations. However, it's important to note that GDI gates have limited driving capability due to the use of NMOS transistors for both pull-down and pull-up functions. Therefore, GDI gates are generally used in low-power applications or as intermediate stages in larger logic circuits.

GDI gates offer a simple design structure with fewer transistors compared to other low-power techniques, such as stacked or footless logic. This simplicity facilitates ease of design and reduces the area overhead.

GDI gates typically have a smaller layout area compared to other low-power techniques. This makes GDI an attractive choice when area efficiency is a consideration.

The successive approximation method, a particular algorithm, is used for the conversion of analogue input signals into digital representations. SAR ADCs are extensively used in many different applications due to their average speed, low power consumption, and comparatively simple design. Because of its 8–18 bit resolution range, SAR ADCs are the chosen ADC for low-cost, medium–to–high resolution applications. This kind of ADC is utilized in mobile battery-powered devices because of its compact form size and low power consumption.

Even if the internal circuitry might operate at a much quicker rate than the sampling rate because of the Successive Approximation approach. This is due to the This ADC's internal circuitry converts the data using a binary search procedure, as the name implies. We go into more depth about it in a later section of this piece.

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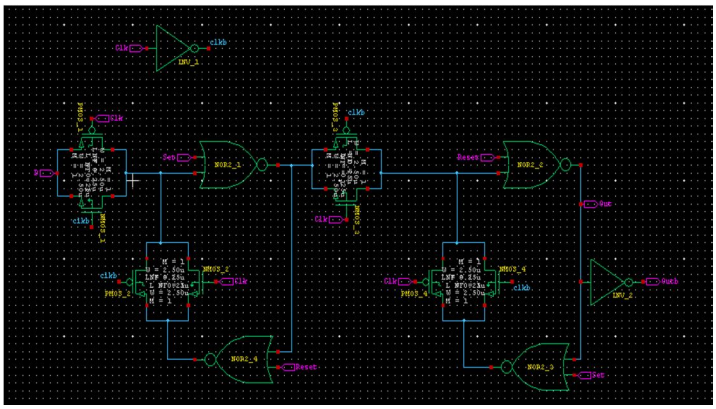


FIG: 3 internal architecture of D flip-flop using GDI Nor gate

C. DAC

A DAC is a device or circuit that converts a digital signal into an analog signal by utilizing discrete digital values. It generates a continuous analogue output that is proportionate to the input digital value by taking a succession of discrete digital values—typically expressed as binary numbers—and converting them into discrete digital values.

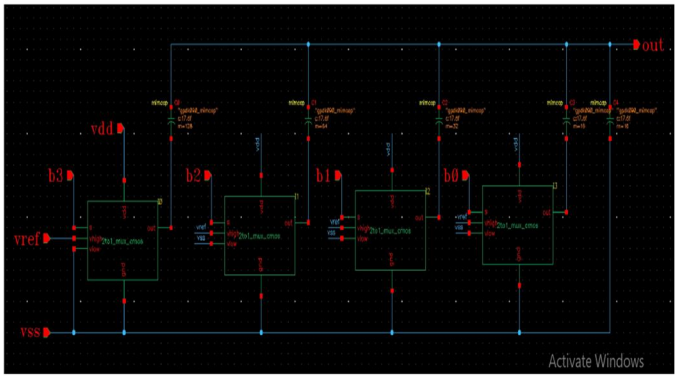


FIG: 4 DAC Schematic of 2:1 mux in CMOS

A power of two's presence or absence in the entire sum of the powers is represented by each bit in the binary system, which is a positional system, or place value system.

To put it another way, the entire digital to analogue conversion process can be compared to a scaling operation, where the binary count is mapped to a range of voltages, with 0V serving as the minimum and maximum input binary voltages, respectively.

IV. EXPERIMENTAL RESULTS

A. Schematic

Schematic for ADC using GDI technique Nor gate

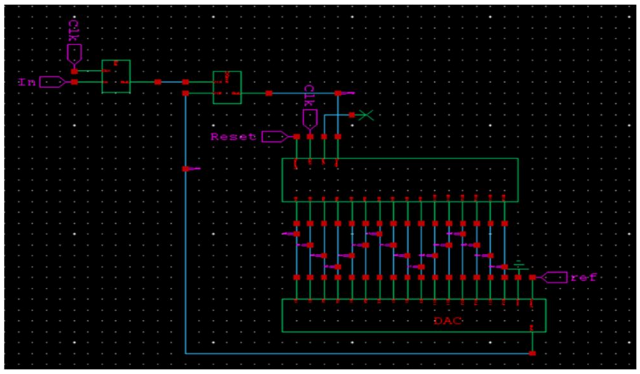


Fig: 5 Schematic for power efficient SARADC

B. Waveform

This is the waveform regarding to SARDAC using GDI technique.

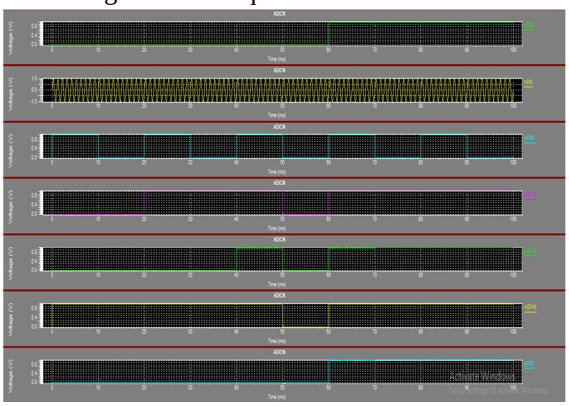


Fig: 6 Waveform for power efficient SARADC

C. Comparison Table

In existing method we used CMOS technology but compared to that GDI technique gives less power consumption and delay.

METHOD	AREA	POWER	DELAY
EXISTING METHOD	1130	0.991mw	14.43ns
PROPOSED METHOD	1130	23.3µW	34.46ns

Table 1: comparison between proposed and existing method

V. CONCLUSION

This paper16-bit successive Tanner 250nm GDI technology simulates the ADC approximation functionally. As the SAR ADC consumes more power, to achieve minimum power consumption, a low-power comparator and DAC are utilized. In the domain of biomedical applications, it was believed that the SAR ADC was more appropriate. Providing a summary of the SAR ADC brings this endeavor to a close. The outputs supplied with this logic are quite solid, according to the GDI-based SAR ADC, and they have less area, latency, and power. As technology continues to evolve, SAR ADCs are expected to further advance in terms of resolution, speed, power efficiency, and integration capabilities. These advancements will enable SAR ADCs to meet the increasing demands of modern applications, ensuring accurate and reliable conversion from analogue to digital for a variety of technologies in various industries.

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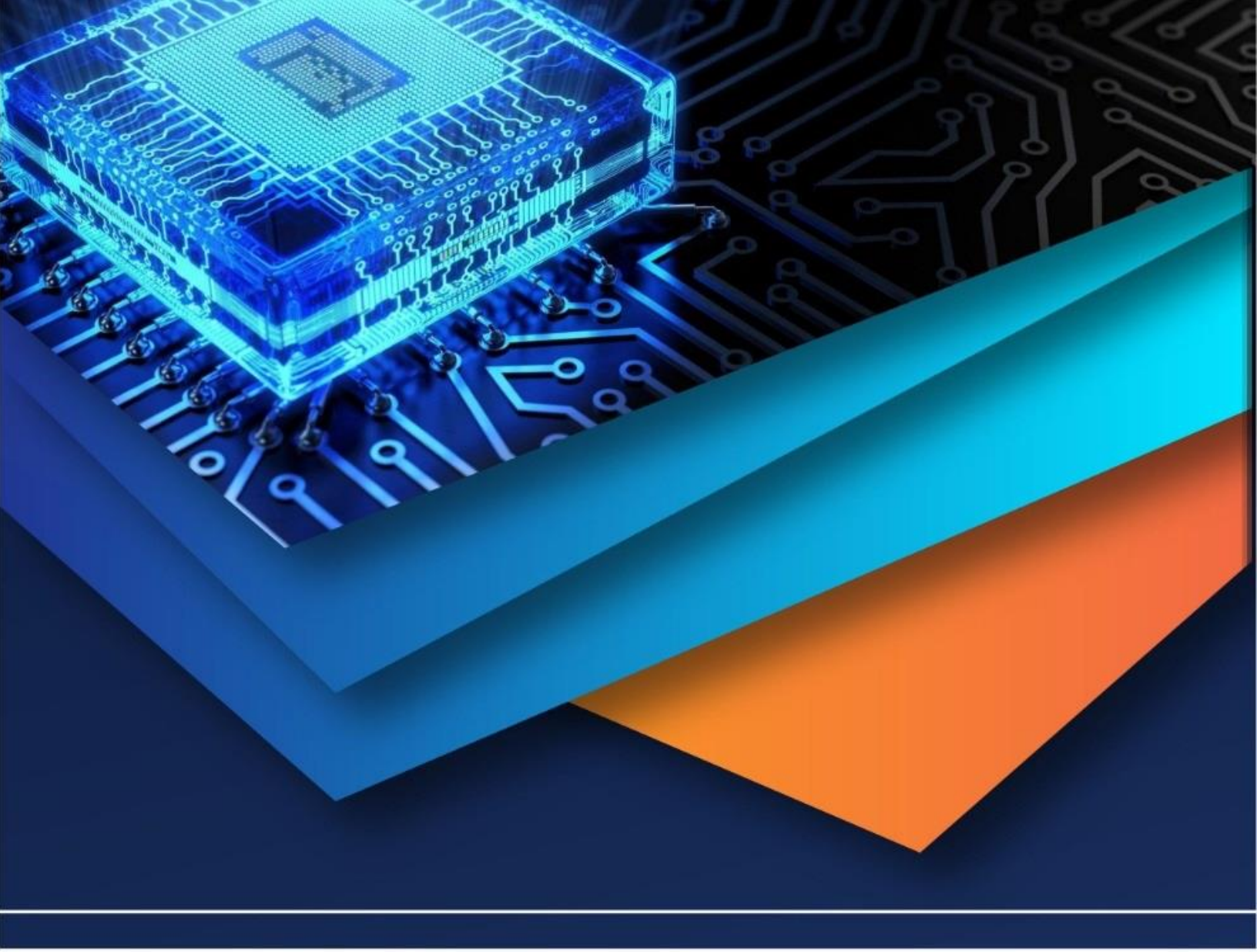
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