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Design and VLSI implementation of SRAM memory array using Application-specific Integrated circuits design flow

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Abstract ***Static Random-access memory (SRAM) are useful structure blocks in operations like data storage, embedded operations, cache recollections, microprocessors. The circuits should retain larger impunity to noise voltages. So, the Stationary Noise Margin (SNM) of the circuits should be veritably high. Large SRAM arrays that are extensively used as cache memory in microprocessors and operation-specific integrated circuits can absorb a big portion of the chip area. Highly compact circuits like SRAM arrays are estimated to cover relatively 90% of the System on chip area within the coming years. To optimize the performance of similar chips, large arrays of fast SRAM help to speed up the system performance. As a result, numerous minimal-size SRAM cells are tightly packed making SRAM arrays the compact circuitry on a chip. In this work an attempt is made to design a 8 X 8 SRAM memory array along with different components like Write driver circuit, Pre-charge circuit, Row and Column Decoder. Different SRAM architectures such as 6T, 7T and 8T are designed and different parameters such as Static Noise Margin and power dissipated are measured and the best performing memory design has been selected. 8T design has been resulted with least power dissipation. Hence this cell is selected for designing the memory array. A schematic of 8 x 8 array is designed and the layout of single SRAM 8T is created and to complete the ASIC design flow, DRC is done and the pre and post simulation are compared and verified. The integrated SRAM is operated with an input voltage of 0 to 1.8V.***

I. INTRODUCTION

Memory is a component that holds the state of a task for the duration it is needed. It is a block that holds the data and instructions that are needed by the CPU for execution. Static random access memory (SRAM) is a volatile memory present onchip. It is mainly used as cache memory. With the advent of technology, a large number of research is being conducted to reduce the power and area and increase the memory cell's stability. There is a dire need to know the one that best suits the application with the various architectures present. There is no single architecture that can suit the designer's need, it boils down to the kind of application that is being designed, and the various constraints like area of the chip, the power dissipated etc. are being taken into account before determining the kind of memory that is needed. This report presents a detailed comparative study on the 3 different SRAM memory architectures. A 8T SRAM with its layout and its back annotation is done.

Static Random Access Memory (SRAM) is a type of volatile memory that is commonly used in digital electronics applications to store small amounts of data. The design of an SRAM involves creating a circuit that is capable of storing and retrieving data quickly and reliably. The main challenge in designing an SRAM is to balance the conflicting requirements of high speed, low power consumption, and small area. The circuit must also be able to operate reliably over a wide range of operating conditions such as temperature and supply voltage. Additionally, the design must take into account factors such as the number of memory cells required, the access time, the power consumption, and the overall cost. Therefore, the design of an SRAM involves careful consideration of various tradeoffs and optimization techniques to ensure that the resulting circuit meets the desired specification

II. THEORETICAL BACKGROUND

Static Random Access Memory (SRAM) is a type of volatile memory that is widely used in digital electronic devices, such as computers and mobile phones, for storing data that needs to be accessed frequently and quickly. SRAMs are typically implemented as arrays of memory cells, each consisting of a flip-flop circuit that can store one bit of data.

Designing and implementing an SRAM memory array using Application-specific Integrated Circuits (ASICs) design flow involves several stages, including:

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1) *Specification and Architecture Design:* In this stage, the specifications and requirements of the SRAM memory array are defined. This includes the number of memory cells, the size of each cell, the data access time, the power consumption, and other parameters. The architecture of the memory array is also designed, which involves selecting the type of memory cell, the number of rows and columns in the array, and the organization of the memory.
2) *Circuit Design:* In this stage, the individual circuits that make up the SRAM memory array are designed. This includes designing the flip-flop circuits that store the data, the bit-line and word-line circuits that enable data access, and the sense-amplifier circuits that amplify the signals from the memory cells.
3) *Layout Design:* In this stage, the physical layout of the SRAM memory array is designed. This involves placing the individual circuits on the chip, routing the interconnections between the circuits, and optimizing the layout for performance and reliability.
4) *Verification:* In this stage, the design is verified to ensure that it meets the specifications and requirements. This includes simulating the circuit behavior, testing the layout for timing and signal integrity, and verifying the functionality of the memory array.
5) *Fabrication:* In this stage, the ASIC chip is fabricated using semiconductor manufacturing processes. This involves creating the silicon wafer, depositing and patterning the layers of materials that make up the circuits, and testing the functionality of the chip.
6) *Testing and Characterization:* In this stage, the fabricated chip is tested to ensure that it meets the specifications and requirements. This includes testing the functionality of the SRAM memory array, measuring the timing and power characteristics, and characterizing the chip for reliability and yield.

III. DESIGN AND IMPLEMENTATION

A. *Design for Implementation SRAM memory array*

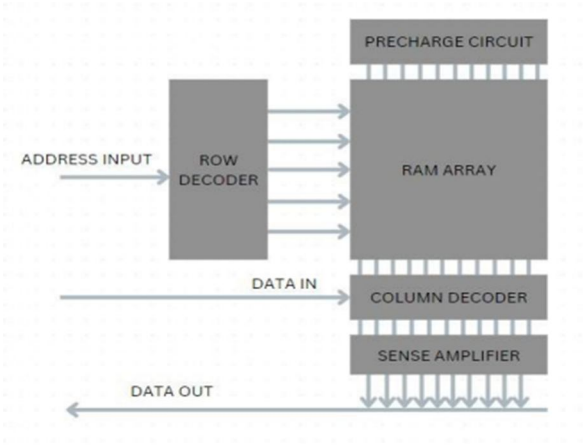


Figure 3.1: Block diagram of SRAM Array Architecture

1) *RAM Array:* Includes SRAM bit cells which should occupy minimum area to achieve cell density i.e number of 1bit SRAM cells per unit area should be as high as possible.
2) *Decoder:* Memory cell matrix consists of rows and columns. Each row is accessed through word line while each column is accessed through bit line. Data lines are responsible for transferring data to and from bit lines depending upon write and read operation respectively. Generally, by making word line high entire word is obtained. So, column decoder is used to distinguish among columns.
3) *Sense Amplifiers:* Bit stored in a memory cell is determined by the voltage across bit lines. However, due to large number of cells connected to a column circuitry, it is difficult to get a proper output. Therefore, sense amplifiers are used as it gives stability and reliability to circuitry.
4) *Pre-charge circuit:* Before every read and write operation, pre-charge becomes high and both bit lines are charged to a value Vdd/2. During pre-charge and equalizer cycle, both bit lines are shorted so that voltage difference across them is zero. When pre-charge is off and sense amplifier turns on, it senses small voltage difference between two bit lines and accordingly stores a bit in memory cell.

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5) *Read Write Circuit:* The read-write circuit in SRAM is responsible for reading and writing data to and from the memory cell. It consists of a sense amplifier, write driver, and bitlines. During a read operation, the sense amplifier senses the voltage difference between the bitlines and amplifies it to determine the stored data. During a write operation, the write driver applies a voltage to the bitlines to write the desired data into the cell. The read-write circuit operates at high speed and low power to ensure efficient operation of the SRAM.

B. Circuit Description

1) *Decoder:* It is just a combinational circuit that converts binary information from n input lines to maximum of 2n unique outputs. Enable inputs must be on for the decoder to function otherwise its outputs assume a single "disabled" output code word. With this the binary input conversion gets easier with the operation and we need for the desired output from this kind of combinational output by which we can use it for no of operations like data, word line selection for the memory cell. And also for the other digital information storage working.

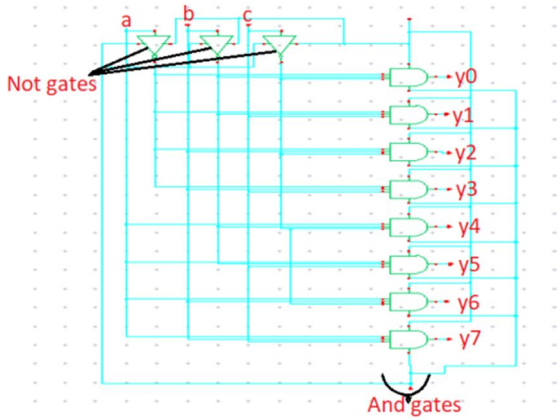


Figure.3.2 Decoder circuit

2) *Pre Charge Circuit:* Sense amplifier are the vital component in the memory design. The job of sense amplifier is to sense the bit line for proper monitoring action. It improves the read and write speed of the memory cell. Its another job is to reduce the power needed for the operation. The sense amplifiers primary job is to amplification of the voltage is being produced on the bit line at the time of operation. As it has the important job in the memory so it has different circuits for the operation. As we know that in SRAM operation we don't need refresh of the memory for the further process, so the sense amplifiers non destructive at the time of operation. As the column multiplexers are connected in the memory cell at that time multiplexer should choose one sense amplifier for the single input. So that we can get proper use of the sense amplifier in the designing circuit. These are the various parameters of an sensing amplifier

Gain A = Vout/Vin.

Sensitivity S =vin min - least noticeable sign

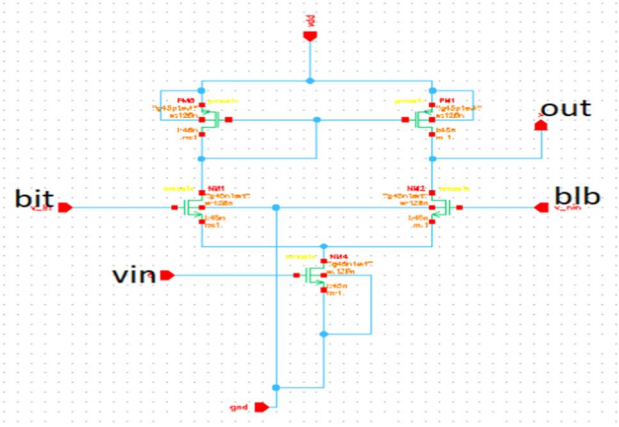


Figure 3.3: Sense Amplifier

3) *Read Write Circuit:* The read-write circuit in SRAM is responsible for the critical task of reading and writing data from and to the memory cell. The circuit consists of several components, including the bitlines, write driver, sense amplifier, and control logic i.e write enable. During a read operation, the control logic activates the wordline corresponding to the desired memory cell, which in turn drives the stored data onto the bitlines. The sense amplifier then amplifies and compares the voltage difference between the bitlines to determine the stored data. During a write operation, the control logic activates the wordline and applies the desired data to the bitlines using the write driver. The stored data in the memory cell is then updated based on the voltage level on the bitlines. The read-write circuit operates at high speed and low power to ensure efficient operation of the SRAM. The sense amplifier and write driver consume most of the power in the circuit and are designed to operate quickly to minimize the time required for data access.

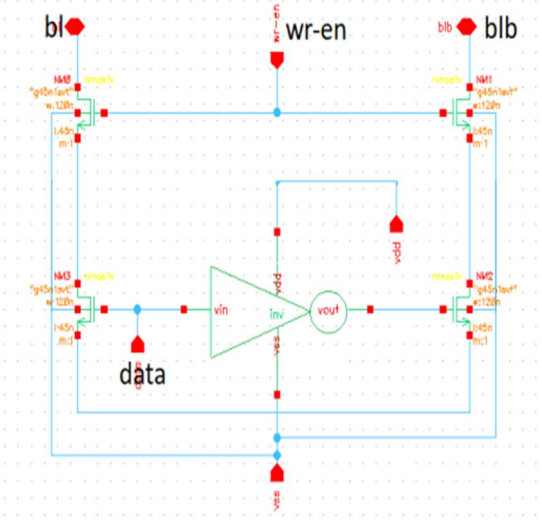


Figure 3.4: Read Write circuit

C. *Simulation of Different SRAMs*

1) *6T SRAM:* 6T SRAM consists of two cross coupled inverters and two access transistors as shown in below figure.

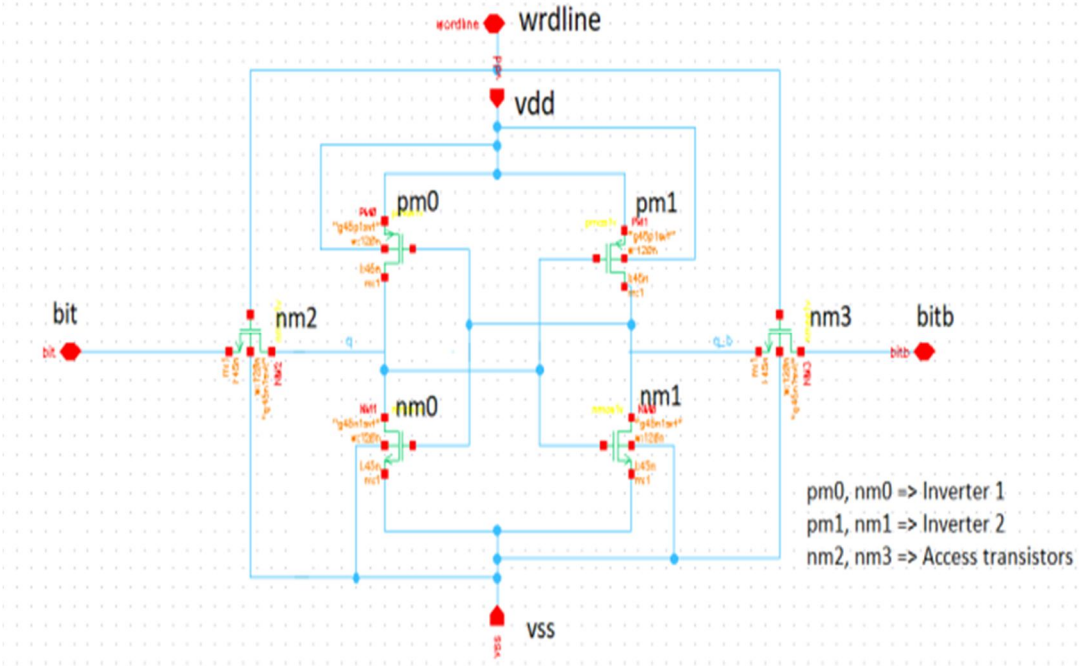


Figure 3.5: 6T SRAM

2) 7T SRAM: 7T SRAM has an extra pull down transistor(nm4) which helps in holding of data during hold operation.

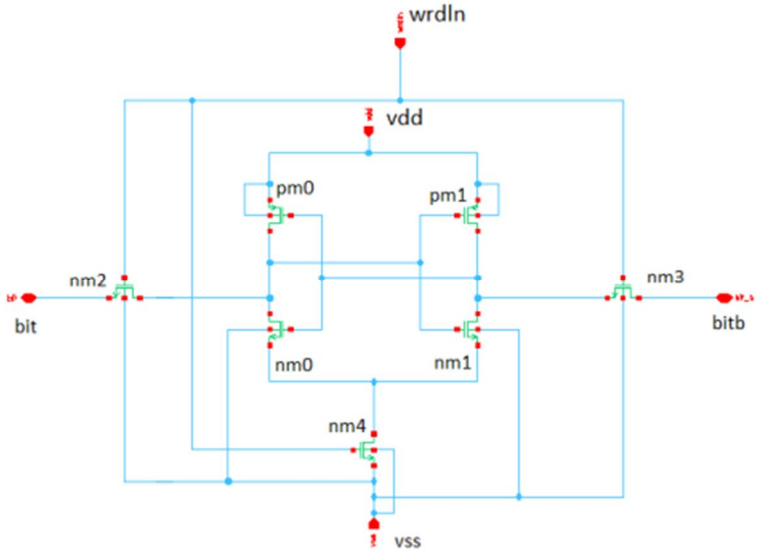


Figure 3.6: 7T SRAM

3) 8T SRAM: 8T SRAM has different word lines (rwl & wwl) for read and write operation.

wwl- write word line
rwl- read word line
wbl- write bit line
wblb- write bit line bar
rbl- read bit line

- It is enhanced 6T SRAM. Read and Write are decoupled (independent read and write)
- Stability is better
- Can do read and write at the same time
- Advantage : low voltage operation
- Disadvantage: Area increases

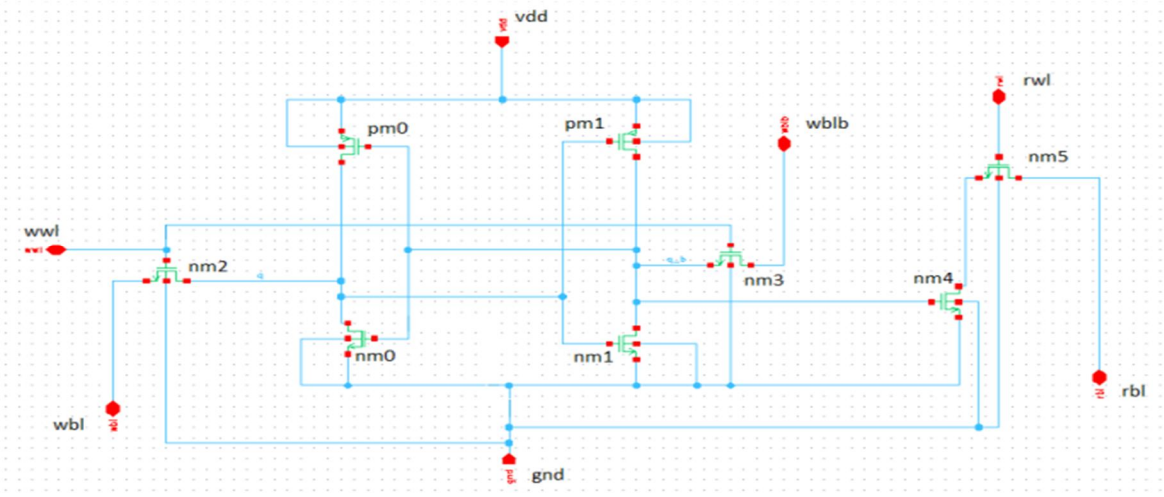


Figure 3.7: 8T SRAM

D. 8x8 SRAM Memory Array

A 8 x 8 memory array is designed using the 8T as the base memory cell. Two Decoders – Row Decoder and Column Decoder are also designed. Initially the output of the row decoder was connected with the word line of the cells of each row. The column decoder was connected with the bit line and an internal inverter was used to give the negated value to the bitline bar. Some of the problems faced with this design were as follows

- During the write operation for a particular cell, the word line for the entire row would be high. Therefore, since all the other outputs of the column decoder would be 0, all the remaining cells would be refreshed and hence all the data would be lost.
- While selecting a particular cell, the corresponding row decoder and column decoder lines has to be high, by doing so we can write a logic "1" into the cell. But it is not possible to write a logic "0" with this design.
- Hence if the column decoder line should not be used as the bit line, but then the selection of a particular cell to read or write would not be possible. Hence to overcome all these problems we have added an AND gate whose inputs would be from the row and column decoder lines and the output of the AND gate would go to the word line of respective cells. All the bit lines of all the memory cells are shorted together, hence whatever value has to be written into the cells will be given into this bit cell and the value will be written to only that particular cell whose row decoder and column decoder lines are high hence enabling their word line. With these changes in the design all the above stated problems have been solved.

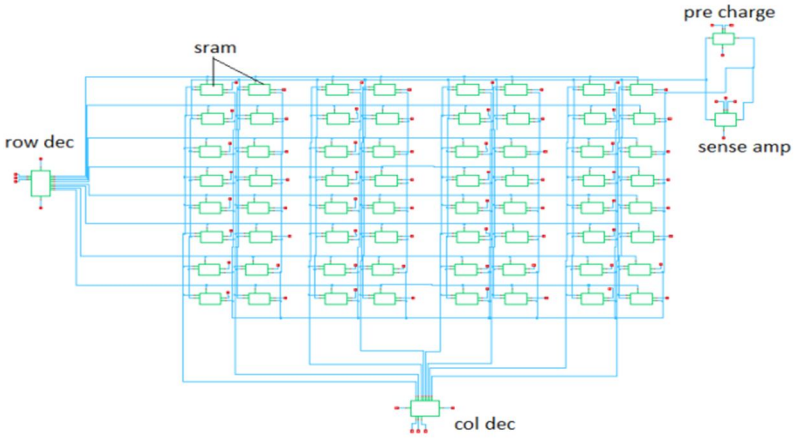


Figure 3.7: 8x8 SRAM array

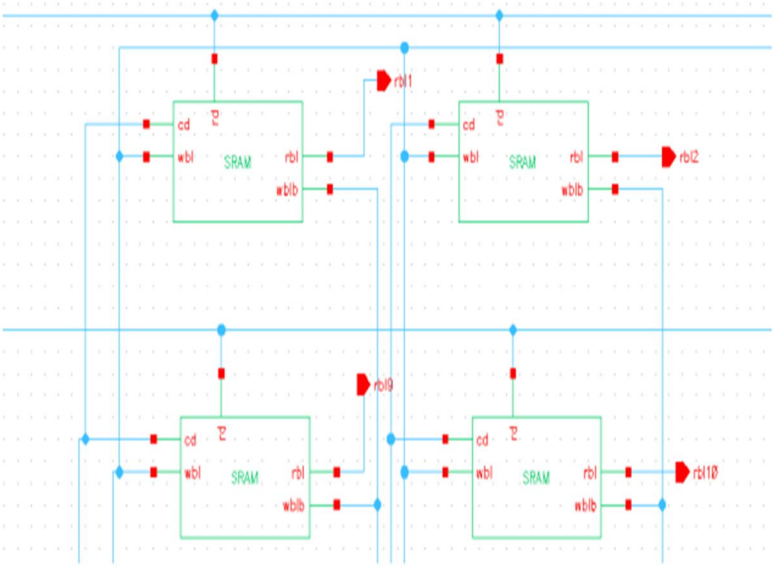


Figure 3.8: Zoomed view of SRAM array

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IV. RESULTS AND DISCUSSION

A. *Peripheral Circuits Output*

1) *3:8 Decoder Output:* The schematic of the 3:8 Decoder is prepared, simulated and the outputs are observed and verified. Decoder schematic is constructed using inverter and 3 input and gate.

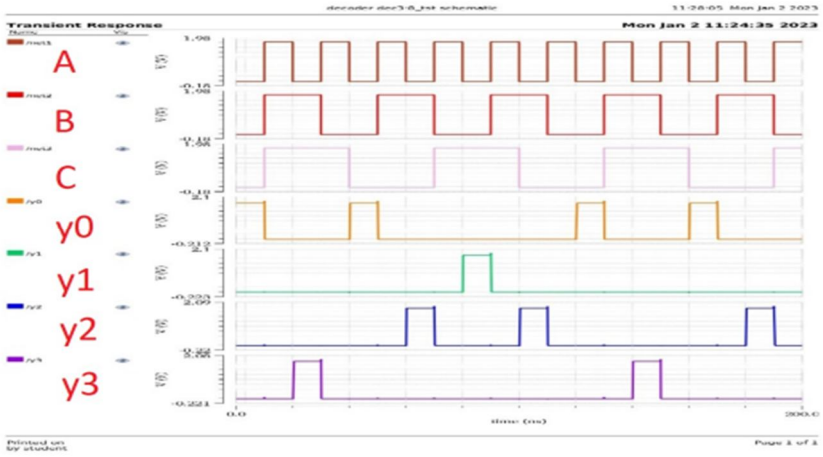


Figure 4.1: Decoder circuit output

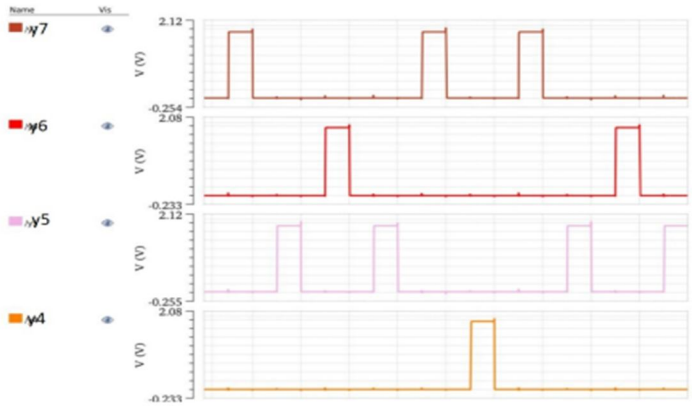


Figure 4.2: Decoder circuit output

A 3:8 decoder is a digital circuit that takes in 3 input signals and produces 8 output signals. It is also known as a 3-input to 8-output decoder. The decoder works by enabling one and only one of the output lines based on the input combination. The input lines A, B, and C can be either high (1) or low (0). Based on the combination of the input signals, one and only one of the output lines will be high (1), and the rest will be low (0).

For example, when **A**=0, **B**=1, and **C**=0, only **Y2** will be high (1), and all other output lines will be low (0).

2) *Pre Charge Circuit Output:* The schematic of the Pre-charge circuit is constructed, simulated and its outputs are observed and verified

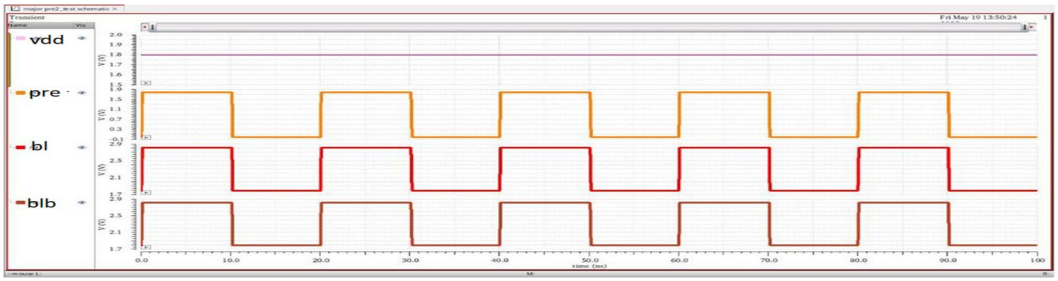


Figure 4.3: Pre charge circuit output

A precharge circuit graph includes an input line labeled "Pre" on the left side and an output line labeled "bl (bitline) and blb (bitbar line)" on the right side. When the "Pre" signal is activated, the precharge circuit charges the output node to a predetermined voltage level, typically the power supply voltage (Vdd). This ensures a known starting point for subsequent evaluations or computations. The precharge circuit disconnects the output node from other components, allowing it to be charged independently. It is commonly used in dynamic logic circuits to maintain stability and facilitate proper operation.
For example, when **pre**=low (0) then **b1**, **blb**=low (0) and when **pre**=high (1) then **b1**, **blb**=high (1)

3) *Read Write Circuit Output:* The schematic of the Read Write circuit is constructed, simulated and its outputs are observed and verified.

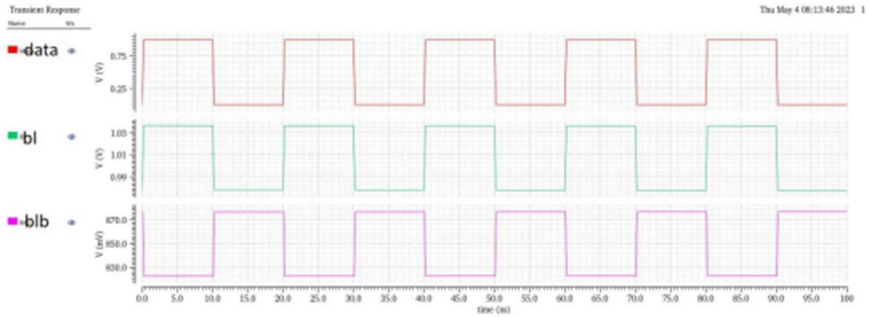


Figure 4.4: Read Write circuit output

The read/write circuit manages the flow of data between the external source and the memory/storage, facilitating both reading and writing operations. During a read operation, the control logic activates the wordline corresponding to the desired memory cell, which in turn drives the stored data onto the bitlines (Data is low implies bitline will be low). During a write operation, the control logic activates the wordline and applies the desired data to the bitlines using the write driver (when data is high bit line should be high).

B. Output of SRAM cells

1) 6T,7T,8T SRAM output

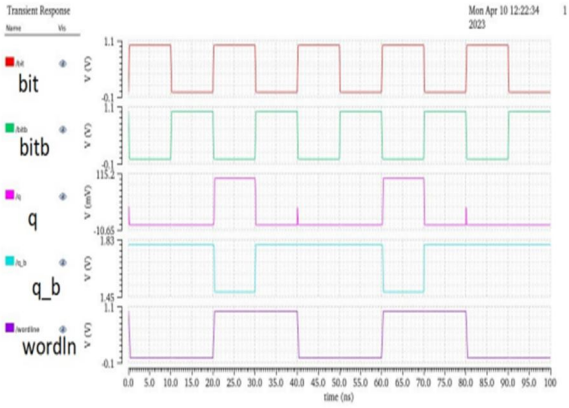


Figure 4.5: 6T simulation output waveform

In a 6T SRAM cell, the output is typically represented by a single bit stored in the memory cell. When the "Wordline" signal is activated (high), it allows access to the SRAM cell. If the cell stores a logic high (1), the "Data" output line would reflect a high voltage level. Conversely, if the cell stores a logic low (0), the "Data" output line would indicate a low voltage level.
For example, when bitline is high (1), **q** stores 1and **qb** will store 0 only if world line is high.

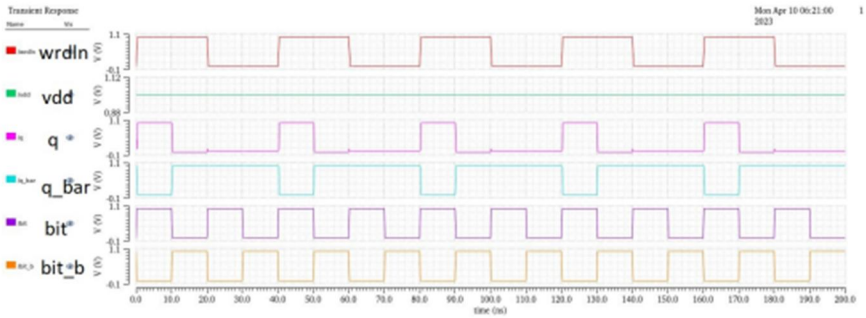


Figure 4.6: 7T simulation output waveform

In a 7T SRAM cell, the output is typically represented by a single bit stored in the memory cell. The cell consists of seven transistors arranged in a cross-coupled configuration, similar to the 6T SRAM cell but with an additional pass transistor. The graph illustrates the relationship between the "Wordline" signal activation and the corresponding output data value. When the "Wordline" signal is activated (high), it allows access to the SRAM cell. If the cell stores a logic high (1), the "Data" output line would reflect a high voltage level. Conversely, if the cell stores a logic low (0), the "Data" output line would indicate a low voltage level.
For example, when bitline is high (1), **q** stores 1and **qb** will store 0 only if world line is high.

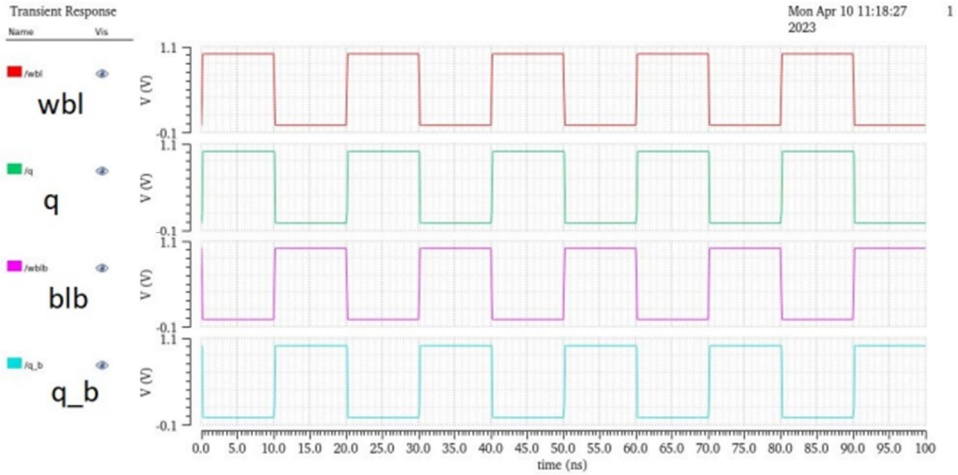


Figure 4.7: 8T write operation output waveform

8T SRAM is enhanced 6T SRAM where read and write operation can be done at a time as read and write circuit are decoupled. In the above 6T,7T SRAM we can see there is common wordline for both read and write operation but in 8T there is a separate wordline for read and write operation i,e write word line(wwl)for write operation and read word line (rwl) for read operation.
For write operation - Can write the value 0 or 1 into **q** by using write bit line(wbl) making the write world line(wwl) high.



Figure 4.8: 8T read operation output waveform

For read operation – read word line(rwl) should be high, and if read bit line(rbl) is high whatever the value stored in q will be copied.

For more understanding - To do the reading, rwl should be high, assume rbl and qb is high (1) which implies nmos (nm4) in the circuit (Figure 3.7: 8T SRAM) which connected to ground will be on and allows rwl value decrease towards low (0) value which conclude value of q is low (0).

2) Static Noise Margin

Static noise margin is used to measure the stability of memory cell in the presence of Noise. It can be defined as the minimum voltage that can be applied at storing nodes so that flipping of state occurs. By using the voltage transfer characteristics of two inverters present in the memory cell we can calculate SNM. The inverters present in the memory cell are used to keep up stable states and their output nodes hold the information stored in the memory cell Because of the noise exists at storing nodes the node voltages starts fluctuating and stability of cell degrades. The SNM measures the permitted levels of the noise voltages and accordingly the capacity of these inverters to hold their state in the vicinity of noise.

Static Noise Margin (SNM) = maximum length of diagonal of the square Butterfly curve has been used to find SNM of different SRAM cells.

SNM of 6T SRAM = 299mV

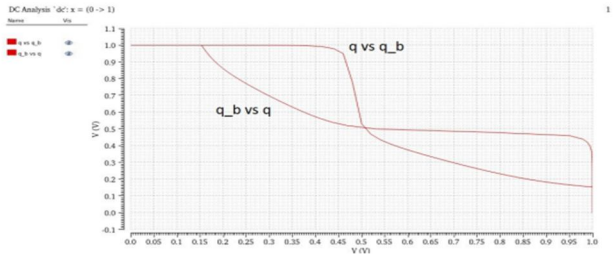


Figure 4.9: 6T snm waveform

SNM of 7T SRAM = 375 Mv

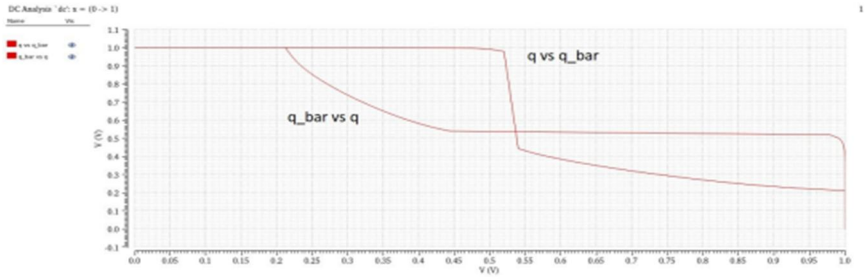


Figure 4.10: 7T snm waveform

SNM of 8T SRAM = 299mV

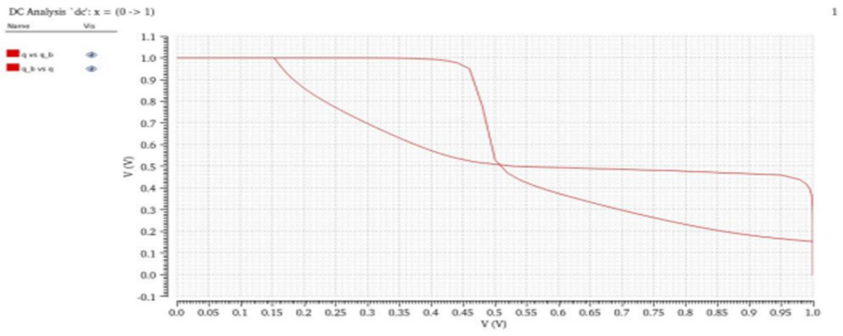


Figure 4.11: 7T snm waveform

3) Power Consumption

Low power static random access memories (SRAM) has become a critical component in modern VLSI systems. In cells, the bitlines are the most power consuming components because of larger power dissipation in driving long bitline with large capacitance. The cache write consumes considerable large power due to full voltage swing on the bitline. The aim of the project is to get a new SRAM cell to reduce the power consumption during write and read operation.

Waveforms to determine power consumed by different SRAM cells has been plotted.

Avg power consumption of 6T SRAM = 16.36µW

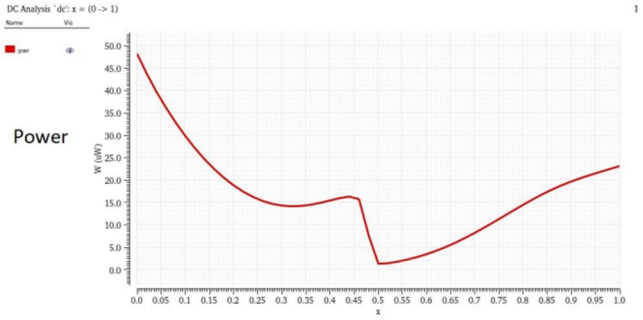


Figure 4.12: 6T power consumption waveform

Avg power consumption of 7T SRAM = 13.42µW

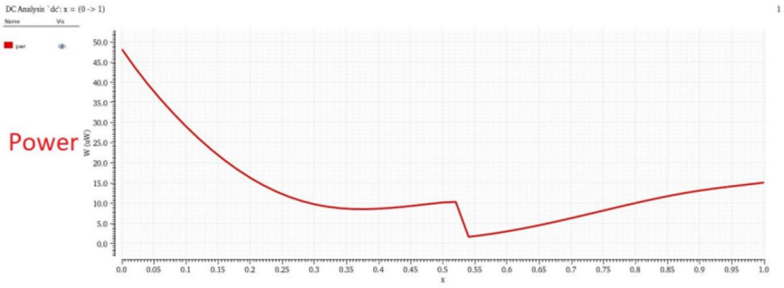


Figure 4.13: 7T power consumption waveform

Avg power consumption of 8T SRAM = 16.36µW

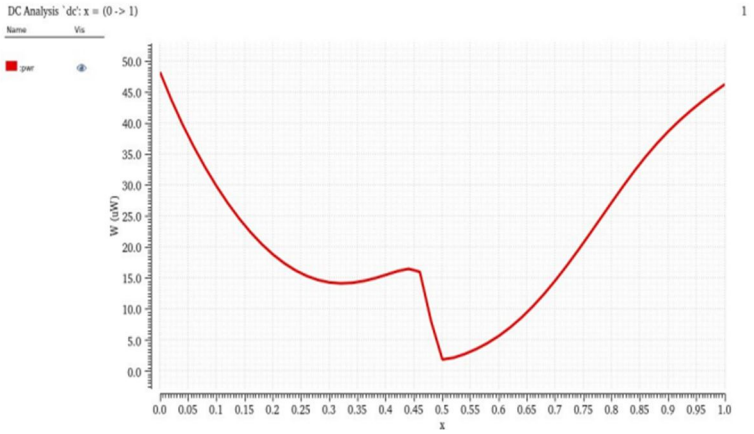


Figure 4.14: 8T power consumption waveform

C. Layout of 8T SRAM cell

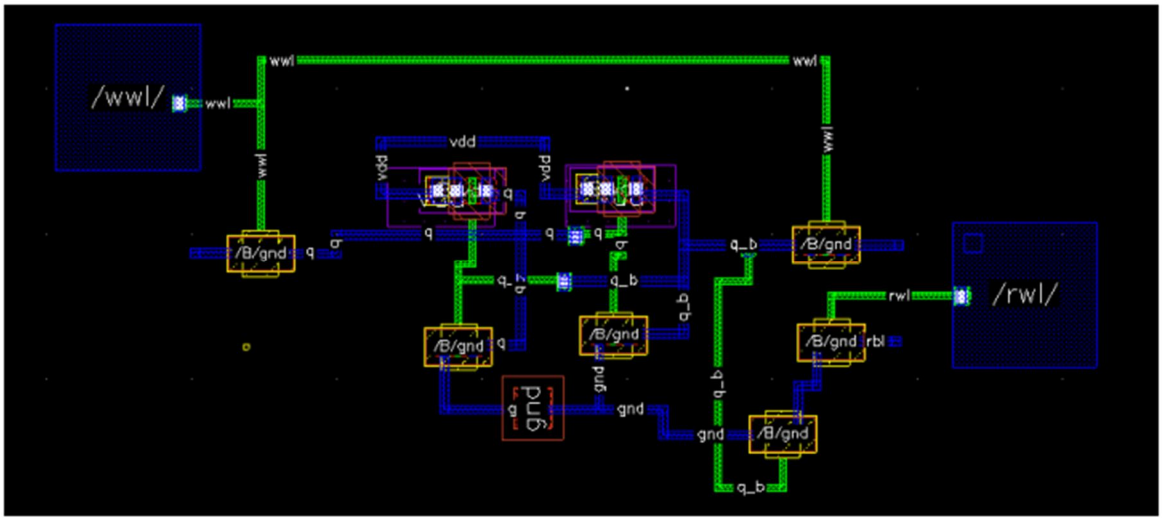


Figure 4.15: Layout of 8T SRAM

V.CONCLUSION

This work compares different SRAM cell architectures along with their various parameters. A 8T cell is designed which outperforms the standard SRAM cells in terms of the power dissipated by the source. The major focus of this work was to compare the Static Noise Margin and Power dissipated of each of the cells. There is no single architecture that can be concluded to be the best suited for every application. 8T can be intuitively chosen for low power applications, as it consumes less power as compared with the other architectures and also has a similar comparable snm as the other architectures, which makes it suitable for highly accurate and reliable applications. There always exists a trade-off in every cell and it boils down to the liability of the designer to choose the one that fits best for the specific application.

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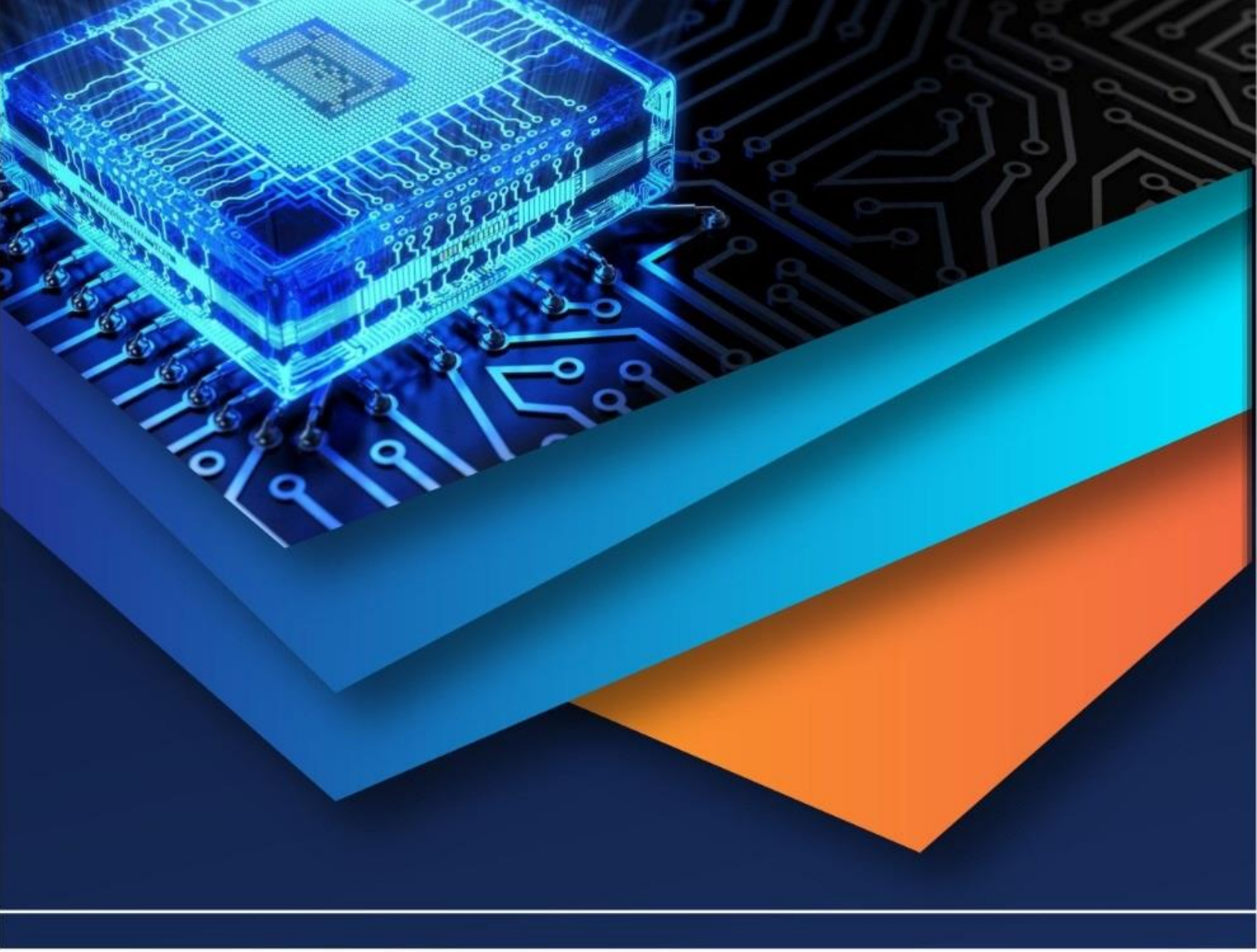
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