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Design Automation of 2 Stage COMS Op-Amp Using PSO Algorithm

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Abstract: ***Operational amplifiers, also referred to as op-amps, are crucial components of electronic circuit design that find extensive use in signal processing, amplification, and control systems, among other areas. As demands for better circuit performance, efficiency, and compactness continue to rise, optimizing op-amp designs is essential. In this research, the particle swarm optimization algorithm with LTSpice simulation is used to create and optimize a three-stage CMOS op-amp using state-of-the-art approaches. A baseline op-amp circuit is produced through laborious design iterations and performance evaluations carried out within LTSpice. This serves as the foundation for additional optimization efforts. The PSO method in MATLAB is then applied as the optimization process moves forward.***

Particle Swarm Optimization is a computational optimization methodology inspired by the social behaviour of organisms such as bird flocking and fish schooling. In Particle Swarm Optimization, a population of potential solutions, called particles, moves through the search space. Both the global best-known location and each particle's unique best-known position affect its motion of the swarm. The project intends to obtain optimal op-amp performance by balancing design trade-offs and pushing the frontiers of efficiency and innovation through the combined power of LTSpice simulation and MATLAB optimization. Designers can find the best op-amp configurations that adhere to strict design specifications more quickly by combining the strengths of both tools. In the end, this project shows evidence of the integration of optimization and simulation methods in electronic circuit design. Through the use of LTSpice for circuit simulation and the PSO method for optimization, designers can explore new avenues for op-ampdesign, hence promoting breakthroughs in electronic systems and electrical engineering innovation.

Operational amplifiers play a crucial role in modern electronic circuits, finding applications in a wide array of systems including signal processing, instrumentation, and control. This paper presents a comprehensive methodology for the design and automation of a three-stage operational amplifier using LTspice simulation software and MATLAB scripting. The aim of this work is to achieve a high-performance opamp design while minimizing manual intervention and optimizing the design parameters efficiently.

The design process begins with the definition of specifications such as gain, bandwidth, slew rate, and power consumption, which are essential for determining the required characteristics of each stage in the opamp. Subsequently, an initial schematic is developed in LTspice, incorporating three amplifier stages: differential input stage, intermediate gain stage, and output buffer stage. Each stage is carefully designed to meet the specified requirements while ensuring stability, linearity, and low distortion.

LTspice is utilized for circuit simulation, allowing for accurate performance evaluation under various operating conditions. Monte Carlo analysis and corner-case simulations are performed to assess the robustness and reliability of the opamp design against process variations and environmental factors. Through iterative simulations and optimization, the circuit parameters are fine-tuned to achieve the desired performance metrics.

To automate the design process and enhance efficiency, MATLAB scripting is employed for parameter extraction, optimization, and post-processing of simulation results. MATLAB interfaces with LTspice through the Control Panel feature, enabling seamless communication and data exchange between the two platforms. Optimization algorithms such as genetic algorithms or particle swarm optimization are implemented to systematically explore the design space and converge towards an optimal solution. The proposed methodology offers several advantages including reduced design time, improved design robustness, and scalability for complex opamp architectures.

Moreover, the automation framework facilitates rapid prototyping and iteration, allowing designers to efficiently explore design trade-offs and optimize performance metrics. In conclusion, the integration of LTspice simulation and MATLAB automation provides a powerful framework for the design and optimization of three-stage operational amplifiers. The presented methodology demonstrates the feasibility of achieving high-performance opamp designs with enhanced efficiency and reliability, paving the way for advancements in analog integrated circuit design.

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I. INTRODUCTION

This chapter introduces an overview of CMOS 2-stage operational amplifier and fundamental concept of Particle Swarm Optimization (PSO). Section 1.1 presents an overview of 3-stage CMOS op-amp, section 1.2 discusses about Particle Swarm Optimization, section 1.3 presents the objective of the project and section 1.4 presents the organization of the project.

A. Introduction

Op–amp's are the backbone of modern electronic circuits, providing indispensable functionality in a wide array of applications ranging from audio amplification to sensor signal conditioning. Their versatility and reliability make them integral components in electronic devices and systems across various industries. However, designing op-amp circuits presents a myriad of challenges for engineers. These challenges include achieving optimal performance metrics such as gain, bandwidth, and stability while balancing constraints such as power consumption and cost. Moreover, the relentless drive for miniaturization and integration exacerbates these challenges, necessitating the development of efficient design and optimization techniques.

The two-stage CMOS op-amp consists of two main stages:

1) Differential input stage and
2) Output stage.

In the differential input stage, differential pairs of transistors are utilized to achieve high input impedance, differential gain, and common-mode rejection. The output stage, typically a common-source amplifier, provides additional gain and drives the output signal to the desired level. Designing a three-stage CMOS op-amp to achieve required performance specifications like gain, bandwidth, and stability requires careful consideration of transistor sizes, biasing arrangements, and compensating strategies.

The popular circuit simulation program LT-Spice provides a strong platform for modeling and debugging op-amp circuits. Circuit behavior may be seen, transient and AC analysis can be carried out, and design iterations can be made to maximize performance with LT-Spice. Designers can validate the functionality of the two-stage CMOS op-amp, simulate its behavior under many operating conditions, and improve the design to satisfy performance requirements by utilizing LT-Spice. Furthermore, designers can investigate

trade-offs in their designs, evaluate the effects of parameter changes, and spot possible difficulties like distortion or stability concerns with LT-Spice.

B. Particle Swarm Optimization (PSO)

The computer optimization method known as Particle Swarm Optimization (PSO) was motivated by the social behaviours of creatures like fish schools and flocks of birds. A population of possible answers, referred to as particles, traverses the search space in PSO. Both the global best-known position of the swarm and each particle's best-known position impact its motion.

Here's a brief overview of how PSO works:

1) Initialization: To start, PSO randomly initializes a population of particles in the search space. Every particle is a possible answer to the optimization issue.
2) Assessment: Every particle's fitness is assessed using an objective function, also known as a fitness function, that gauges how well the particle is positioned inside the search area.
3) Updating Personal Best: Based on its judgment of fitness and present position, each particle upgrades its own best position. If the current position is better than the personal best position it has encountered so far, the personal best position is updated.
4) Updating Global Best: The global best position of the swarm, which represents the best solution found by any particle in the swarm, is updated based on the personal best positions of all particles.
5) Updating Velocity and Position: Based on its individual experience (personal best) and the collective experience of the swarm (global best), each particle modifies its position and velocity. Particles are able to efficiently search the search space because to this modification.
6) Termination: When a termination condition is satisfied, such reaching a maximum number of iterations or finding a workable solution, PSO ends.

PSO is often used to solve optimization problems in various fields such as engineering, economics, and machine learning. Its simplicity, efficiency, and ability to handle complex search spaces make it a popular choice for many optimization tasks. However, like any optimization algorithm, its performance can depend on parameter settings and problem characteristics

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C. Objectives

1) Design a schematic representation of a 2-stage CMOS op-amp circuit using LT Spice.
2) Apply PSO, to optimize the performance of the 2-stage CMOS op-amp circuit using MATLAB.
3) Address challenges inherent in op-amp design.
4) Obtain the best solution for the given design specifications.

D. Organization of Report

The work in this thesis is organized into five chapters including this chapter.
Chapter 2 comprises literature review associated to the project.
Chapter 3 comprises of the stages in designing and optimization three-stage CMOS op-amp using PSO algorithm.
Chapter 4 comprises of result obtained for the design and its analysis.Chapter 5 consists of conclusion and future scope of the work.

E. Conclusions

In this chapter, an overview of 2-stage CMOS op-amp and the fundamental concepts related to the PSO optimization algorithm is presented. The objectives of the project are formed and organization of the report is presented.

II. LITERATURE REVIEW

This chapter presents the literature survey of the various methodologies related to the project.

A. Circuit Design

Developing a low input offset voltage, 2-stage CMOS op-amp is the goal of [1]. In essence, an op-amp, consists of two distinct inputs as well as a single output. The difference between the applied signals from its two independent inputs is the output voltage signal of an op-amp. This suggests that the output will be voltage-free if there is no variation between the two inputs. The operational amplifier has evolved into a very useful and multipurpose tool as all signals in real life are inherently analog and require ADC and DAC. This study presents a unique approach to constructing a low offset voltage, two-stage CMOS operational amplifier. Using CEDENCE tools and appropriate requirements, the proposed model and the unmodified model have been simulated in 100nm CMOS process technology. The offset voltage of the op-amp has been considerably decreased following the adjustment, according to the results. Additionally, it has been discovered that the compensating capacitor significantly affects the performance of the op-amp; as a result, by choosing the ideal capacitance, we may enhance the op-amp's performance. When developing a high-performing two-stage CMOS op-amp, these findings can be important.
Any analog integrated circuit must have operational amplifiers, and enhancing their performance has a big impact on the overall design. A 2-stage, or differential amplifier followed by a common source amplifier, is one of the more elegant and space-efficient ways to create an operational amplifier [2]. The design of a 2-stage CMOS operational amplifier is presented. The traditional and widely used method of designing operational amplifiers has been the 2-stage op-amp structure. The 2-stage op-amp can perform on par with systems using cascode stages when it comes to resistive loads. Even though inherent gain and supply voltages are constrained in modern CMOS technology, a 2 stage op-amp construction can nevertheless provide a high gain and strong output swing. In 180 nm technology, a 2-stage CMOS operational amplifier has been built and simulated. A two stage CMOS op-amp can provide performance that is comparable to cascode or other sophisticated structured OP-amps when the Op-amp is driving a capacitive load. However, more area on the chip is needed for the frequency adjustment that the miller capacitor and resistor give.
Two-step settling is used in switching capacitor stages in analog to digital converters (ADCs). Charge pumps are used in the first phase of settling to apply charge to the load capacitance, and negative feedback is used in the second step to satisfy the settling criteria. Determining the ideal ratio of C_l/C_c and g_{m2}/g_{m1} is crucial [3]. Thus, the necessary settling time and accuracy may be determined while using the least amount of power. It is now necessary to construct entire analog-digital subsystems using the same technology on a single integrated circuit due to the recent and significant development in chip complexity. Because of this, it has become more and more crucial to implement analog functions in MOS technology. In recent years, significant progress has been made in the implementation of functions like instrumentation amplifiers, voltage references, high-speed digital audio converters, and sampled data analog filters in CMOS technology.
This work describes the two-stage CMOS operational amplifier's analysis and, comprising a rail-to-rail class AB output stage to maximize SNR ratio and a rail-to-rail gain-boosted folded cascode amplifier to increase speed and DC gain from 68 dB to 123 dB in the input stage [4]. With a 3.3 V power supply, the Cadence Spectre Circuit Simulator simulates 350nm CMOS technology.

With a 5 pF load, a minimal settling time of 22.3 ns, a high DC gain of 156 dB, a phase margin of 69 degrees, and a power consumption of less than 7 mW, this op-amp achieves more than 90 dB in PSRR. Several circuit topologies have been proposed in recent decade to enhance FC amplifiers in analog & digital circuit designs to get huge output signal swing and high gain. This may be done by utilizing cascode technology, which is frequently utilized in the design of two or more stages, to create a design with improved frequency response. It has been reported that certain op-amps in the AB class have modest CE and are capable of producing dynamic currents exceeding 100IB in their output stages. To reduce power consumption when operating in the sub-threshold area, each branch's current is set at a low value. This current therefore has an impact on the op-amp's slew rate.

Due to the reliability issue with small-size MOSFET semiconductors and the growing use of lightweight, long-lasting battery-operated handy electronic systems, low-voltage power sources for CMOS synchronised circuits are being used more frequently [5]. Microelectronics' rapid advancement in recent years has led to an increase in the number of applications that call for a super low sufficient signal estimate module, such as implantable devices used in biomedical applications to monitor a few Neuro-solid exercises. Examining the biological indicators of the human body is a very fascinating topic since it frequently yields important information about the body's wellbeing. These details enable medical professionals to evaluate illnesses. outcomes show that the suggested intensifier met each component of the advance plan in a successful manner. The ECG Checking Framework, a 2 stage functional enhancer created for low voltage and low power applications, is presented in this study. Applications requiring low power, low voltage, high CMRR, and high PSRR, including small battery-operated devices and biomedical instruments, are well suited for this two-stage enhancer with mill operator compensation. The circuit of a Phantom was created using 0.90um CMOS technology.

A two-stage CMOS operational amplifier's response to single event transients (SET) is examined in this research. Op-amp parameter study is carried out for technologies with wavelengths of 90 nm, 130 nm, and 180 nm [6]. The impacts of SETs have become important in these circuits because of deep submicron CMOS. As technology advances, more attention is being paid to these SETs, as seen by the transient analysis results. Almost all systems have linear components, which are crucial components. They include, among other things, voltage regulators, comparators, and amplifiers. Such components become very challenging to design analogically at submicron levels because of the sensitivity of the circuits and the trade-offs with different parameters. Reduced device size make the op-amps more susceptible to noise.

The design and analysis of 2-stage CMOS op-amp utilizing advanced 45 nm technology is presented [7]. The op-amp, a fundamental building block in analog integrated circuits, plays a crucial role in numerous applications, including signal processing and amplification. The design process involves a comprehensive exploration of circuit parameters, trade-offs, and optimization techniques to meet the desired performance specifications. The work begins with an analytical description of the 45 nm technology node, highlighting its significance in the era of miniaturization and integration. The paper delves into the systematic design process, encompassing transistor sizing, biasing, and load selection. With a significant voltage gain, the developed two-stage op-amp has proven that it can efficiently amplify weak signals. The op-amp's versatility for a range of high-gain applications is demonstrated by the DC gain exceeding the given target. The op-amp also has a large bandwidth, which allows it to handle signals across a wide range of frequencies. For applications requiring precise signal amplification across a range of frequency spectrums, this result is essential.

Operational amplifiers are mostly employed as feedback systems and have a high forward gain. However, a differential amplifier or a single stage op-amp cannot offer very high gain, so when very high gain is required, two stage op-amps are utilized. Therefore, there needs to be one more component after the differential amplifier in order to boost the gain. With a bias current of 50 uA and a 1.8 V dc supply, this amplifier generates a gain of over 66 dB and an extremely high slew rate of 95 V/us [8]. The gain can increase with a drop in current, but the slew rate will also decrease, affecting the amplifier's sensitivity. As a result, the design of a high slew rate amplifier incorporates high gain and low power consumption. Measured are the several parameters, including phase margin, power consumption, and gain bandwidth product.

B. Design Optimization

The 2-stage CMOS op-amp redesign process with the lowest phase margin and frequency response inaccuracy is presented in this research [9]. The suggested proposal follows the design procedure for a two-stage operational amplifier. Cadence simulation results are provided to demonstrate the effectiveness of the suggested redesign procedure phases. In AMS 0.35 μm CMOS technology, the suggested designing process for a two-stage CMOS op amp is put into practice.

According to the simulation findings, the phase margin is 60.36 with a 0.6% error and the frequency response is 5.7 MHz with a -5.83% error in a power supply of ±2.5 V. The design process has the least amount of phase margin and frequency response error when compared to earlier efforts.

A Flash ADC converter with a 3-bit resolution is implemented in LTspice with 180nm technology, the resistive ladder network, comparators, thermometer, and binary encoder comprise the suggested Flash ADC [10]. 1.8 V is the reference voltage that is used on the resistive ladder network. In the flash analog to digital converter a 2-stage operational amplifier serves as a comparator. A priority encoder is used to convert the thermometer code into binary code. The main issue with flash ADCs often arises from the fact that as resolution bits grow, so does the area and circuit power consumption. The fast advancement of science and technology has led to a significant increase in the field of digital signal processing. In most digital domains, signal processing provides several benefits, including high accuracy, reduced silicon area, programmability flexibility, faster and more cost-effective design processes, and the ability to design systems with high speed and less area. ADC's average power and conversion time, among other parameters, are computed and contrasted.

In almost all electrical systems, one of the most often used components is the operational amplifier. Therefore, it is always crucial to create a good op-amp since it offers several benefits. For certain applications in fields like communication, a lot of research has been done to reach a reliable level of a design that deals with high speed, low power consumption, and lower slew rates. Modern communication needs to be much more immune to the effects of noise, have a much larger bandwidth, and consume less power. However, creating an op-amp that is ideal, is a difficult task. The most common observation is that power needs and bandwidth are traded off. This work presents a novel design for a low power, two-stage operational amplifier using a Miller compensated topology to increase stability [11]. Tanner EDA tool is used to design and simulate the circuit utilizing 45 nm CMOS technology. With a good phase margin, a notable power decrease and improvement of unity gain BW are obtained. A number of parameters are calculated and contrasted with a few recent works in order to determine the design's effectiveness.

The group intelligence bionic optimization algorithm known as Particle Swarm Optimization was first proposed by Kennedy and Eberhart in 1995. The standard PSO optimization process works under the assumption that there is a flock of birds randomly distributed in an n-dimensional space, known as the particle swarm, with each bird representing a particle and having its own spatial position and flight speed. Among the benefits of PSO, swarm intelligence algorithm is its straightforward algorithmic concept, its easily programmable parameters, and its ease of use [12]. Many academics have successfully addressed linear problems, nonlinear difficulties, multiple- objective optimization problems, and other challenges by applying PSO to a variety of domains. Nevertheless, the algorithm also has evident issues with problem solving, including a slow convergence speed, premature maturity, early local optimization, and other issues that result in a slow convergence speed, poor search accuracy for the optimal value, and an unsatisfactory optimization effect.

The PSO technique has gained increased traction in recent times. In the majority of cases, it has been demonstrated to be an efficient optimization technique [13]. In order to maximize outcomes, we improved the PSO parameters after applying the PSO method to a sample Artificial Neural Network (ANN) application and measuring the improvement. English number character recognition is the application. Two metrics related to processing time and result correctness are considered. This research aims to demonstrate that PSO may be optimized for optimal outcomes by experimentally adjusting its parameters. To demonstrate the impact of PSO in an ANN application, we employed a two-stage methodology. Initially, we trained a supervised Multilayer Perceptron (MLP) Artificial Neural Network to detect English numerals. The network was initialized with homogeneous randomly generated weights, and the results were recorded. The PSO method was then included to supply the network with optimum weights, and the results were once more run and recorded.

One of the most pressing issues in operating an interconnected power system is Reactive Power Planning (RPP) [14]. To get the best reactive power planning solution, the study effort funded by this article uses the population-based optimization technique of Standard Particle Swarm Optimization (STD-PSO). Three PSO technique modifications are covered in the proposed work: Fixed Inertia Weight PSO (FIW-PSO), Linearly Decreasing Weight PSO (LDW-PSO), and a hybrid Grey Wolf Optimization with PSO (GWO-PSO) technique. These variations are intended to improve performance by effectively controlling the local search and pushing the algorithm towards global optimization. Effective reactive power source planning is critical to the safe and efficient functioning of the power network. Increased power demand, irregular power flow, and restrictions on transmission line expansion are the main causes of increased transmission loss and power line congestion in the contemporary interconnected power network environment. Reactive power control and planning are therefore vital to maintaining efficient power system functioning and restoring stability margins to previously existent circuits.

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The Inverse Kinematic (IK) problem for redundant serial manipulator robots has been solved in this study using the PSO technique. The study's novel approach is to take the joints' varying continuity into account [15]. Due to the identification of this issue, the robots' Inverse Kinematic problem-solving method has greatly improved in terms of accuracy, Execution Time (ET), Standard Deviation (SD), and iterations required by using the optimum algorithm. The 5-Degree of Freedom 5R robot model's Inverse Kinematic issue has been solved using the approach. Using PSO, the IK for five DOF-serial manipulator robots were resolved in this study. In three distinct scenarios, the robot was maneuvered in the three-dimensional workspace using a spiral route. In the first instance, the route yielded 100 equidistant continuous points, and the PSO was able to resolve the issue. The trajectories were formed by 100 randomly selected and equally spaced points in the second and third cases, respectively.

Despite demonstrating strong optimization performance, the original PSO still has a serious problem with premature convergence [16]. Because of this, several researchers have been altering it, producing a vast variety of PSO variations that perform marginally better or noticeably better. The basic PSO has primarily been altered through the use of four primary strategies: collaboration, multi-swarm approaches, hybridizing PSO with other well-known meta heuristic algorithms like Differential Evolution (DE) and Genetic Algorithm (GA), and altering the PSO governing parameters. This study aims to give a thorough overview of PSO, including its fundamental ideas, binary PSO, neighbourhood topologies, historical and contemporary PSO variations, and notable engineering applications. Primary goal is to provide an extensive overview of PSO, including binary and continuous PSO, various PSO topologies, Hybrid PSO variants, and PSO variations. It also discusses the applications of partial swarm optimization variants in optimization issues. This review article is primarily concerned with PSO-based feature selection. To the best of the authors' knowledge, no book exists that provides a thorough overview of the most recent advancements in PSO variants and the application of PSO to feature selection issues.

C. Fitness Evaluation

A PSO-based notion for optimizing nonlinear functions is presented. A few paradigms are described together with their evolutionary history and a discussion of one paradigm's application [17]. Applications such as paradigm's benchmark testing is described, along with recommendations for neural network training and nonlinear function optimization. The article describes the connections between genetic algorithms and artificial life as well as particle swarm optimization. A technique for optimizing continuous nonlinear functions is presented in this study. The algorithm lacks metaphorical backing, however the social metaphor is explored because the approach was found by simulating a basic social model. This study provides an overview of the evolution of the particle swarm optimization idea from social simulation to optimizer, describing it in terms of its forerunners.

PSO uses the memory of the particle and swims to find the global optimum solution. Due to its minimal constraints on the objective function and joint search space continuity, as well as its capacity to adjust to changing conditions, PSO has emerged as one of the most significant algorithms for evolutionary computation and swam intelligence. The progress on algorithm enhancement over the previous few years is then reviewed, along with applications in fields including neural networks, electronics, and multi-objective optimization [18]. Several future directions for PSO research are mentioned along with the issues that still need to be handled. By rearranging the particles in the solution space, the algorithm finds the best solution. Researchers are becoming more interested in PSO due to its ease of realization and potential for optimization in a wide range of issues. Two aspects are the main emphasis of most works. The first is the enhancement of PSO performance by parameter adjustments, population diversification, and hybridization with other optimum strategies.

The enhanced PSO to choose a route for electric power communication; incorporate the discrete concept and random inertia weight into the routing scheme is presented [19]. Additionally, a real-world example is provided to demonstrate the viability and effectiveness of PSO in resolving routing issues related to power communication.

The fast progress of information technology has led to continued growth in the field of education, and in particular, in remote e-learning. A component of open pedagogy is the movement to remove financial and geographic obstacles from everyone's access to high-quality education [20]. In this study, we propose a particle swarm optimization (PSO) based adaptive learning technique. The algorithm determines the characteristics of the learners by looking at the traces that they leave on e-learning platforms, forums, and social networks. Primary goal is to raise the retention rate by giving every learner the support they require.

D. Conclusions

This Chapter provides a review of the literature on the many approaches used in the project.

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III. DESIGN AND OPTIMIZATION OF 2-STAGE OP-AMP

The PSO is used to construct and optimize a 2-stage op-amp. The PSO technique is implemented in Section 3.2, while Section 3.3 uses LTSpice and MATLAB to simulate a 2-stage CMOS op-amp circuit.

A. Design of 2-Stage CMOS Op-Amp

Designing a 2-stage op-amp involves a systematic process aimed at achieving desired performance metrics while considering various design constraints. The process typically begins with defining the specifications and requirements of the op-amp circuit, including Gain, Bandwidth, Phase Margin, power consumption, and area.

The performance metrics that are examined are gain, unity gain-bandwidth, phase margin, slew rate, power dissipation, and area as given in equations from 1 to 6. These metrics are extracted from [7] [20]:

1) Gain: In a two-stage op-amp, the ratio of the output voltage to the input voltage is vital to take into account. This includes both the open-loop gain and the closed-loop gain (with feedback).

$$A_v = (g_{m1} / (g_{d2}+g_{ds4})) (g_{m6} / (g_{ds7}+g_{ds6})) \quad (3.1.1)$$

2) The frequency at which the op-amp's open-loop gain reaches unity (1), or 0 dB, is known as the unity-gain bandwidth.

$$GBW = g_{m1}/C_c \quad (3.1.2)$$

where C_c is the compensation capacitor.

3) Phase margin: Phase margin monitors the stability of the op-amp and specifies the amount of phase shift margin before the circuit becomes unstable. It is vital for preventing oscillations and guaranteeing dependable operation.

$$PM = \pm 180 - \tan^{-1}(GBW/p_1) - \tan^{-1}(GBW/p_2) - \tan^{-1}(GBW/z)w \quad (3.1.3)$$

4) Slew rate: The highest possible rate of change of the output voltage per unit of time is referred to as the slew rate. It determines the op-amp's ability to respond to fast input signal changes without distortion

$$SR = I_5/C_c \quad (4)$$

5) Power dissipation: Minimizing power is important for cost-effective designs.

$$P = (V_{DD}-V_{SS}) (I_5+2I_7) \quad (5)$$

6) Area: Refers to the physical size occupied by the op-amp circuit on the IC chip. Minimizing area is important for cost-effective manufacturing and integration with other circuitry.

$$Area = \sum^{n} i=1 \; W \quad *Li \quad (6)$$

The nonlinear equations of design cannot be solved analytically or in a systematic manner. Thus, multi-objective optimization will be utilized in conjunction with automation to attain optimal outcomes. The matched devices of the 2-stage op-amp basic differential amplifier design are M1 & M2, M3 & M4, and M5 & M8. The recommended PSO programming generates at random the set of starting values for circuit design or dimensions, within a specific range required by the area requirements.

B. PSO Algorithm

The PSO algorithm is a nature-inspired optimization technique used to find the optimal solution for a given problem. It mimics the social behavior of birds flocking or fish schooling. In PSO, a population of candidate solutions, called particles, move through the search space. Each particle adjusts its position according to its own experience and the experiences of neighboring particles. This adjustment is based on the principle of "attraction" towards the best-known position found by the particle itself and the best-known position found by any particle in the swarm. PSO is commonly used in optimization problems where traditional methods are inefficient, such as in engineering design, data mining, and machine learning

Among the swarm-based techniques that are most highly recognized in the literature is PSO. The basic PSO has primarily been altered through the use of four primary strategies: cooperation and multi-swarm approaches, hybridizing PSO with other well-known meta-heuristic algorithms like Differential Evolution (DE) and Genetic Algorithm (GA), and altering the PSO governing parameters.

Kennedy and Eberhart, first introduced the PSO as a continuous real-valued algorithm. This variation is referred to as the standard PSO (SPSO) in this study. In SPSO, a swarm of particles explores a D-dimensional search space in pursuit of the optimal solution.

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There is a vector of current velocity for each particle i. $Pbest_i = [Pbest_{i1}, Pbest_{i2},..., Pbest_{iD}]$ and a current position vector $X_i = [x_{i1}, x_{i2},..., x_{iD}]$ represent the best location determined by particle i and the optimal position determined by the whole swarm. Particle i is guided by $Gbest = [Gbest_1, Gbest_2,..., Gbest_D]$ to update its location and velocity.

Standard PSO:

$v_{id}\ (t + 1) = v_{id}\ (t) + c_1r_1\ (Pbest_{id}\ (t) - x_{id}\ (t)) + c_2r_2\ (Gbest_d\ (t) - x_{id}\ (t))$

$x_{id}\ (t + 1) = x_{id}\ (t) + v_{id}\ (t + 1)$

where r_1 and r_2 are two uniform random variables created inside the [0, 1] interval, and c_1 and c_2 are the cognitive and social acceleration coefficients. Algorithm displays the pseudo-code of the SPSO.

The SPSO Algorithm's Pseudo-Code:

1: Initialization
2: Define the swarm size S and the number of dimensions D
3: for each particle i ∈ [1..S]
4: Randomly generate X_i and V_i , and evaluate the fitness of X_i denoting it as f (X_i)
5: Set $Pbest_i = X_i$ and f ($Pbest_i$) = f (X_i)
6: end for
7: Set $Gbest = Pbest_1$ and f (Gbest) = f ($Pbest_1$)
8: for each particle i ∈ [1..S]
9: if f ($Pbest_i$) < f (Gbest) then
10: f (Gbest) = f ($Pbest_i$)
11: end if
12: end for
13: while t < maximum number of iterations
14: for each particle i ∈ [1..S]
15: Evaluate its velocity v_{id} (t + 1) using Equation (1)
16: Update the position x_{id} (t + 1) of the particle using Equation (2)
17: if f (x_i (t + 1)) < f ($Pbest_i$) then
18: $Pbest_i = x_i$ (t + 1)
19: f ($Pbest_i$) = f (x_i (t + 1)
20: end if
21: if f ($Pbest_i$) < f (Gbest) then
22: $Gbest = Pbest_i$
23: f (Gbest) = f ($Pbest_i$)
24: end if
25: end for
26: t = t + 1
27: end while
28: return Gbest

Hybridization, as used within the meta-heuristics domain, is the process of combining the best features of 2 different algorithms that can solve the same issue to create a new algorithm that performs better than each method alone.

The flow-chart for the proposed design optimization of the 2-stage op-amp is as shown in fig. 3.2.

C. Circuit of 2- stage CMOS op-amp

LTSpice was used as the simulation tool in the experimental setup to simulate the CMOS op- amp circuit. LTSpice's schematic editor was used to build the circuit schematic, which includes biasing networks, capacitors and CMOS transistors.

Parasitic effects were not taken into account when modeling capacitors as perfect components. The simulation parameters were set up to perform transient analysis, AC small-signal analysis, and DC operating point analysis. These investigations shed light on the op-amp circuit's frequency-domain properties, transient response, and DC biasing conditions. The circuit design of 2-stage op-amp is represented in Fig. 3.3

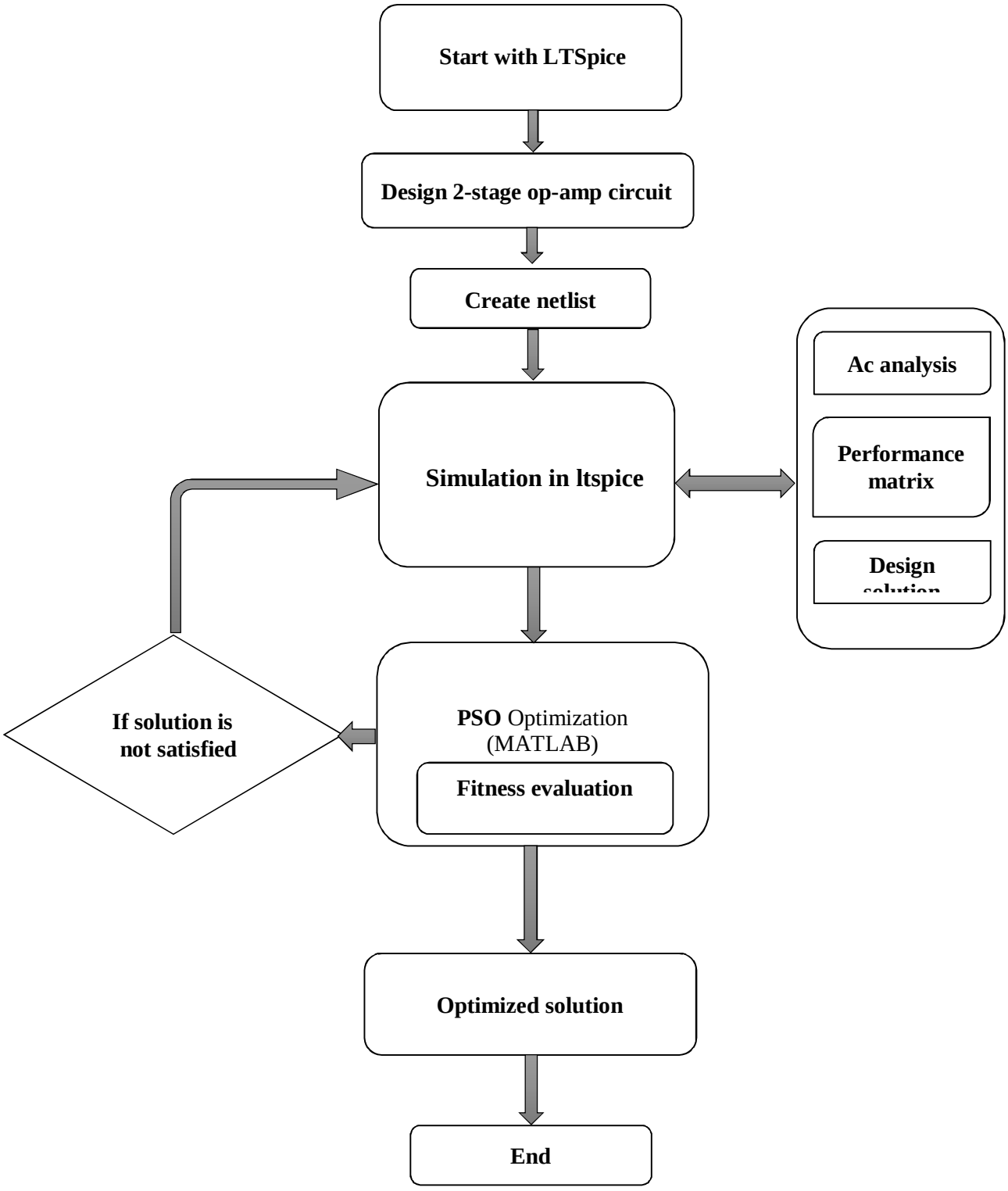


Figure 3.3.1 : Flowchart of design automation of 2 stage op-amp.

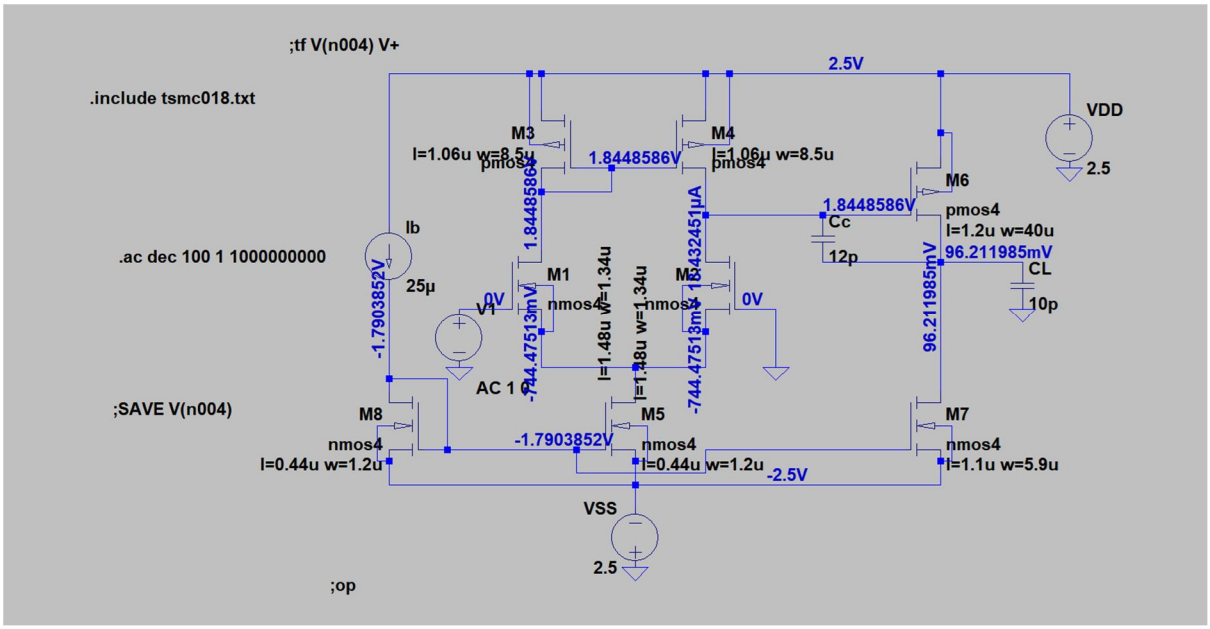


Figure 3.3.2 : Schematic of 2-stage operational amplifier

W[1]	L[1]	W[3]	L[3]	W[5]	L[5]	W[6]	L[6]	W[7]	L[7]	I_b	C_c

Figure 3.3.3 : 2-stage op-amp solution vector for PSO programming.

The design goals are to minimize power and area while maximizing Gain(G), Phase Margin(PM), unity- gain bandwidth(UGBW) and Slew Rate. During the design phase, the ideal solution vector is calculated, consisting of the width and length of the op-amp devices M1 through M8, along with its bias current Ib and compensating capacitor Cc. A used solution vector for the suggested PSO programming is shown in Fig. 3.3.1

It is anticipated that the matched devices of the basic differential amplifier configuration of the 2-stage op-amp are M1 - M2, M3 - M4, and so on since the current mirror is M5 - M8. After that, a SPICE simulation is run on the PSO-produced design to get the necessary performance data. These performance metrics are therefore seen by the PSO as prerequisites for the second design iteration, which will be evaluated by SPICE simulations. As shown in Fig. 3.3.2, the optimization process by PSO and verification by SPICE are therefore carried out iteratively in a loop for the specified number of generations in order to generate the final optimum design solution.

Without requiring temporary files, basic data transfer interfaces between the MATLAB and SPICE platforms are developed. First, a MATLAB file is used to construct a circuit netlist file. After that, MATLAB starts SPICE and uses a DOS batch file to run the circuit netlist file in the SPICE environment. After the initial iteration, performance measures are assessed by parsing the output files produced by SPICE using MATLAB methods. These measures serve as a reference for the design creation of PSO programming that follows. A bidirectional data transfer link between the SPICE and MATLAB platforms is constructed in order to produce an integrated PSO-SPICE architecture.

Real valued numbers are utilized to encode solution vector. The fitness value of every solution indicates how optimal it is. Every solution vector is smoothly integrated into the LTSpice netlist and then simulated in order to calculate the fitness. The performance measurements are taken from the SPICE waveform data file and log file, and the fitness value of the solution vector is calculated using a weighted method [21]. Fitness evaluation is thus performed at each iteration of PSO programming by communicating the actual performance measurements generated by SPICE to the MATLAB environment and comparing them to the desired metrics.

After the mutation, LTSpice simulations are performed using the newly adjusted parameters to evaluate the circuit's performance. A fitness function use a range of circuit performance measures, such as gain, phase margin, bandwidth, and power consumption, to assess the revised solution's fitness.

If the revised response performs better than the initial one, the solution is adjusted accordingly. This iterative process continues until a termination criteria is met, such as reaching a limit number of iterations or achieving the desired performance improvement.

IV. RESULTS AND DISCUSSION

This chapter presents the implementation results of the proposed optimization. The optimal design solutions and simulation results of the 2-stage CMOS op-amp is presented.

Table 4.1 lists the lower and upper bounds of the device dimensions that were taken into consideration, along with the final design solution produced by the integrated PSO-SPICE based framework for two design specifications after 50 generations. Intel i7 13th gen i7-1355U 1.70 GHz processor-based system, which is reasonable.

Table 4.1: Dimension of the ideal design transition solution

ameter(µm)	Lower bound	Upper bound	PSO-SPICE Design	
			PSO (1)	PSO (2)
W[1]	1	12	1.34	1.34
L[1]	0.18	2	1.48	1.48
W[2]	1	12	1.34	1.34
L[2]	0.18	2	1.48	1.48
W[3]	2.52	28	8.5	8.4
L[3]	0.18	2	1.06	1.09
W[4]	2.52	28	8.5	8.4
L[4]	0.18	2	1.06	1.09
W[5]	2.16	24	1.2	1.9
L[5]	0.18	2	0.44	0.25
W[6]	32	360	40	20
L[6]	0.18	2	1.2	1.2
W[7]	13.5	150	5.9	6.5
L[7]	0.18	2	1.1	1.2
W[8]	2.16	24	1.2	1.9
L[8]	0.18	2	0.44	0.25
I_b (uA)	15	30	25	24.8
C_c (pF)	0.22* C_1	3	12	12.3

Table 4.2: Results of integrated PSO-SPICE

Performance Metrics	Design Specification-1	PSO SPICE Design Result	Design Specification-2	PSO SPICE DesignResult	[21]
		PSO-1		PSO-2	
Open-loop DC Gain(dB)	65	73.71	70	71.87	76.31

Unity-Gain Bandwidth (MHz)	1	1.013	2	1.003	11.65
gin (^{o})	≥65	72.42	≥60	60.5°	68.78
(V/µs)	1	1.41	1	1.21	9.83
Power Dissipation(mW)	Min	0.188	Min	0.213	0.166
)	Min	77.52	Min	125.21	262

The 2-stage op-amp performance metrics that were derived from the suggested designs are listed in Table 4.2 and fairly contrasted with the simulation findings that were published in study [21]. The design is focused on minimizing power dissipation, maximizing phase margin which results in better stable circuit, and designed for low frequency measurement and instrumentation applications, rest of the performance metrics are fairly better than the given designs.

The frequency responses of the PSO-1 and PSO-2 designs are shown in Figure. 4.1 and Figure. 4.2. The PSO-SPICE integration allows for the smooth transfer of design variables and performance metrics between SPICE and PSO, making it easier to evaluate fitness on precise SPICE-generated performance measurements, for every iteration, without experiencing any de-rating from PSO.

Conclusions

In this chapter, implementation results of the proposed PSO algorithm with MATLAB and LTSpice are discussed. Simulation and Synthesis performed using MATLAB. Frequency response of 2-stage op-amp is generated and the comparative results are tabulated.

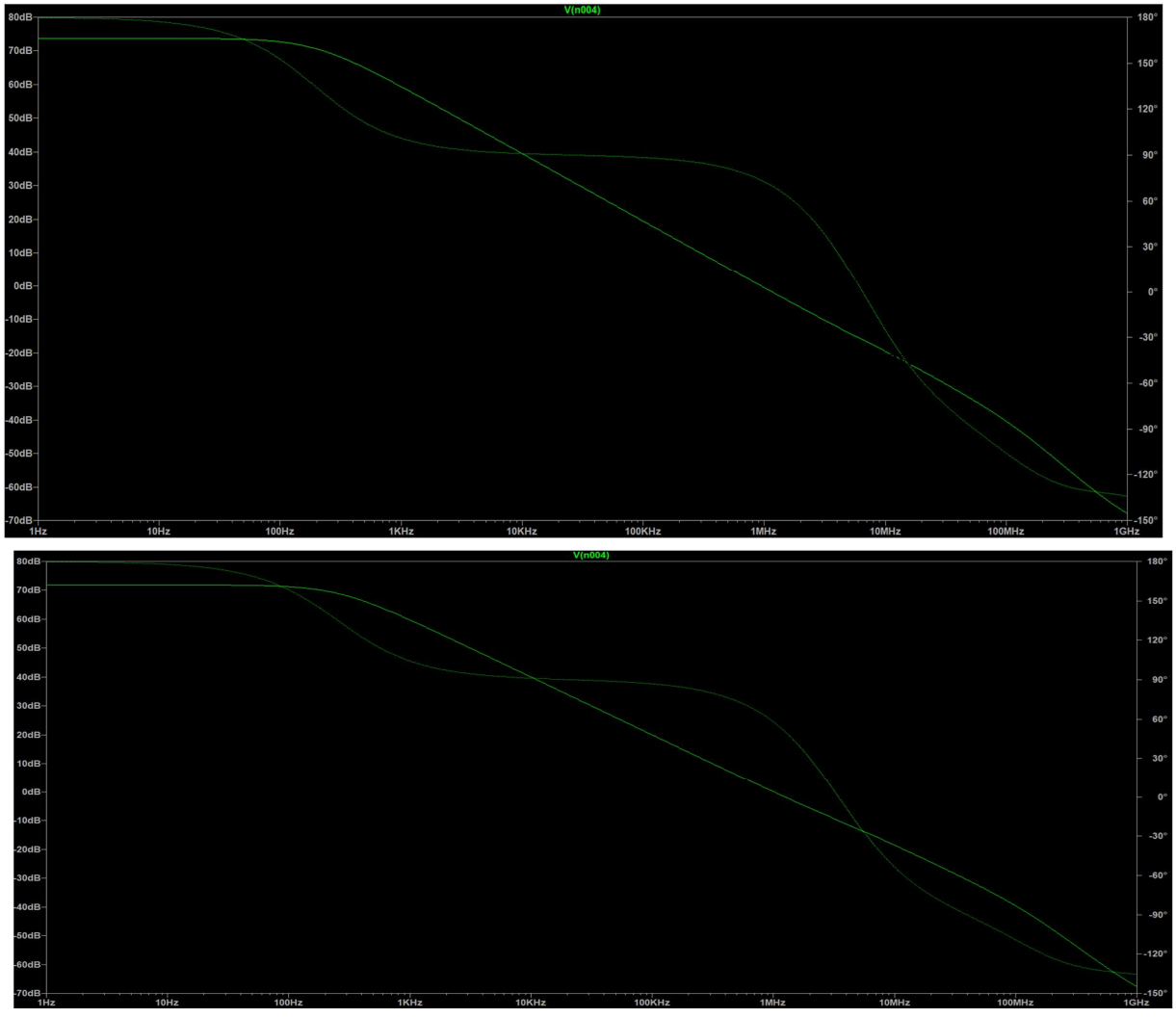


Figure 4.2 : Frequency response of 2-stage op-amp from PSO-SPICE framework of PSO -2.

V. CONCLUSIONS AND FUTUREWORK

A. Conclusion

The objective of the proposed study is to design and optimize analog circuits using the PSO algorithm, demonstrated through a 2-stage op-amp. Commencing with a comprehensive specification analysis, we established the design constraints of the 2-stage op-amp to fulfill the desired specifications. Utilizing the Particle Swarm Optimization (PSO) algorithm, we conducted the optimization process, focusing on parameters such as gain, bandwidth, and power consumption to refine the op-amp design. With MATLAB's PSO programming, the design process is executed and continually verified through SPICE simulations. Utilizing precise SPICE-generated performance data for suitability evaluation ensures the optimization process's accuracy and robustness at every iteration. There are no de-ratings due to PSO procedures. Consequently, the integrated PSO-SPICE framework presents a scalable and dependable technique applicable to optimize analog circuits of varying sizes and complexities. Furthermore, the optimization method facilitates exploring design trade-offs, enhancing performance metrics. Convergence towards an optimized design is evident through numerical data and convergence criteria, underscoring the effectiveness of the PSO algorithm in op-amp optimization. This methodology represents an advancement in analog circuit design and optimization by leveraging advanced PSO approaches.

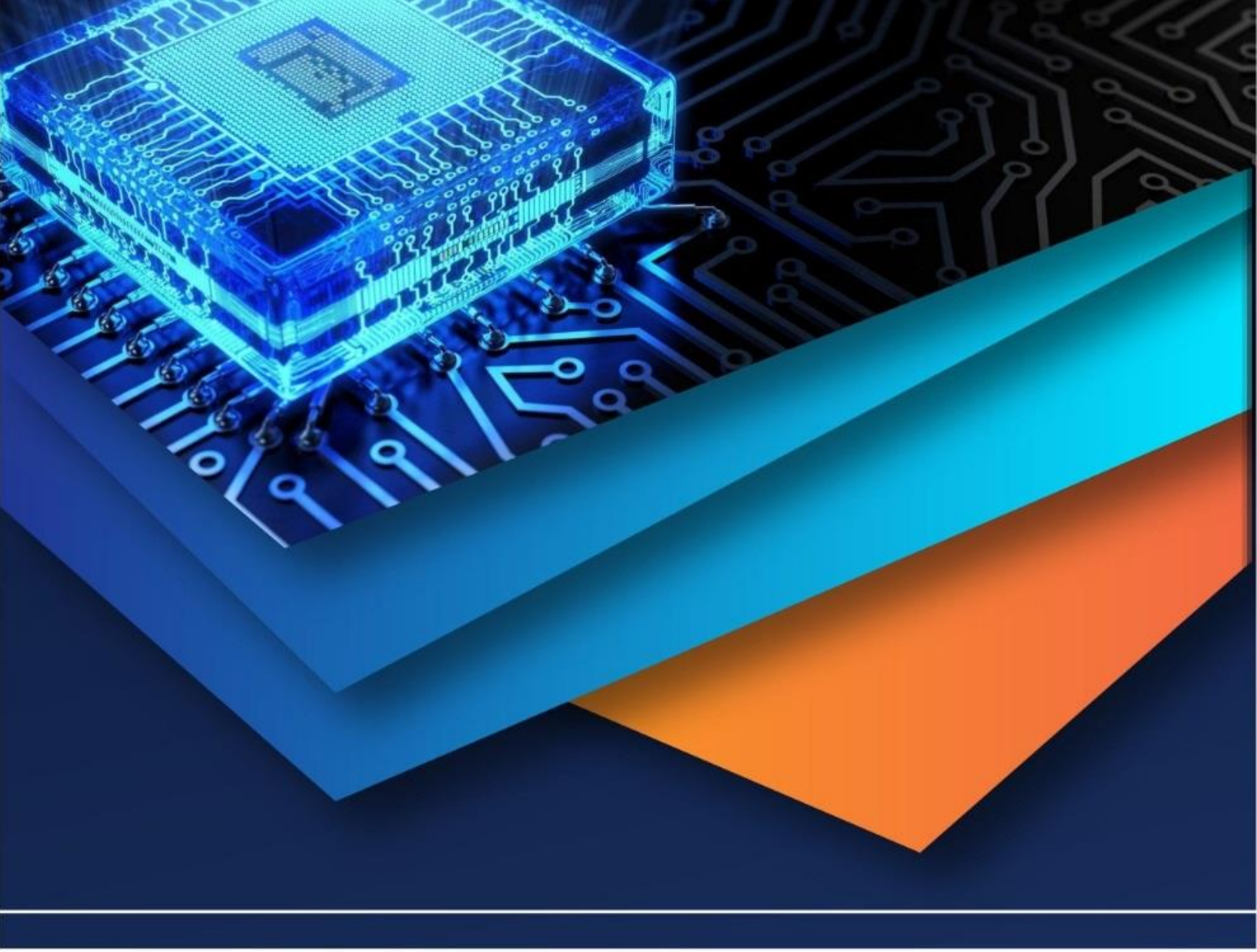
B. Future work

It's important to understand the limitations of our research, particularly the assumptions made about the optimization process and the model simplifications. To get over these restrictions and enhance the op-amp design even further, future research might look at other optimization techniques or expand the scope to encompass more types of circuits. More improvements in op-amp performance might be achieved by investigating the combination of state-of-the-art manufacturing methods and novel materials.

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