iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 11 **Issue:** V **Month of publication:** May 2023

DOI: https://doi.org/10.22214/ijraset.2023.52541

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 11 Issue V May 2023- Available at www.ijraset.com

Design of BCD Adder Using QCA Technology

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Abstract: ***Quantum-dot Cellular Automata (QCA) technology is a promising alternative to traditional complementary metal-oxide-semiconductor (CMOS) technology for implementing digital circuits due to its potential for high speed, low power consumption, and small size. In this paper, we present a design for a Binary Coded Decimal (BCD) adder using QCA technology. The BCD adder is a crucial building block for arithmetic operations in decimal representation. The proposed design uses QCA cells to perform the addition operation of two BCD digits, which are encoded as a 4-bit binary number. The design includes a full-adder circuit, a BCD-to-binary converter, and a carry-lookahead adder. Simulation results using QCA Designer software demonstrate the functionality and feasibility of the proposed BCD adder design. The proposed design provides a promising alternative to traditional CMOS-based BCD adders and can contribute to the development of QCA-based digital circuits.***

Keywords: ***QCA (Quantum-dot Cellular Automata), QCA cell, One bit BCD adder, power, area, faster.***

I. INTRODUCTION

Quantum-dot Cellular Automata (QCA) is a novel nano electronic technology that has the potential to revolutionize the field of digital electronics. QCA is based on the principle of quantum mechanics and uses the interaction between quantum dots to perform logic operations. Unlike traditional complementary metal-oxide-semiconductor (CMOS) technology, QCA does not rely on the flow of electrons to perform computations. Instead, it uses the Coulombic interaction between adjacent quantum dots to encode and process information. The potential benefits of QCA technology include ultra-low power consumption, high speed, and extremely small device size. QCA circuits can operate at room temperature and can potentially achieve clock speeds beyond the limits of CMOS technology. The small size of QCA devices also means that they can be densely packed, enabling the creation of highly complex circuits on a single chip. Despite the promising potential of QCA technology, there are still several challenges that need to be addressed. One of the main challenges is the difficulty of manufacturing QCA devices and circuits using current fabrication techniques. Additionally, there are still many unanswered questions about the behavior and reliability of QCA circuits. In this context, research efforts are focused on developing efficient QCA-based circuits and addressing the challenges associated with the technology. QCA technology has the potential to drive the next generation of digital electronics and could be an important player in the field of nanoelectronics.

A. QCA Cell

QCA (Quantum-dot Cellular Automata) cell is a fundamental building block in QCA technology, which is a promising alternative to conventional CMOS technology for designing nanoscale digital circuits. QCA cells are used to implement logic functions and interconnect components in QCA-based circuits. A QCA cell typically consists of a small number of quantum dots arranged in a specific geometric pattern. Quantum dots are nanoscale structures that can confine electrons to discrete energy levels. In QCA, the position of electrons in the quantum dots represents the logical states of 0 and 1. The basic principle behind QCA cells is electron tunneling, which allows electrons to move between adjacent quantum dots. The movement of electrons is influenced by the electrostatic interaction between the quantum dots. This interaction is based on the Coulombic repulsion between like charges and attraction between opposite charges. The specific geometry and arrangement of quantum dots in a QCA cell determine its functionality. Different QCA cell designs exist, such as the majority gate, inverter gate, and others.

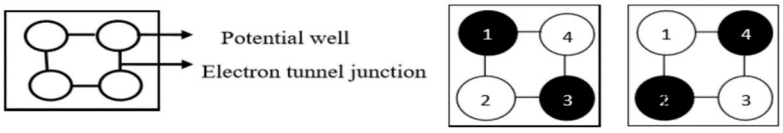


Fig 1: QCA Cell

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Volume 11 Issue V May 2023- Available at www.ijraset.com

B. QCA Wire

In Quantum-dot Cellular Automata (QCA), wires play a crucial role in transmitting and propagating signals between QCA cells or gates. QCA wires are designed to carry information in the form of electron polarization, which represents binary states (0 and 1) in the QCA technology.QCA wires are typically composed of a series of quantum dots arranged in a specific pattern. Quantum dots are nanoscale semiconductor regions that can confine a small number of electrons, allowing for discrete energy levels and precise control over their behavior. In QCA, these quantum dots are used to manipulate and control electron positions to encode information. The wire layout in QCA is designed to ensure proper signal propagation and minimize signal interference or crosstalk. QCA wires need to be placed close to QCA cells or gates to enable efficient interaction between neighboring cells. To transmit a signal along a QCA wire, the quantum dots within the wire are polarized in a specific configuration. The polarization of the electrons determines the binary value being conveyed (0 or 1). By carefully arranging the polarization of the quantum dots, the information can be propagated through the wire to the neighboring QCA cells. Overall, QCA wires in QCA technology serve as the conduits for carrying and transmitting information using the polarization of electrons in quantum dots. They play a critical role in enabling signal propagation and computation within QCA circuits.

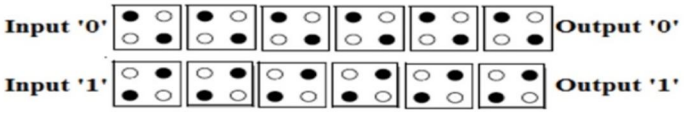


Fig 2: QCA Wire

C. QCA Inverter Gate

The inverter gate is a fundamental building block in QCA technology, used to invert the logical state of a signal. It plays a crucial role in implementing various digital logic circuits. In QCA, information is encoded using the position and alignment of electrons within quantum dots, which act as nanoscale "cells" or "dots." These dots are arranged in a regular grid, and the electrons can tunnel between neighboring dots based on their alignment. The QCA inverter gate consists of four quantum dots arranged in a square configuration. Two input dots are positioned diagonally opposite, while two output dots are placed at the other pair of diagonally opposite corners. The configuration ensures that the output dots exhibit the opposite electron alignment compared to the input dots. The QCA inverter gate has several advantages, including its small footprint, low power consumption, and high-speed operation. It forms the basis for constructing more complex QCA circuits and can be combined with other QCA gates to implement various logic functions, such as AND, OR, and XOR gates, for designing larger digital systems.

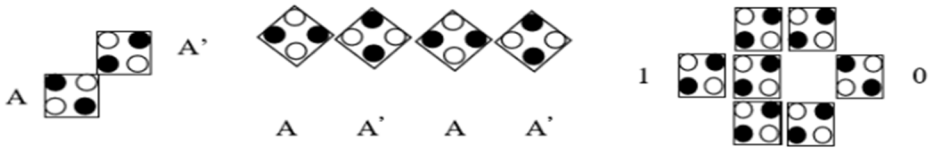


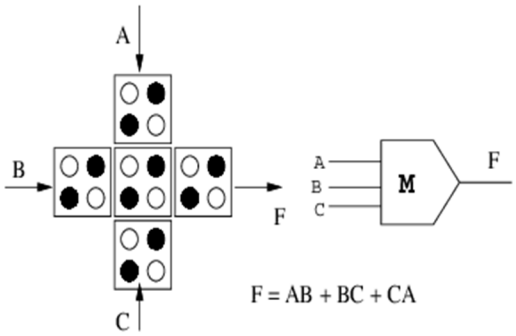
Fig 3: QCA inverter

D. QCA Majority Gate

The majority gate is a fundamental logic gate used in QCA technology for performing logic operations. It is based on the principle of electron localization and relies on the interaction between quantum dots to implement Boolean functions. The majority gate takes three input signals (A, B, and C) and produces an output signal (F) based on the majority of the input values. The output signal is determined by the state of the majority of the input signals. If the majority of the inputs are set to a "1" (logic high), the output will be set to "1"; otherwise, the output will be set to "0" (logic low).The functionality of a QCA majority gate is achieved through the interaction of electrons in the quantum dots. In a majority gate, three quantum dots are arranged in a triangular configuration, with each dot representing one input signal. The presence or absence of an electron in each dot corresponds to the logic values "1" and "0", respectively. When electrons interact within the quantum dots, they experience Coulomb repulsion, causing them to arrange themselves in a stable state. The arrangement of electrons determines the output of the majority gate. If two or more dots contain electrons, the repulsive forces between them cancel each other out, resulting in a stable state and producing a logic high output. Conversely, if one or fewer dots contain electrons, the output is logic low.

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A	B	C	F	
0	0	0	0	
0	0	1	0	
0	1	0	0	AND Logic A fixed to 0
0	1	1	1	
1	0	0	0	
1	0	1	1	OR logic A fixed to 1
1	1	0	1	
1	1	1	1	

Fig 4: QCA Majority Gate

II. LITERATURE SURVEY

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of processor, where they are used to calculate addresses, table indices, and similar operations. Although adders can be constructed for many numerical representations, such as binary-coded, decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used torepresent negative numbers, it is trivial to modify an adder into an adder– subtractor. Other signed number representations require a more complex adder. Adders are fundamental circuits for most digital systems and several adder designs in QCA have been proposed, and a performance comparison was improved. Better adder performance depends on minimizing the carry propagation delay and reducing the area. In 1993, Lent et al. proposed a physical implementation of an automaton using quantum dot cells. The automatonquickly gained popularity and it was first fabricated in 1997. Lent combined the discrete nature of both cellular automata and quantum mechanics, to create nanoscale devices capable of performing computation at very high switching speeds and consuming extremely small amounts of electrical power. Today, standard solid state QCA cell design considers the distance between quantum dots to be about 20 nm, and a distance between cells of about 60 nm. Quantum dot Cellular Automata are based on the simple interaction rules between cells placed on a grid. A QCA cell is constructed from four quantum dots arranged in a square pattern. These quantum dots are sites electrons can occupy by tunneling to them. Because of Coulombic repulsion, the two electrons will always reside in opposite corners. The locations of the electrons in the cell (also named polarizations P) determine two possible stable states that can be associated to the binary states 1 and 0. Although adjacent cells interact through electrostatic forces and tend to align their polarizations, QCA cells do not have intrinsic data flow directionality. The basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. The physical mechanism for interaction between dots is the Coulomb interaction and the quantum-mechanical tunneling. Electrons are able to tunnel between the dots, but they cannot leave the cell. If two mobile electrons are placed in the cell.

III. METHODOLOGY AND METHODS

A. Methodology

The main objective of this paper is to design a reversible BCD arithmetic circuit that can perform both BCD addition and subtraction using a minimal number of garbage gates and constant inputs. The proposed circuit introduces two optimized gates that overcome the limitations of existing reversible gates mentioned in the literature. The new gates offer improved performance in terms of the number of garbage outputs and constant inputs. BCD, or Binary Coded Decimal, is a number system that represents decimal numbers using binary digits. It uses four binary digits to represent each decimal digit, ranging from 0000 to 1001 for the decimal numbers 0 to 9, respectively. In the proposed design, the circuit can handle both single-digit and multi-digit BCD numbers. For a single-digit BCD number, its equivalent binary representation consists of four binary digits. For a multi-digit BCD number, such as a two-digit number, its equivalent BCD representation includes eight binary digits. The first four digits represent the first decimal digit, and the next four digits represent the second decimal digit. The paper demonstrates that the proposed reversible BCD arithmetic circuit outperforms existing approaches in terms of the number of garbage outputs, constant inputs, and overall efficiency. It provides an effective solution for performing reversible BCD addition and subtraction in a single circuit, contributing to the advancement of BCD arithmetic circuits in digital systems.

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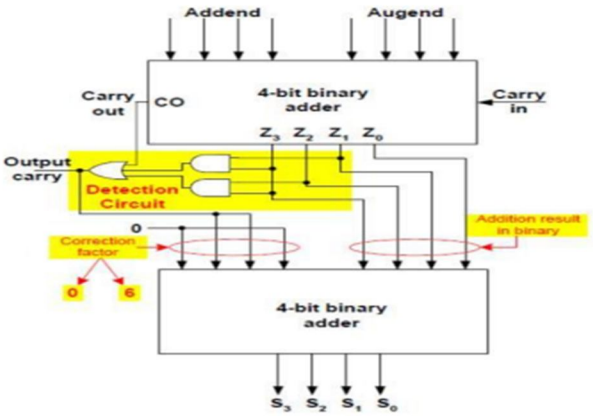


Fig 5: One Digit BCD adder

B. QCA BCD Adder

A conventional Binary Coded Decimal (BCD) adder is a circuit that adds two 4-bit BCD numbers in parallel and generates a 4-bit BCD result. The block diagram of a conventional BCD adder is shown in Figure 5. In order to produce valid BCD output, the circuit incorporates correction logic. The 4-bit BCD numbers (X and Y) along with a carry input are fed into a conventional 4-bit parallel adder. The adder computes a 4-bit sum and a carry output. To e ensure the BCD result is correct, additional steps are taken. If the carry output is set or if the sum exceeds nine (indicating a value greater than 9), the intermediate sum output is incremented by binary 0110. This correction is achieved using a second stage 4-bit parallel adder circuit. To understand the new design strategy, let's examine the 4-bit binary adder, denoted as ADD1. ADD1 takes inputs dA(3:0) and dB(3:0) (representing the BCD digits) along with the carry cin. It performs the binary addition and produces binary results bcout (carry out) and bS(3:0) (sum output). It has been demonstrated that in QCA-based rippling adders, the optimal logic structure for carrying a carry signal Ci through a single bit position involves introducing only one Majority Gate (MG) between Ci and Ci+1.In summary, the conventional BCD adder circuit adds two 4-bit BCD numbers in parallel, incorporates correction logic for generating valid BCD output, and utilizes a 4-bit parallel adder and correction stage. The new design strategy optimizes the carry propagation through a single bit position by employing a minimal number of Majority Gates.

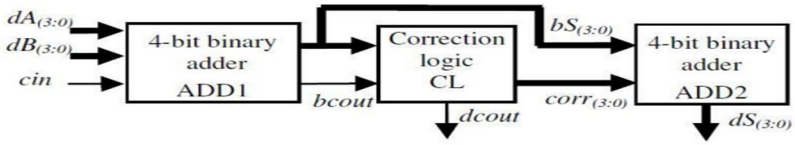


Fig 6: BCD Adder using QCA

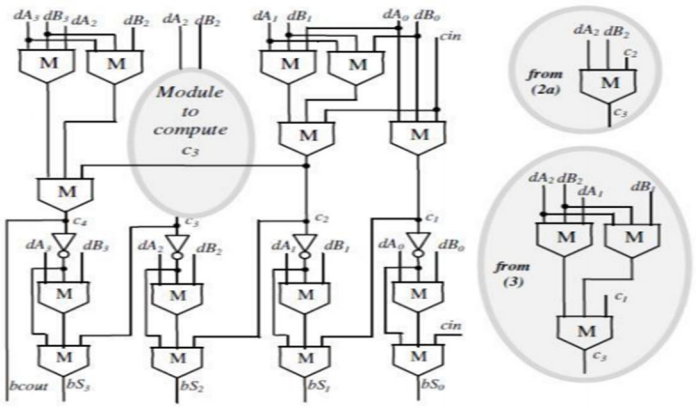


Fig 7: New BCD Adder Using QCA

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IV. XILINX ISE OVERVIEW

Xilinx ISE (Integrated Software Environment) is a comprehensive suite of tools developed by Xilinx, a leading provider of programmable logic devices (FPGAs) and related software. ISE is primarily used for designing, implementing, and debugging digital logic circuits on Xilinx FPGA platforms. Here's an overview of the main components and features of Xilinx ISE:

1) *Design Entry:* Xilinx ISE provides multiple methods for entering and capturing the digital design. Users can choose between schematic-based entry using the ISE Project Navigator, Hardware Description Language (HDL) entry using languages like VHDL or Verilog, or a combination of both.
2) *Synthesis:* Once the design is entered, ISE offers a synthesis tool that converts the high-level design description into a gate-level representation. It analyzes the design, optimizes it for area, power, and performance, and generates a corresponding netlist that can be used for subsequent steps.
3) *Implementation:* The implementation phase in Xilinx ISE involves mapping the synthesized design onto the target Xilinx FPGA device. It includes processes such as technology mapping, placement, and routing, which determine the physical configuration of the FPGA resources to realize the desired logic functionality.
4) *Constraints and Timing Analysis:* Xilinx ISE allows designers to specify constraints on the design, such as maximum clock frequencies, input/output delays, and resource allocation. Timing analysis tools within ISE perform static timing analysis to ensure that the design meets the specified constraints and operates correctly.
5) *Simulation:* ISE includes a built-in simulator that allows designers to verify the functionality of their designs before proceeding to the implementation phase. It supports both behavioural and gate-level simulations, enabling thorough testing and debugging of the design.
6) *Programming and Configuration:* Xilinx ISE provides tools for configuring and programming the Xilinx FPGA devices. This involves generating bitstreams or configuration files that can be loaded onto the FPGA to configure it for the desired functionality.
7) *Debugging and Analysis:* ISE offers various debugging features, including the ability to view waveforms, set breakpoints, and perform interactive debugging of the design. It also provides advanced analysis capabilities, such as power estimation, utilization reports, and resource utilization analysis.
8) *Third-Party Ecosystem:* Xilinx ISE is well-integrated with a wide range of third-party tools and IP (Intellectual Property) cores, allowing users to leverage pre-designed components and optimize their design flow.

V. SIMULATION RESULTS

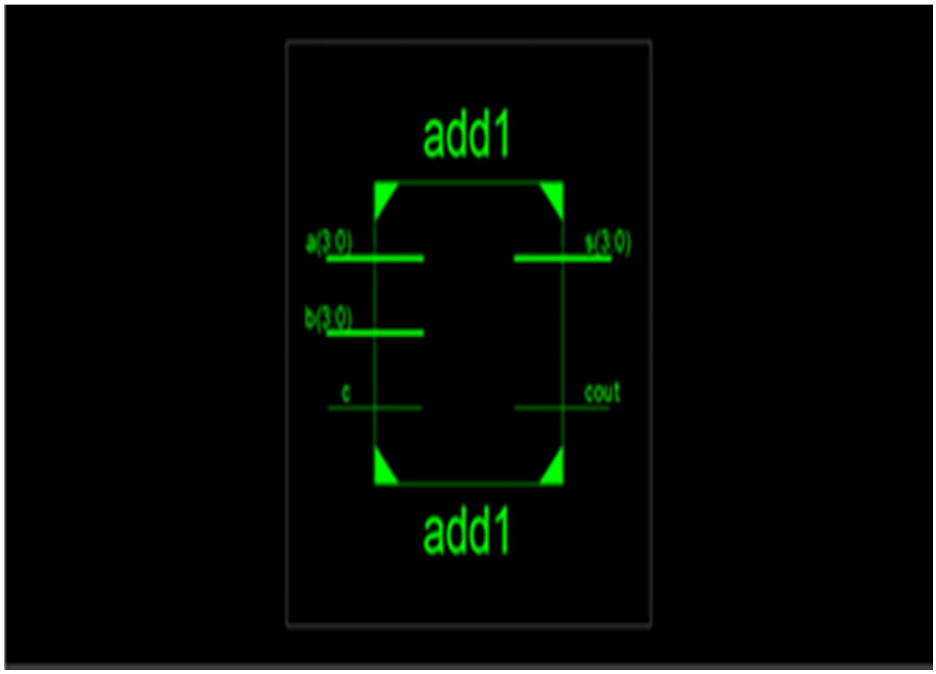


Fig 8: BCD adder schematic diagram.

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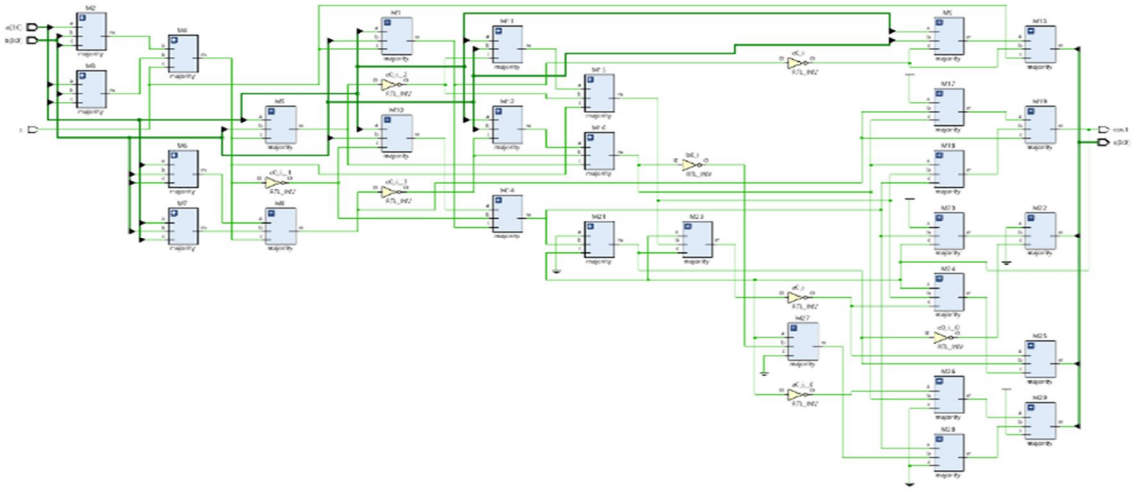


Fig 9: RTL diagram.

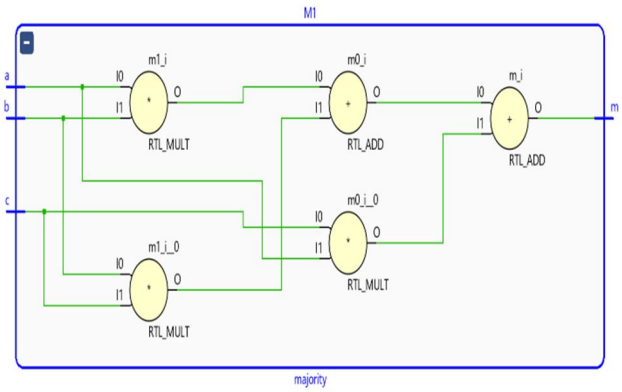


Fig 10. Internal Logic Circuit.

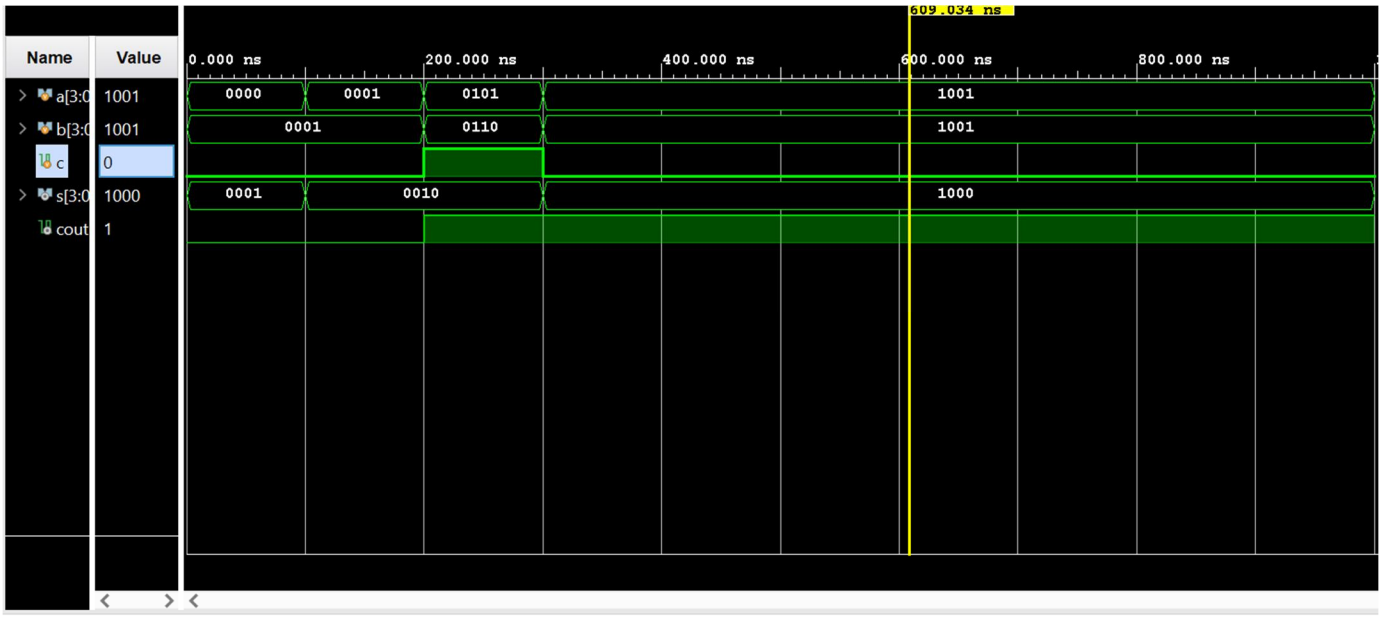


Fig 11. Timing diagram of QCA BCD adder.

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VI. CONCLUSION

In conclusion, the design of a Binary-Coded Decimal (BCD) adder using Quantum-dot Cellular Automata (QCA) technology offers promising prospects for high-performance arithmetic circuits. QCA technology provides advantages such as ultra-low power consumption and high-speed operation at the nanoscale, making it a potential alternative to conventional CMOS technology. The BCD adder design utilizing QCA gates and interconnections effectively performs addition of two BCD numbers, considering individual digit positions and carry generation. By leveraging the unique properties of QCA, such as electron localization, the design achieves the required logic functions for BCD addition, including carry propagation and generation. The evaluation of the BCD adder design demonstrates its potential for improved power consumption, delay, and area utilization compared to CMOS-based designs. These favorable metrics highlight the advantages of QCA technology and its applicability in digital systems. Overall, the design of the QCA-based BCD adder showcases the potential of QCA technology in advancing arithmetic circuits. It opens up avenues for further exploration and development of QCA-based designs for efficient and high-performance digital systems.

VII. FUTURE SCOPE

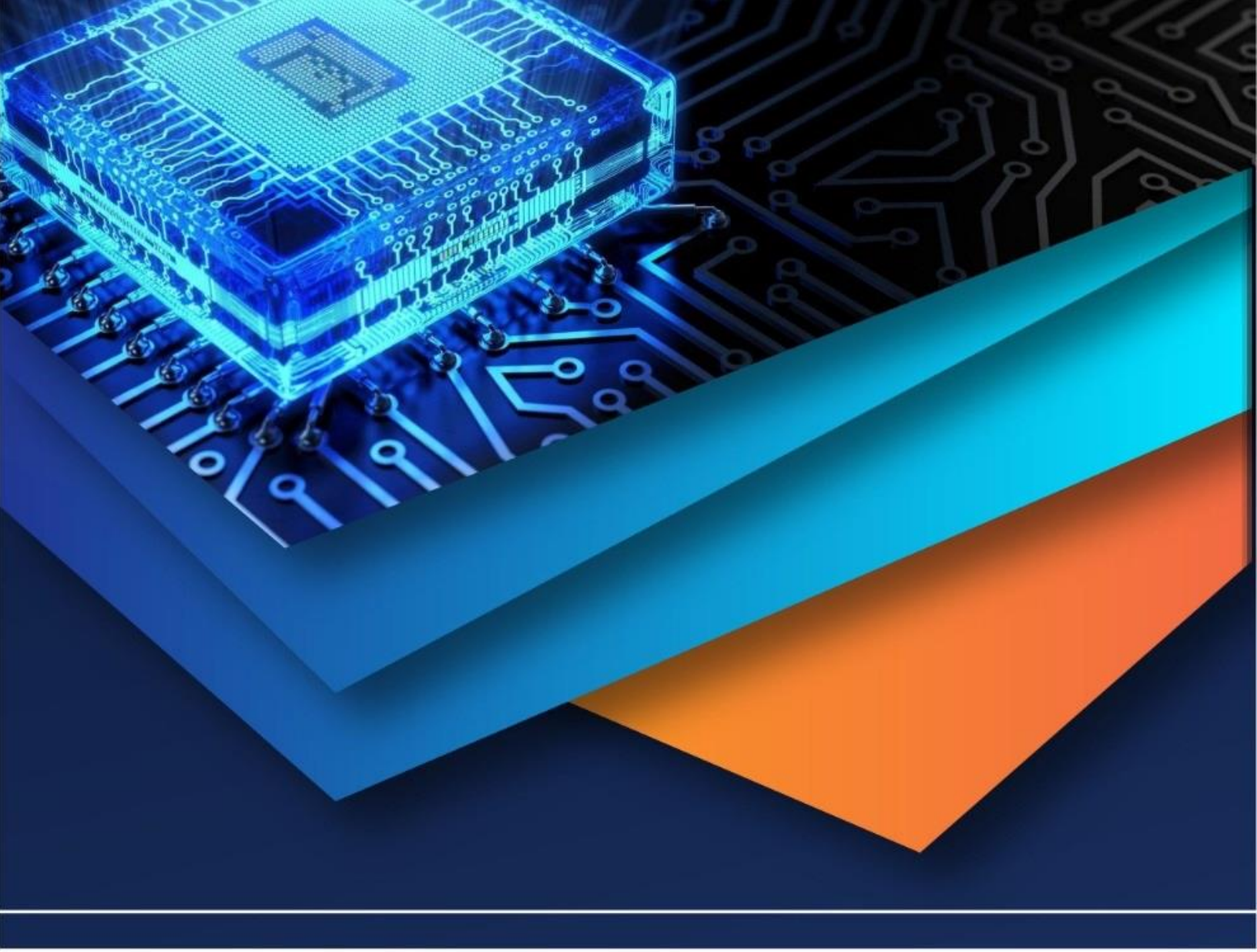
The future scope of QCA BCD adder is promising, offering several potential advancements and applications. Here are some key areas of future development:

1) *Scaling and Integration:* QCA technology has the potential for further scaling down to nanometer dimensions, enabling higher integration densities. The future scope involves optimizing the QCA BCD adder design for smaller footprints and exploring techniques to increase the number of digits that can be processed simultaneously.
2) *Power Efficiency:* QCA technology has inherent advantages in terms of low power consumption. Future research aims to explore advanced QCA architectures and circuit designs to further improve power efficiency, enabling energy-efficient computing systems.
3) *Speed and Performance:* QCA exhibits high switching speeds due to the absence of charge-based interactions. Future developments involve exploring techniques to enhance the performance of QCA BCD adders, such as reducing propagation delays, optimizing clocking schemes, and minimizing interconnect delays.

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