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Design of Full Swing Carry Generator Using Mentor Graphics

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Abstract: ***A Full adder is built specifically for creating full-swing carry output utilizing Mentor graphics in this project. Mentor Graphics is electronic design automation software that is used to create superior electronic devices more quickly and cost-effectively. The proposed circuit, which has a high driving capability, is suitable for a wide range of multistage structure applications. In digital processing equipment, full adders are used for multiple adders. This circuit design employs a unique mode to provide a full swing carry output, and its performance is governed by suitable inputs, static power reduction, and transistor series construction. The full adder proposed here is an efficient gate for Integrated Circuits (ICs).***
The performance between simulation and measurement produced a very good approximation result. When compared to other circuits, the cell's performance under variations indicates its excellent driving capabilities while consuming very little power and PDP. The circuit makes use of a one-of-a-kind module to provide full-swing Carry output, and its performance is governed by appropriate inputs, static power reduction, and transistor series formations.
Keywords: Driving capability, Full adder, Universal gates, Delay, Power consumption, and PDP.

I. INTRODUCTION

Nowadays, VLSI technology is widely used because it helps to design electronic components like microprocessors and memory chips, which require millions of transistors. Its application covers Safety systems, personal entertainment systems, and medical electronic systems.

VLSI (Very Large-Scale Integration) is a field of electronics that involves designing integrated circuits (ICs) with millions or billions of transistors on a single chip. The research in this area focuses on exploring new technologies like nanotechnology, 3D ICs, and quantum computing. This area of VLSI research focuses on developing design methodologies for chip design. This involves various stages like design entry, logic synthesis, physical design, verification, and testing. Complex digital systems can now be realized on a single silicon chip thanks to modern VLSI technology.

The semiconductor industry has been one of the fastest-growing segments of the global economy as a result of the steadily rising integration density and falling unit costs.

Everywhere VLSI circuits are utilized, including embedded processors in cars and other mobile devices, microprocessors in personal computers and workstations, graphic cards, digital cameras, camcorders, and cell phones.

The number of transistors that can be integrated into a single chip has significantly increased over the course of multiple generations of VLSI technology development. Bipolar, NMOS, PMOS, CMOS, BiCMOS, and other types are among them. Miniaturization and computer power have improved with each subsequent generation. Small-scale integration (SSI), medium-scale integration (MSI), large-scale integration (LSI), very large-scale integration (VLSI), ultra-large-scale integration (ULSI), and beyond are the first through fifth categories.

VLSI circuits are used in virtually every application, including embedded processors, anti-lock braking systems in automobiles, personal entertainment systems, medical electronic systems, and microprocessors in personal computers, graphic cards, digital cameras, camcorders, and phones. Field-programmable gate arrays (FPGAs), a type of reconfigurable embedded technology, are becoming more and more essential to modern society. Researchers are interested in digital circuits because they have a great future and a bright horizon. The new designs for digital circuits take into account energy conservation, high efficiency, and modest space occupation. Arithmetic blocks and other computing systems are crucial components of FPGAs and portable systems. In digital signal processors (DSPs) and central processing, units (CPUs) for image processing and digital filters like discrete cosine transforms (DCTs) and finite impulse responses (FIRs), multipliers are frequently utilized as arithmetic components. Half adders (HAs), full adders (FAs), ripple-carry adders (RCAs), and compressors typically comprise multipliers, with FAs serving as the central component of these complex cells. For the application of these systems, it is crucial to achieving an effective FA cell.

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The goal of VLSI design is to create smaller circuits that are highly efficient, fast, and reliable while minimizing power consumption and maximizing performance. VLSI design techniques include layout optimization, transistor sizing, and logic synthesis to achieve complex functionality in a compact form factor.

This letter proposes a novel, highly functional 1-bit FA cell based on a new block diagram. By utilizing cutting-edge circuit approaches including transmission gate logic, pass transistor logic, and other optimized designs, the suggested circuit performs better in these two VLSI applications while using fewer transistors. Compared to classic Adder, this leads to a more effective implementation with the decreased area, power consumption, and enhanced performance.

II. EASE OF USE

The low-power VLSI circuits are created for low-power requirements in industrial applications, according to Farid N. Najam and Gary K. Yeap [1]. The fundamentals of MOS transistors and the introduction to VLSI systems were outlined by Debaprasad Das [2]. In order to address the issues with traditional complementary metal-oxide semiconductor (CMOS) circuits, hybrid FAs have gained increased attention in recent years [4].

Power, delay, and area are the three key design criteria that are taken into account. In addition, factors including driving ability, stability, and fabrication defects are taken into account. The high power and delay time of traditional CMOS devices make up for their adequate stability against changes in the manufacturing process [3]. Despite CMOS' benefits, other methods are now being utilized as alternatives since CMOS requires a lot of space, has a lot of internal nodes, and generates a lot of static power because there are direct paths from the power supply (VDD) to the ground (GND). To reduce the power delay product (PDP) utilized in the fundamental VLSI circuit building blocks, full adders are created using pass transistor logic (PTL), CMOS logic, and an inverter logic next to XOR logic to create the logic of XNOR [5]. In order to eliminate circuit faults and arithmetic circuit errors, self-checking and self-repairing capabilities are proposed and employed, primarily in industrial applications, to consume little power and operate at high speed [6]. Transmission gate logic and CMOS are used in the modified full adder (MFA) design to minimize propagation latency and power consumption. The MFA generates a power delay with only 12 transistors plus an inverted XOR, NOR, and sum-generating module [7].

We describe a modified hybrid full adder (HFA) circuit with reduced latency, full swing outputs, and enhanced performance. In terms of driving capability, latency, power performance, and noise margin, it performs similarly to three previous modified hybrid full-adder circuits [8].In order to achieve similar or faster speed with less power and space usage, adder circuits with fewer transistors are being developed in comparison to full adder circuits.[9].We describe a modified hybrid full adder (HFA) circuit with reduced latency, full swing outputs, and enhanced performance.

Driving capability, latency, power performance, and noise margin are compared with those of three other modified hybrid full-adder circuits to assess how well it performs.[10]. Median filters are commonly used in image processing to get rid of impulse noise and keep edges in pictures. Sorting networks are used to implement real-time hardware, and this paper suggests a modified version of the current data comparators that uses two's complement and carry select methods to improve delay and area factors, making it suitable for high-speed and reduced area applications in the parallel architecture of modified shear sorting for developing a median filter.[11]. A nine-transistor full adder model is used to create an eight-bit ripple carry adder that reduces the circuit's power consumption in order to compare the efficiency of different full adders.[12]. To reduce the delay and excessive power consumption caused by high input impedance, a high-performance conventional carry look-ahead adder is developed for more demanding applications. [13].

Power and space-efficient multipliers are combined with approximate half adders, full adders, and OR gates for partial product accumulation in error-tolerant Digital Signal Processing (DSP) applications.[14]. Effective multipliers are crucial for applications including image processing, image recognition, and signal processing. Dadda multipliers can be implemented with a reduction methodology that significantly reduces the number of transistors, power consumption, propagation delay, and area, improving processor performance. This reduction methodology uses pass transistor logic and a binary to excess one converter in a square root carry select adder. [15].

The results demonstrate that the proposed MFA design performs better in terms of power delay and is suitable for application in VLSI circuits.

Given the aforementioned benefits and drawbacks of circuits, the majority of them work in accordance with a certain block design and comprise modules to produce outputs.

III. PROPOSED CIRCUIT

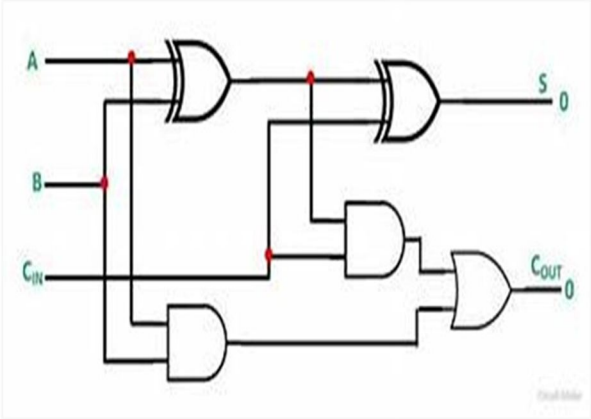


Fig.1 Full adder Block Diagram

In the block diagram above, a full adder circuit is constructed by joining two half-adder circuits with an OR gate. On the left side is the first half-adder circuit, which has two single-bit binary inputs A and B. It will generate two outputs, SUM(S0), and carry out, as was demonstrated in the prior half-adder tutorial.
The SUM(S0) output of the first half adder circuit is also provided to the input of the second half adder circuit. We enabled the carry-in bit over the second half order circuit's other input. Once more, it will output SUM(S0) and execute bit. The Full adder circuit's SUM(S0) output is its last output.
On the other hand, the OR logic gate is additionally provided with the Carry Out of the First Half Adder Circuit and the Carry Out of the Second Adder Circuit. The final carry-out of the full adder circuit is obtained after the logic OR of the two Carry outputs.

A digital circuit that adds three binary inputs and produces a sum and carry output. Used in computer arithmetic.
The most important bit, or MSB, is represented by the Final Carry out.

1) Sum(S0)

a) Combine the inputs A and B using the XOR method.
b) Execute an XOR operation on the result with carry.
c) The sum is then shown as (A XOR B) XOR.
d) C-in which is represented as (A ⊕ B) ⊕ C-in

2) Carry

a) Put inputs A and B through a 'AND' function.
b) Combine inputs A and B using the 'XOR' method.
c) Combine both of the outputs from the previous two steps using the 'OR' operation.
d) So, the 'Carry' can be represented as: (A.B) + (A ⊕ B)

Table.1 Truth table of full adder

A	B	C-in	SUM	C- out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

For different combinations of the input, outputs are calculated using the above equations. Since we have three inputs, we have eight combinations of the input to be verified for Sum and C_out.
This information is stated in the truth table shown in the below Table. 1

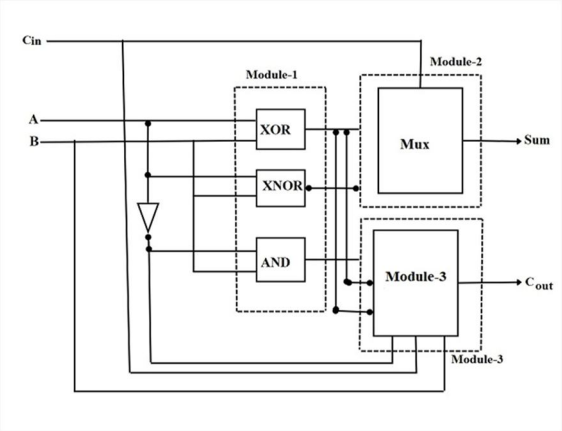


Fig.2 Full Swing Carry Generator

It has a strong driving capacity in this FA cell, making it more useful for multipliers. Sum and C_out must fully swing for this to happen, combined with low power and high speed. This circuit's established trade-off may result in an increase in area, but unique modifications to the transistors' ON/OFF states and asymmetric transistor operation enhance the suggested FA's performance for multistage applications.
Three modules make up the suggested block diagram. In the first, an AND gate is present in addition to XOR-XNOR gates, producing the AB. The Sum module has a similar structure to the traditional one, which is created by cascading XOR-XNOR and a MUX. A special structure creates the C_out. The C_out Boolean function is used to describe the Boolean equations; the output signals that must be passed are A B and A B. Here, the C_out can be formed similarly to a normal block by simplifying this relation, but the objective is to obtain a more beneficial output, hence the C_out relation is not simplified.
In order to avoid any simplification of the C_out relation, the transistor-level circuit of module 3 is built.

IV. SIMULATION TEST BENCH AND RESULTS

Engineers may test and validate the functionality of electronic designs using Mentor Graphics' test bench simulation software. It enables the creation of virtual test environments to excite and examine the behavior of electronic circuits or systems using sophisticated simulation techniques. This reduces the requirement for physical prototyping and testing by enabling the early detection and correction of design flaws. Test bench simulation from Mentor Graphics assists in enhancing design dependability, cutting down on development time, and optimizing overall product performance.

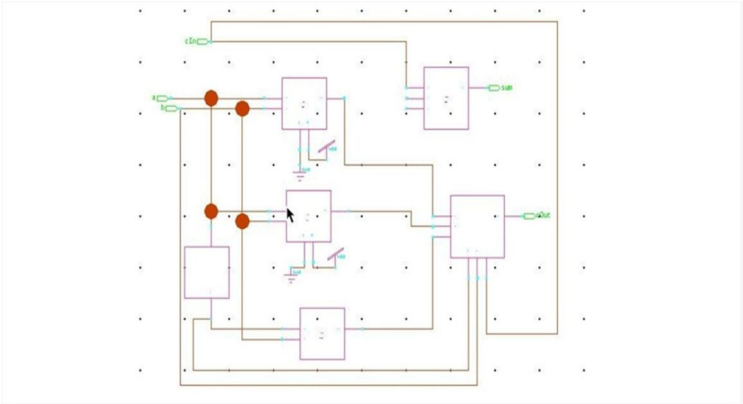


Fig.3 Schematic circuit diagram for the proposed block diagram

Digital circuits for arithmetic and logical operations, including adders and multipliers, depend on full-swing carry generators. In VLSI design, simulation test benches are frequently used to validate the performance of the carry generator under various input conditions.

A module that creates the carry generator module and delivers input stimulation to it often makes up the simulation test bench for a full-swing carry generator. To train multiple scenarios and cover all conceivable input combinations, the input stimulus includes a variety of combinations of input values (A, B, C_in). The carry generator's output values (Sum and C_out) produced throughout the simulation are tracked and recorded by the simulation test bench.

The complete adder computes the sum and carries outputs depending on the input values when the clock signal is high. The total output will be 1 and the carry output will be 0 if A and B are both low and C is high. The total output will be 1 and the carry output will be 0 if A and B are both high and C is low. The sum output will be 1 and the carry output will likewise be 1 if A, B, and C are all high. The sum output and carry output will both be zero in all other circumstances.

Timing diagrams, which display the output values across time, can be used to visualize the output waveform of a complete adder. Depending on the input values, the waveform will display a high or low state for each output at each clock cycle. The whole adder circuit's behaviour can be examined using the timing diagram to make sure it is operating properly.

A significant problem today is the scaling down of silicon-based electronics. In this instance, the planned FA was simulated using 45-nm technology and the predictive technology model (PTM), and the necessary outcomes were reached at high frequencies of 1 and 1.5 GHz.As shown in Table I, post-layout and validation tests are carried out, and the accuracy of the FA is proven in the presence of parasitic extractions.

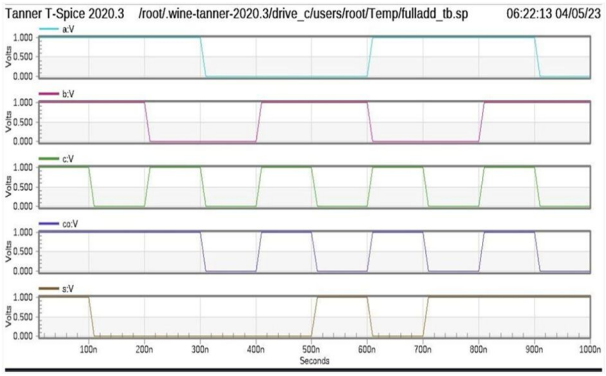


Fig.4 Full adder output waveform

Based on three input bits, the VLSI Full Adder circuit generates a sum bit and a carry bit as outputs. It supports carry propagation and binary addition. The input combinations determine the output waveform, which adheres to addition logic.

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Table.2 Full swing carry generator output analysis

Condition	Power(uw)	Delay(ns)	PDP(fJ)
Pre-Layout	8.4712	0.5312	4.50
Post Layout	11.862	0.921	10.92
Difference	40.03%	73.38%	2.82x

The performance of the carry generator can be assessed using simulation test benches in addition to functional verification in terms of timing, power consumption, and other pertinent metrics. This enables designers to enhance the design and make the necessary modifications to satisfy the required performance standards.

In conclusion, simulation test benches are essential for testing the performance and functionality of a full-swing carry generator during the VLSI design phase. The carry generator can be thoroughly tested under various input situations, and the results of the simulation can assist detect and fix any problems or faults, ensuring the dependability and accuracy of the digital circuit.

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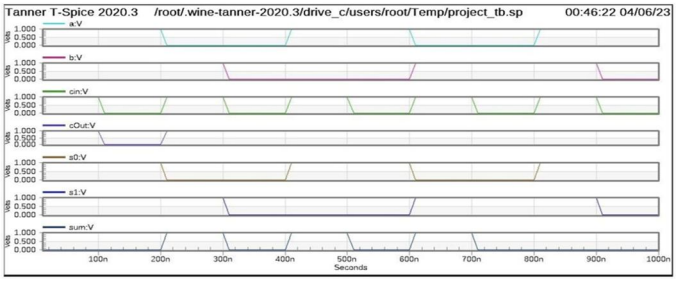


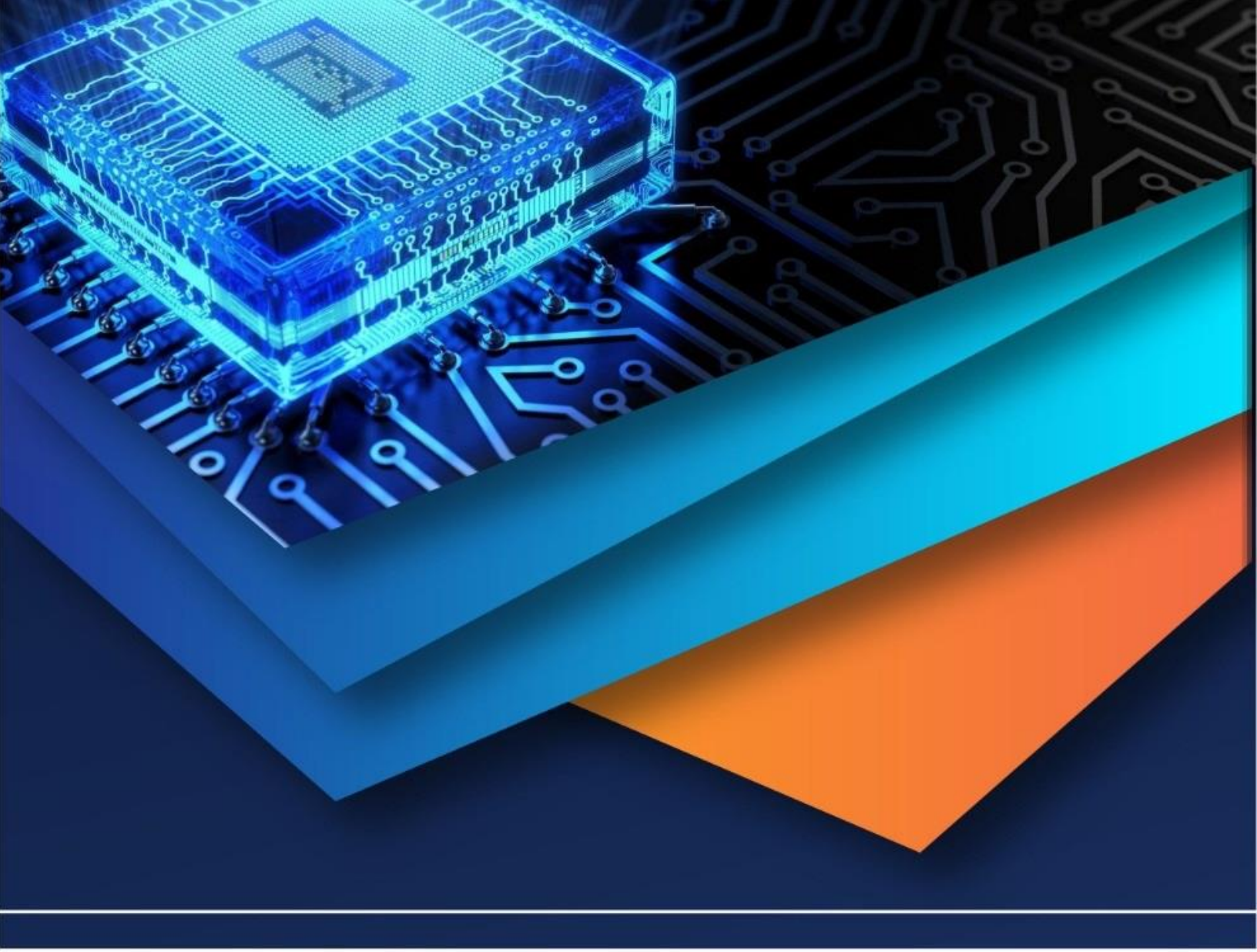
Fig.5 Full swing carry generator

V. CONCLUSION

By utilizing cutting-edge circuit approaches like pass-transistor logic, transmission gate logic, or other optimized designs, a proposed Full Adder architecture in VLSI lowers the transistor count. Compared to conventional Full Adder designs, this leads to a more effective implementation with decreased size, power consumption, and enhanced performance**.** For a stable and high-performance operation, the use of Mentor Graphics in the design of a full-swing carry generator offers an efficient and effective solution for digital circuit design. For a variety of digital applications, it enables designers to build full-swing carry generators that are reliable and optimal. The full-swing carry generator is made to produce carry signals in digital circuits, making it possible to quickly and accurately add or subtract multi-bit integers. In conclusion, the full-swing carry generator is a critical component in digital circuit design, specifically in arithmetic logic units (ALUs) and adder circuits. It offers high-speed, low-latency carry propagation across multiple stages, enabling efficient and reliable arithmetic operations. The full-swing carry generator is advantageous due to its ability to minimize signal delay, power consumption, and area overhead while providing robust performance in various digital systems. Overall, the full-swing carry generator is a key element in modern digital circuit design, contributing to high-performance and low-power arithmetic operations.

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