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Design of High Speed and Area Efficient N-Bit Digital Comparator

Sahithi Sunkireddy[1], Sahithi Thallapally[2], Ganesh Avula[3], B. Shivani Gayatri Devi[4]
[1, 2, 3, 4]*Student, 4th year ECE, CMR Technical Campus, Kandlakoya(V), Medchal Road, Hyderabad*

Abstract: ***A digital comparator is a hardware electronic device or a combinational logic circuit. It is capable of comparing two numbers as input in binary form and determines the output. In the previous designs like in the design of XOR-XNOR(XE) with cross-coupled p-MOS, even though it occupies less area, the full swing output voltage can't be able to produce which creates a problem when the bit width increases. To avoid this kind of disadvantages we are designing a N-bit digital comparator in a way such that it produces full swing output voltage with the improved power efficiency as well as the transistor count in the circuit also decreases. So that it can be used in several applications like scientific computations and test circuit applications etc.***

I. INTRODUCTION

A digital comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to other number. It can be used in several applications such as IR sensors, OP-amp's, Image processing etc.

In one of the previous designs [9], an eight transistor XOR-XNOR(XE) with cross-coupled P-MOS, is used to design the comparator and it helps in improving the speed and power efficiency. But it is not applicable in the increased bit-widths because if the bit width increases it can't be able to produce full swing output voltage.

In another design [8], it uses different logic techniques for the comparison of transistor count, power consumption and propagation delay. And to improve the propagation delay a hierarchical prefix tree structure method had been proposed [10]. However, the power consumption will be more for $\log_2 N$ comparison levels for the wide input operands. Several comparator designs have also been verified like parallel prefix tree structure's, dynamic logics, using subtractors or multipliers in the designing process etc. each having several specifications.

In the evolving VLSI technology, it is important to design any electronic component with less area and improved power efficiency and operating speed. In this paper we are designing the comparator which is efficient in terms of speed, power consumption and area. To improve the power consumption, we have used parallel prefix tree structure method, and to produce the full swing output voltage a novel EX-OR-NOR cell had been considered from [3].

Table 1: Used symbols and abbreviations

ALB	A is less than B
AEB	A is equal to B
AGB	A is greater than B
A	Input operand
B	Input operand
E	Represents equal bit pair
X	Represents unequal bit pair
$\odot$	X-NOR operation
$\oplus$	X-OR operation
CEM	Comparison evaluation model
FM	Final module

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II. DESIGN METHODOLOGY

Let's consider 2 input operands A and B as shown in fig.1. In the comparison process, the bits will be compared form MSB to LSB. It keeps comparing until it encounters two unequal bit pairs. If the output is equal then it means that AEB. If the output is not equal then it will check for less than or greater than. In comparing the bits from MSB to LSB the bit that first encounters logic 1 is greater than the other operand. The outputs for unequal bit pairs are AGB and ALB.

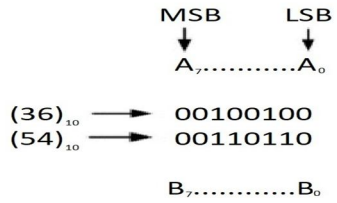


Fig 1**:** Comparison between two 8-bit operands

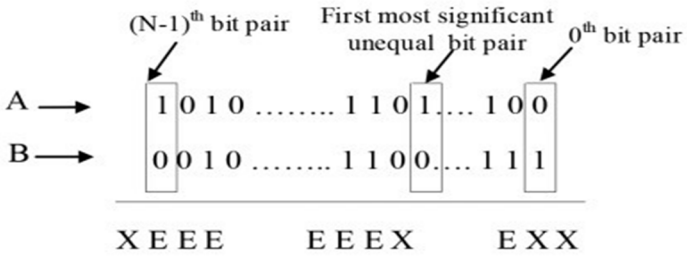


Fig 2: Comparison between two N-bit operands

III. CIRCUIT DESCRIPTION

For the proposed N-bit comparator the RTL design for a 4-bit is shown in fig.3. The circuit has been divided into two sections, they are

A. Comparison Evaluation Module (CEM)

Comparison evaluation module as the name indicates all the comparison process will be done in this section. This section has its individual steps, in each step each type of operation will be performed. In step 1, the XOR and X-NOR operations will be performed. In step 2, AND logic will be used and the inputs are the outputs of XNOR operation from step1 and equality pin(E). In step 3, NAND operation will be performed and the inputs for the NAND gate are the outputs of XOR operation in step1, E and input bits of the operand A. In step 4, the outputs of the NAND logic will be given as the inputs to another NAND gate.

Section 2 is known as Final Module. The final result will be decided in this section. The outputs of step 2 and step 4 will be provided as the inputs to the 1st NOR logic and it decides the logic o or 1 for ALB, if ALB=0 then this output and the output of step2 will be provided as the inputs for the 2nd logic and the final result will be provided.

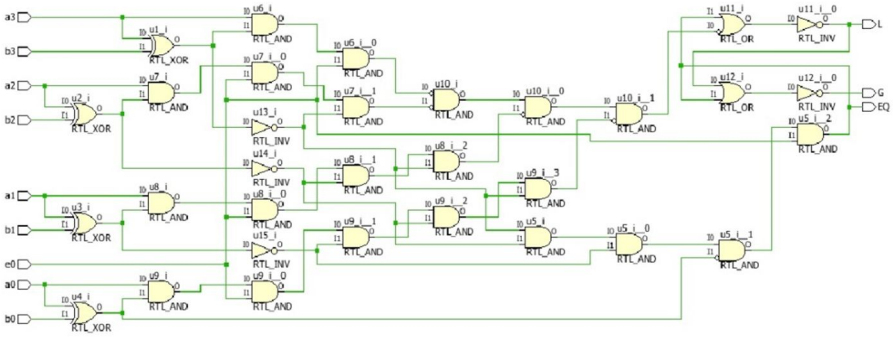


Fig.3: RTL design of the 4-bit comparator with reference to the proposed N-bit digital comparator

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B. Novel Ex-OR-NOR cell

This novel EX-OR-NOR cell is based on pass transistor logic and CMOS logic and this logic has been considered from [3]. It consists of 7 transistors. The M5 transistor in the cell is used for producing full swing output voltage as shown in fig6. In the feedback a PMOS transistor is connected which helps in maintain the logic level on the EX-NOR output terminal. The CMOS logic is used to improve the output for achieving the full swing on the EX-OR output terminal.

Let's consider an example for the proposed N-bit comparator. To explain the process, we have considered a two 4-bit operands A and B, where A=1100, B=1010. Set 1 compares for the equal and unequal bit pairs. The outputs of set 1 are 1001 and 0110. The output 1001 will be the input for set 2 which includes E_0=1 and the output of set 2 is AEB=0. In set 3 and 4 the NAND logic will be performed with its previous sets outputs as it's input's. And in set 5 the final result will be obtained i.e., ALB=0and AGB=1.

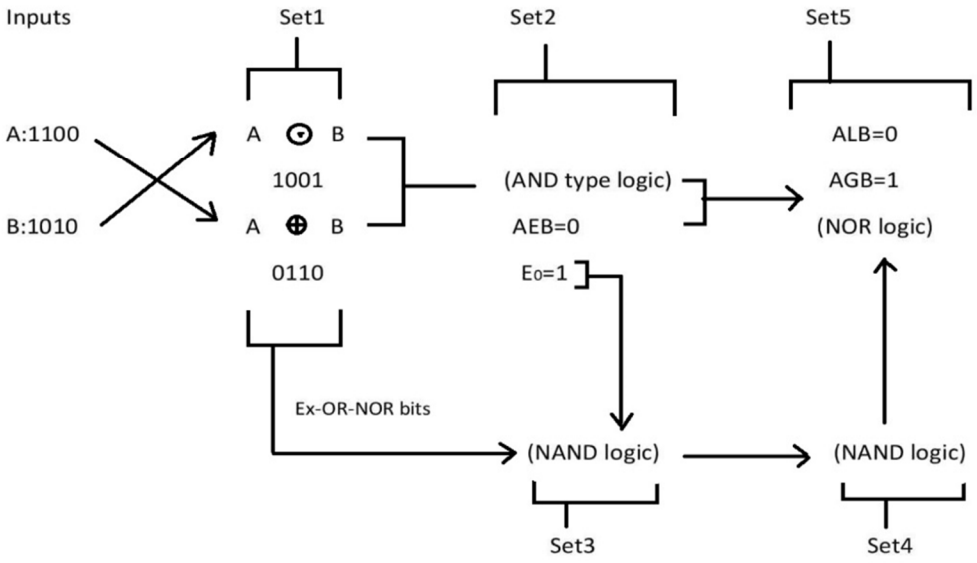


Fig.4: 4-bit comparison using the proposed methodology

IV. AREA, POWER CONSUMPTION AND OPERATING SPEED ESTIMATIONS

A. Area Analysis

The area is analysed by estimating the total number of cells required in each set and the logic cells will be translated into total number of transistors [3]. The total number of logic cells required in CEM and FM are

LC_{CEM} = (N × (set 1 cell)) + (N/4 × (set 2 cell)) + (N × (set 3 cell)) + (N/4 × (set 4 cell))

LC_{FM} = (2 × (set 5 cell))

Where N = Bit-width, LC_{CEM} = Logic cells in CEM, LC_{FM} = Logic cells in FM

Table 2: The following table illustrates total number of transistors for different bit-widths in CEM

Bit-width	Number of transistors in set 1	Number of transistors in set 2	Number of transistors in set 3	Number of transistors in set 4	Total Number of transistors
4	28	-	48	8	84
8	56	12	96	16	180
16	112	36	192	32	372
32	224	84	84	64	756
64	448	180	768	128	1524

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B. Power Consumption Estimation

To minimise the power usage, we need to reduce the usage of no. of transistors. Mainly we have to minimise the switching activities. Hence in the proposed comparator the switching activities have been minimised using the termination bits in the computations.

The below graph compares the transistors used in the proposed comparator and different comparators

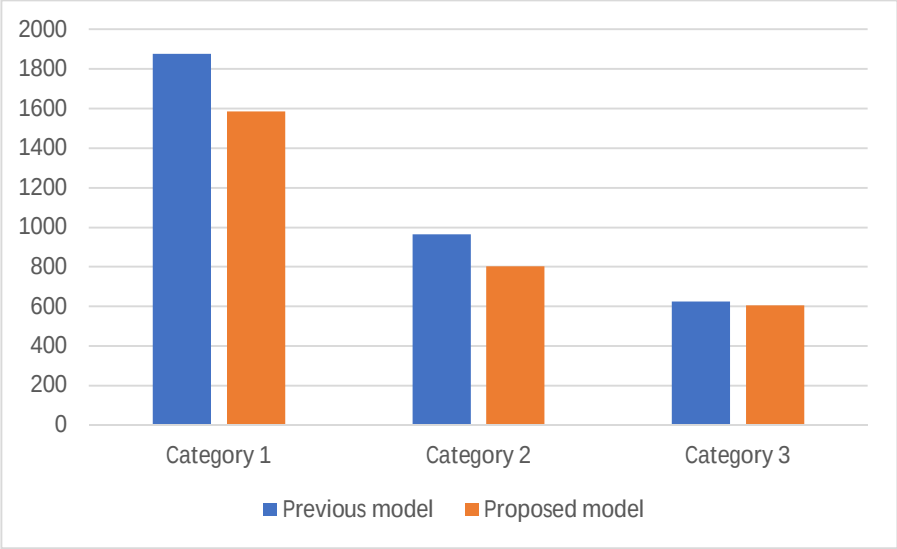


Fig. 5: The graph compares the usage of transistors in the proposed model with the previous models

The X-axis indicates Different comparator structures and the Y-axis indicates Number of transistors.

C. Operating Speed

The operating speed is estimated by the total delay. The total delay is the summation of the cell delays that comes across in the critical path. The total critical path delay (D_{CEM}) in CEM can be estimated by using the following equations [3]

$$D_{CEM} = D_{set\ 1} + D_{set\ 2} + D_{set\ 3} + D_{set\ 4}$$

where, $D_{set\ 1}$, $D_{set\ 3}$ and $D_{set\ 4}$ is equal to D_u and $D_{set\ 2}$ is equal to (N/4) D_U. Hence, the above equation can be written as

$$D_{CEM} = D_U + (N/4)\ D_U + D_U + D_U$$

The total delay in FM(D_{FM}) is estimated by

$$D_{FM} = 2D_U$$

Hence the total delay can be written as

$$D_T = D_{CEM} + D_{FM}$$
$$D_T = 5D_U + (N/4)\ D_U$$

Table 3: Delays for different bit-widths of this model compared with previous models

Bit-width	Maximum delay(ns) for the proposed comparator	Maximum delay(ns) for the previous comparators
4	0.29	0.53
8	0.31	0.62
16	0.37	0.86
32	0.47	1.12
64	0.53	1.93

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V. RESULTS

The proposed N-bit digital comparator has been designed and observed for 4-bit comparison. The RTL design and the behavioral simulation results for the 4-bit are shown in the following figures. And it is observed on Zed-board

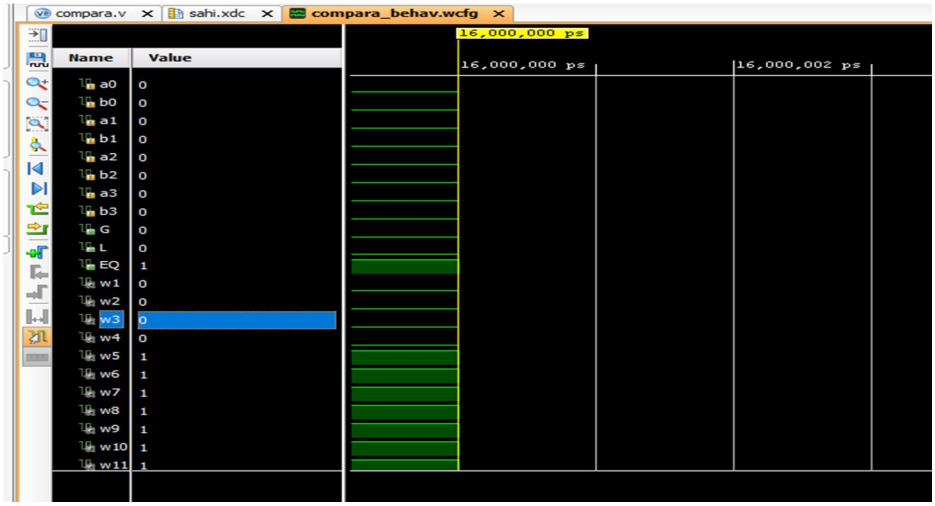


Fig. 6: Behavioural simulation of a 4-bit comparator for A=B

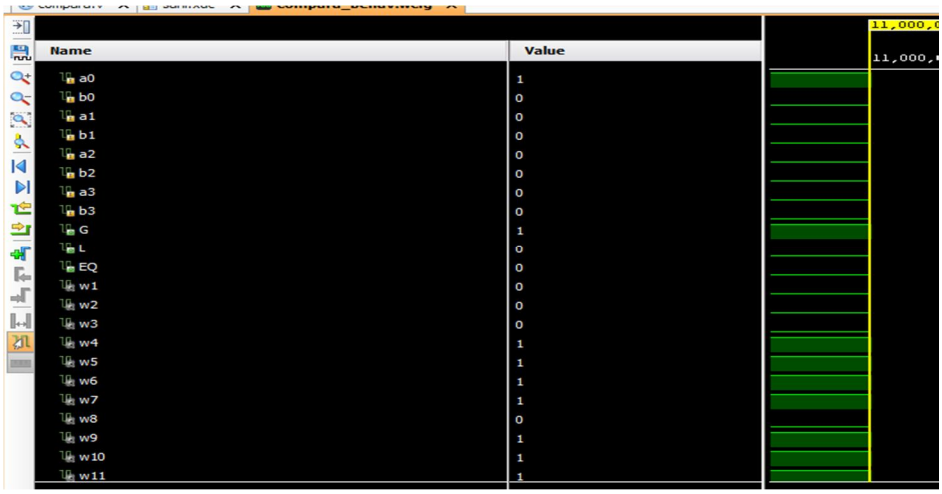


Fig.7**:** Behavioural simulation of a 4-bit comparator for A>B

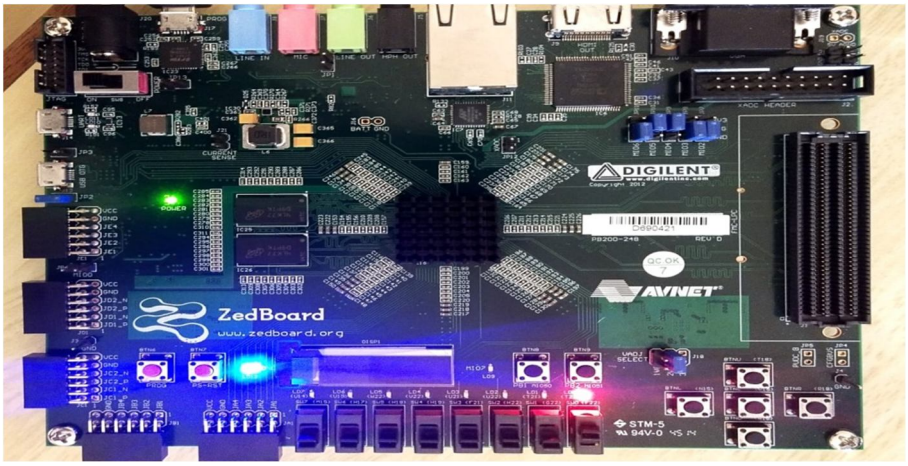


Fig. 8: 4-bit comparison for A<B on Zed-Board

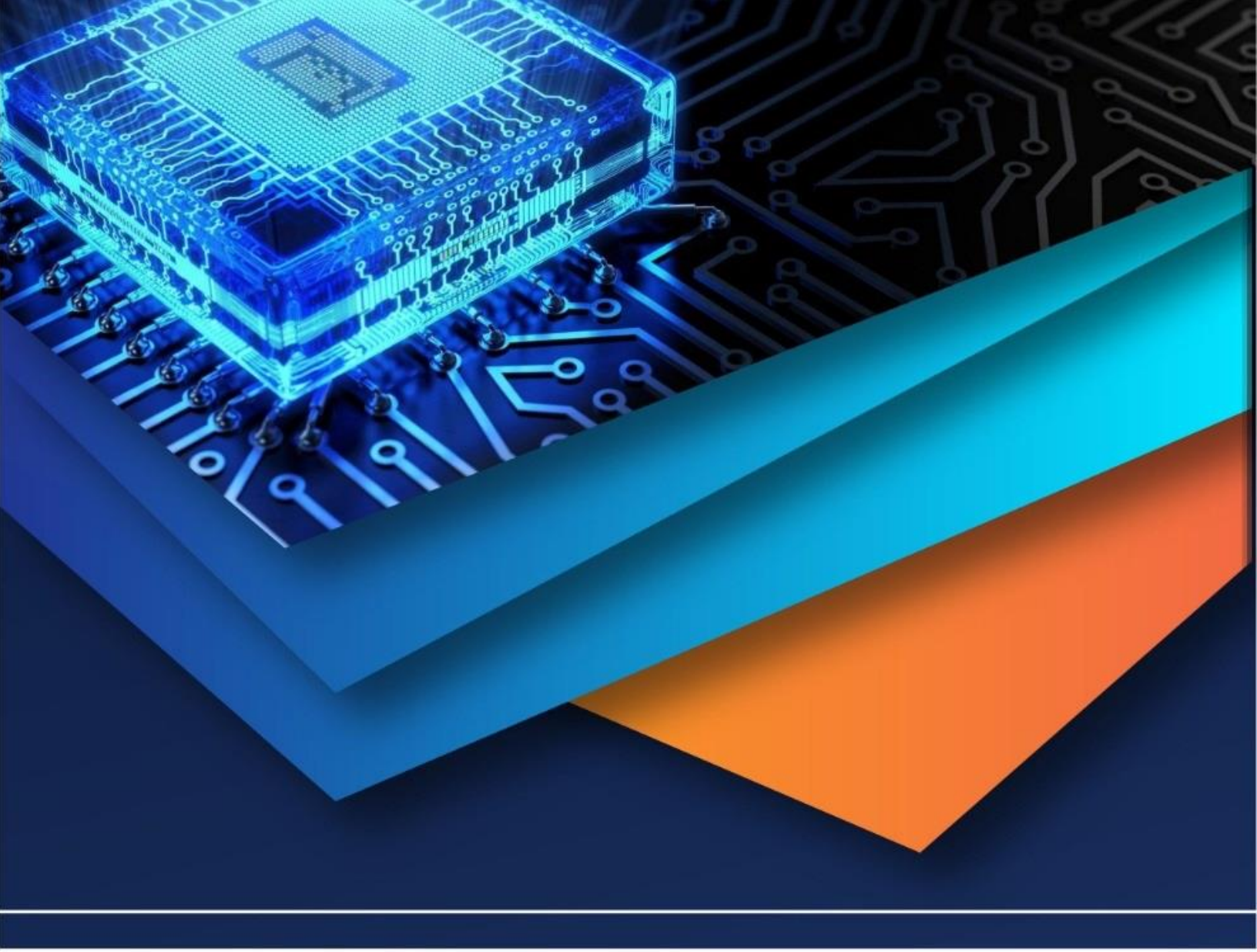
VI. CONCLUSION

This paper presents a novel EX-OR-NOR cell which is used in implementing the proposed N-bit comparator and also this novel cell is used for producing the full swing output voltage for larger bit-width. The estimations for power, area and the operating speed has also been discussed. With the advantages of the proposed model, it can be used in several applications such as test circuits, memory addressing logic, scientific computations etc.

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