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Design of Low Power 64-Bit Hybrid Full Adder

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Abstract: ***In the realm of Computer Science, integrated circuits (ICs) have propelled microprocessor and digital signal processor development, hinging on the 1-bit full adder's significance for mathematical tasks. To amplify overall efficiency, enhancing this adder is pivotal. As demand surges for power-efficient devices like smartphones and MP3 players, maintaining a balance between speed, size, and power usage becomes imperative. Engineers tackle this challenge while bridging battery technology gaps. We propose advanced 1-bit full adder designs, evaluated via Cadence Virtuoso. A hybrid version merges Pass-Transistor Logic (PTL), Transmission Gates (TGs), and static CMOS logic. An optimized alternative incorporates efficient 3T-XOR logic. The comparative study considers crucial metrics: the existing FA's 8.83µW power vs. the proposed's 8.49µW; the proposed's shorter delay of 64.53ps vs. the existing FA's 83.1ps (18 vs. 22 transistors). At 64 bits, the existing FA's consumes 66.8µW with a 470.94ps delay (1408 transistors), while the proposed maintains 35.05µW, 64.53ps, and fewer transistors (1152). In summary, the proposed adder excels in efficiency, delay, and transistor use for energy-efficient arithmetic operations.***

Keywords: 1-bit full adder, hybrid design, low-power circuits, 3T-XOR logic, power efficiency, delay analysis.

I. INTRODUCTION

The rapid advancement of transistor scaling has propelled extensive research in the domain of low-power microelectronic circuit design. Consequently, there has been an exponential surge in the demand for high-performance microelectronic circuit designs. This trend is particularly pronounced in modern applications like image and video processing, digital signal processing (DSP) chips, microprocessors, and numerous others, where substantial arithmetic operations are required. Among these operations, addition stands as a foundational arithmetic function frequently employed in contemporary computational tasks. The 1-bit Full Adder (FA) holds a central role in binary addition as the basic building block for constructing wider word-length adders. As such, enhancing the performance of the FA is pivotal for overall improvements in Arithmetic and Logic Unit (ALU) performance within microprocessors. This article introduces a novel hybrid FA design that incorporates Pass-Transistor Logic (PTs), Transmission Gates (TGs), and 3T-XOR logic. The FA design is implemented using the Cadence toolset within a 180 nm technology context.

II. LITERATURE REVIEW

In the realm of designing Full Adders (FAs) in microelectronics, various logic styles have been employed to achieve different trade-offs between performance, power consumption, and area utilization. Three commonly used single logic style FAs are Complementary Pass Transistor Logic (CPL) based FA [1], 12 Transistor (12-T) FA [2], and Conventional CMOS (C-CMOS) logic based FA [3]. CPL-based FA introduces a dynamic element but suffers from voltage degradation, necessitating additional buffers to restore the signal to the supply voltage level. On the other hand, C-CMOS FA avoids voltage degradation but faces challenges due to its significant input impedance.

To address the limitations of single logic style FAs, researchers have shifted towards hybrid design approaches that integrate the favorable aspects of multiple logic styles within a single FA cell. Two examples of this trend are the TG Adder (TGA) [4, 5] and the Transmission Function Adder (TFA) [6], both of which incorporate Transmission Gates (TGs) in their design to mitigate voltage degradation. However, poor driving capability becomes a significant concern in TGA and TFA FAs.

Other FAs, such as the 24-transistor (24-T) FA [7], 14-transistor (14-T) FA [8], and 10-transistor (10-T) FA [9], utilize multiple logic styles for implementation. The 24-T FA optimizes sum calculation using a 3-input XOR gate, unlike the conventional approach of cascading two separate 2-input XOR gates. The 14-T and 10-T FAs route input bits through a XOR gate acting as an intermediate node, contributing to their low transistor count and compact area. However, these designs face challenges related to driving capability, limiting their application in scenarios with high fan-out.

The Hybrid Pass Static CMOS (HPSC) FA [10] is designed using Pass Transistor Logic (PTL) to generate XOR and XNOR signals in intermediate nodes, while C-CMOS logic is employed on the output side for full-swing outputs. This approach maintains output quality but increases transistor count and capacitance due to the incorporation of C-CMOS logic.

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Innovative designs like the Double Pass Transistor Logic (DPL) and Swing Restored CPL (SRCPL) Hybrid FAs [11] generate AND-OR signals for output carry and XOR-XNOR signals for the sum output. The input carry serves as the select bit for TG-based multiplexers (MUX) to generate outputs from intermediate AND-OR and XOR-XNOR nodes. The Hybrid FA design in [12] employs an inverter in the output side and integrates CPL and TG logic in the input side. The addition of a C-CMOS logic-based inverter in the output side enhances the driving capacity of the FA. Several more Hybrid FAs are reported in [13]–[17], expanding the range of possibilities in this domain.

Gate Diffusion Input (GDI) technique has led to the development of three FA designs (GDI D1, GDI D2, and GDI D3) [18]. While these designs offer innovation, they grapple with the challenge of weak output signals, which can impact the overall performance and reliability of the adder.

III. METHODOLOGY

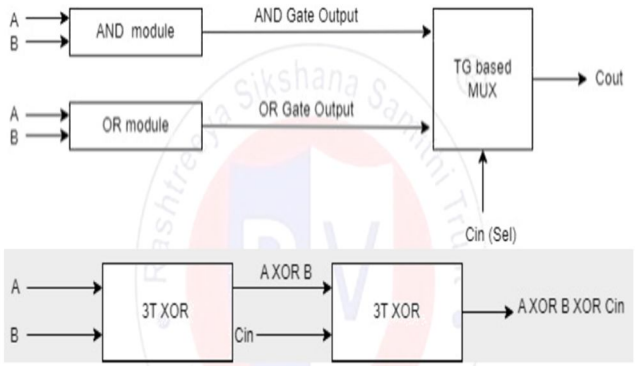


Figure 3.1: Block diagram of proposed 1-bit full adder

The design approach of the proposed Full Adder (FA) involves a systematic division into four primary modules: two modules dedicated to carry generation and two for sum generation, as illustrated in Figure 1. The schematic representation of the proposed design is depicted in Figure 2. The design methodology proceeds through the following sequential sub-sections:

A. Carry Generation

From the observation of the truth table of a Full Adder (FA), it becomes apparent that the carry output (Cout) is governed by specific logical conditions dependent on the input carry (Cin) and the inputs A and B. Two novel modules (modules 1 and 2) are devised for efficient carry generation. The AND-OR module within this scheme, realized through Transmission Gates (TGs) and Complementary Pass Transistor Logic (CPL), executes the carry logic. Distinct conditions such as A = 0 and A = 1 are meticulously implemented through pass transistors and Transmission Gates. A 2:1 Multiplexer (module 2) steers the appropriate carry-out signal, factoring in the input carry (Cin).

B. Sum Generation

The sum output in the initial FA[19] is derived by cascading two XOR modules (modules 3 and 4), both utilizing identical structures. Employing Transmission Gates (TGs) and Pass Transistor Logic (PTs), these XOR gates perform the logical operations based on inputs A and B. The design involves distinct conditions, e.g., A = 0, A = 1, B = 0, and B = 1, systematically implemented using Transmission Gates and pass transistors.

Notably, the initial sum circuit[19], utilizing Pass Transistor (PT) logic, has been enhanced to leverage a more efficient 3T-XOR logic configuration. In this revised approach, the 3T-XOR gate plays a central role in generating the sum output. Its operation hinges on the XOR operation, taking inputs A, B, and Cin into account. By integrating three transistors, including two NMOS and one PMOS, the 3T-XOR gate orchestrates logical operations based on input signals. The transition from PT logic to 3T-XOR logic optimizes the sum calculation within the full adder structure, resulting in reduced transistor count and potential area efficiency. While this transition offers efficiency gains, designers must address challenges like voltage drops and propagation delays associated with the transistor arrangement.

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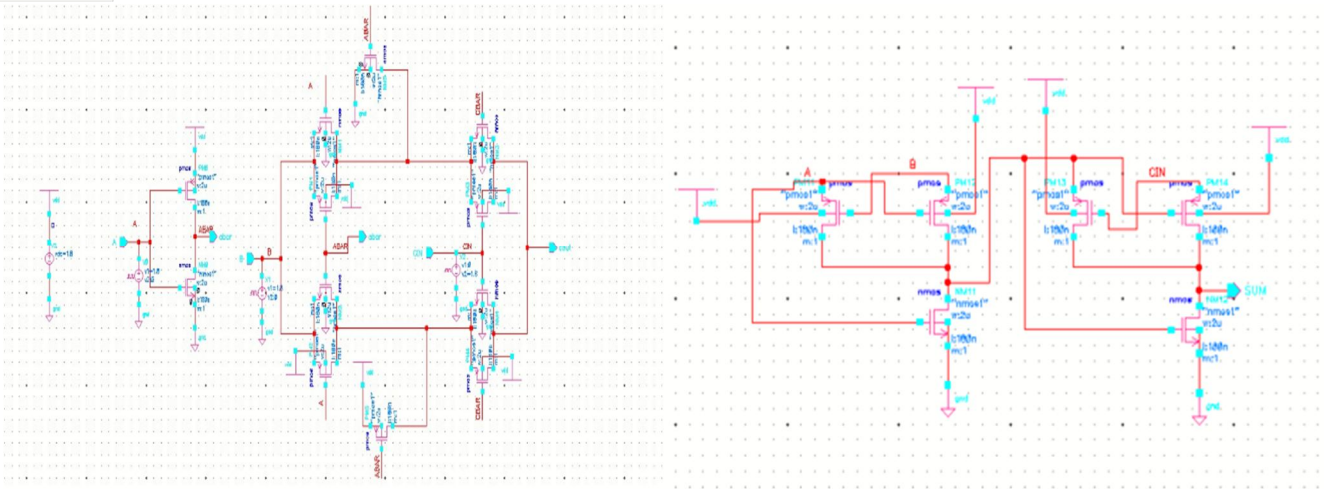


Fig.3.2 Schematic of proposed 1-bit full adder

Advantages of using 3T XOR gates over pass-transistor logic (PTL) XOR gates in the construction of a full adder, focusing on area, power, and delay considerations.

1) *Area Efficiency:* In a full adder circuit, you need multiple XOR gates to perform various intermediate computations. Using 3T XOR gates could lead to better area efficiency for the following reasons:

- *Transistor Count:* 3T XOR gates use fewer transistors compared to PTL XOR gates. In a full adder, where multiple XOR gates are needed, reducing the transistor count for each XOR gate can add up to significant area savings in the entire circuit.
- *Layout Complexity:* PTL XOR gates involve more complex layouts due to the use of additional transistors and their interconnections. This complexity can contribute to larger layout area requirements.
- *Power Efficiency:* Reduced power consumption is another potential advantage of using 3T XOR gates in a full adder:
- *Static Power:* With fewer transistors in 3T XOR gates, there is generally lower leakage current and therefore reduced static power consumption compared to PTL XOR gates.
- *Dynamic Power:* 3T XOR gates might have lower dynamic power consumption because they involve fewer transistors that need to switch during each XOR operation. This can be especially beneficial in a full adder, where multiple XOR gates switch frequently during addition operations.

2) *Delay:* In a full adder, minimizing delay is crucial to achieve high-speed operation. Here's how 3T XOR gates could provide an advantage in terms of delay:

- *Intrinsic Delay:* 3T XOR gates typically have lower intrinsic delay compared to PTL XOR gates. This lower delay can contribute to faster signal propagation within the full adder circuit.
- *Cascade Effects:* Since full adders often consist of multiple stages cascaded together, the lower delay of 3T XOR gates can help reduce the cumulative delay across the entire adder circuit.
- Potential Power Savings: With fewer transistors, 3T-XOR logic might consume less power compared to larger XOR gates. This can be advantageous in low-power designs. design accordingly

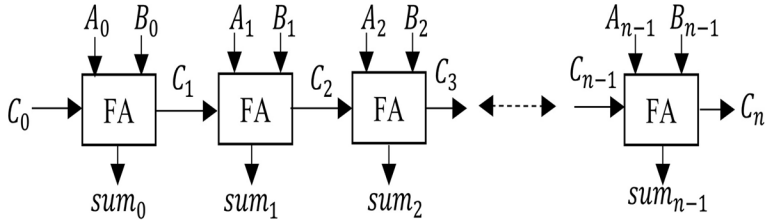


Fig. 3.3. Implementation of n-bit adder using 1-bit FA.

To evaluate its scalability, the proposed Full Adder (FA) design has been extended to accommodate word lengths of up to 64 bits.

IV. RESULTS AND DISCUSSIONS

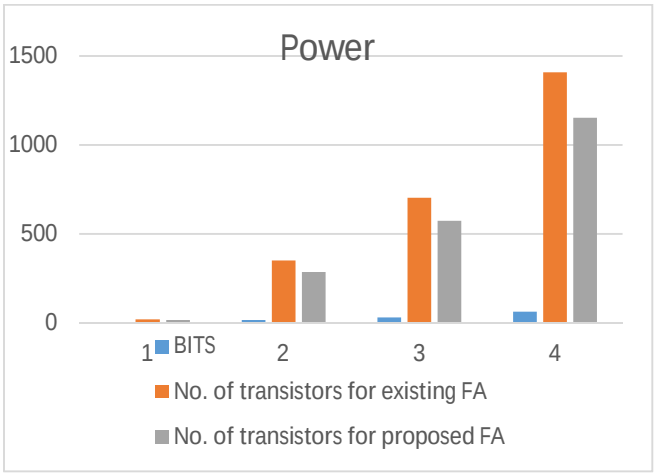


Fig.4.1 Comparison of power between existing full adder [19] with proposed full adder for 1-bit ,16-bit, 32-bit and 64-bits respectively

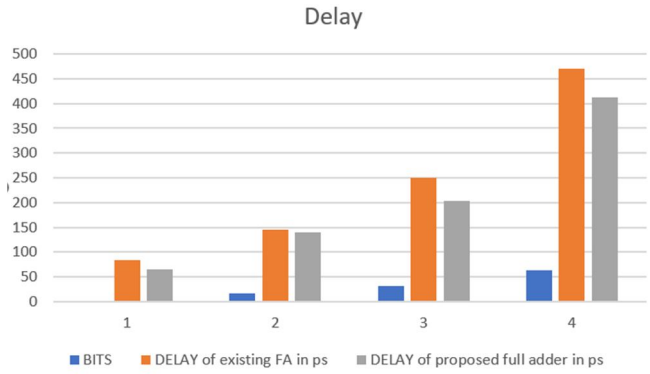


Fig.4.2 Comparison of delay between existing full adder [19] with proposed full adder for 1-bit ,16-bit, 32-bit and 64-bits respectively

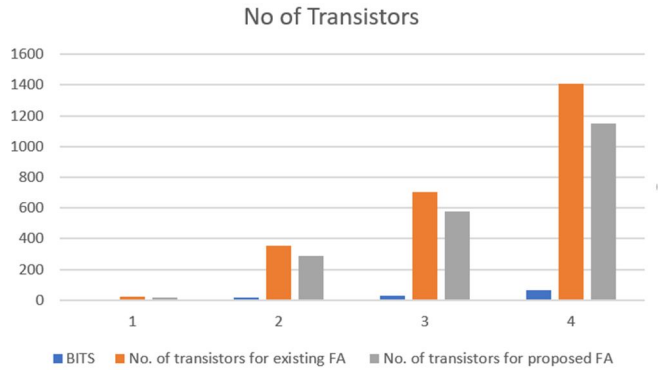


Fig.4.2 Comparison of No of transistors between existing full adder [19] with proposed full adder for 1-bit ,16-bit, 32-bit and 64-bits respectively

Bar graphs presented in Figures 4.1, 4.2, and 4.3 provide a comprehensive visual comparison between the existing full adder [19] and the proposed full adder for varying word lengths: 1-bit, 16-bit, 32-bit, and 64-bit. These graphs illustrate the contrasts in power consumption, delay, and transistor counts, shedding light on the performance disparities between the two designs across different bit configurations

In a comparison between the 1-bit existing hybrid FA[19] and proposed FAs, it's observed that the hybrid utilizes slightly more power at 8.83µW as opposed to the proposed design's 8.49µW. Nevertheless, the proposed design showcases a lower delay of 64.53ps in contrast to the hybrid's 83.1ps, and it achieves this with fewer transistors (18 versus 22). On expanding to 64 bits, the hybrid's power consumption increases to 66.8µW, accompanied by a longer delay of 470.94ps due to the incorporation of more transistors (1408). In contrast, the proposed 64-bit design maintains lower power consumption (35.05µW), a comparable delay (64.53ps), and fewer transistors (1152). In conclusion, the proposed full adder outperforms in terms of power efficiency, delay, and transistor utilization, rendering it a promising choice for energy-efficient and quicker arithmetic operations within more extensive circuits.

V. CONCLUSION

In the existing design, the sum calculation within the full adder is accomplished using Pass-Transistor Logic (PTL). However, upon careful assessment of the design's attributes, a strategic shift towards employing 3T XOR logic has been identified as a promising solution to elevate overall efficiency across multiple fronts. The adoption of 3T XOR logic presents several advantageous outcomes. Primarily, it significantly enhances power efficiency by minimizing the count of transistors involved in the logic implementation. This reduction has a direct impact on both static and dynamic power consumption, effectively conserving energy. Furthermore, the arrangement of transistors in the 3T XOR logic introduces a simplicity that translates into a more streamlined and space-efficient layout compared to the conventional PTL designs. This streamlined layout, in turn, contributes to a reduction in overall circuit area, a crucial factor in modern compact and densely-packed integrated circuits. Additionally, the inherent rapid switching characteristics intrinsic to 3T XOR gates play a pivotal role in achieving swift signal propagation. This aspect is especially valuable when considering the high-speed performance requirements of circuits that incorporate cascaded XOR gates, ensuring that computation is expedited. This strategic transition from PTL to 3T XOR logic reflects a commitment to not only improve power consumption and area utilization but also to enhance signal propagation speeds, thus optimizing the full adder's overall performance. By embracing this alternative logic approach, the design endeavours to strike an efficient balance between these vital design considerations while adhering to stringent constraints inherent in modern integrated circuit design.

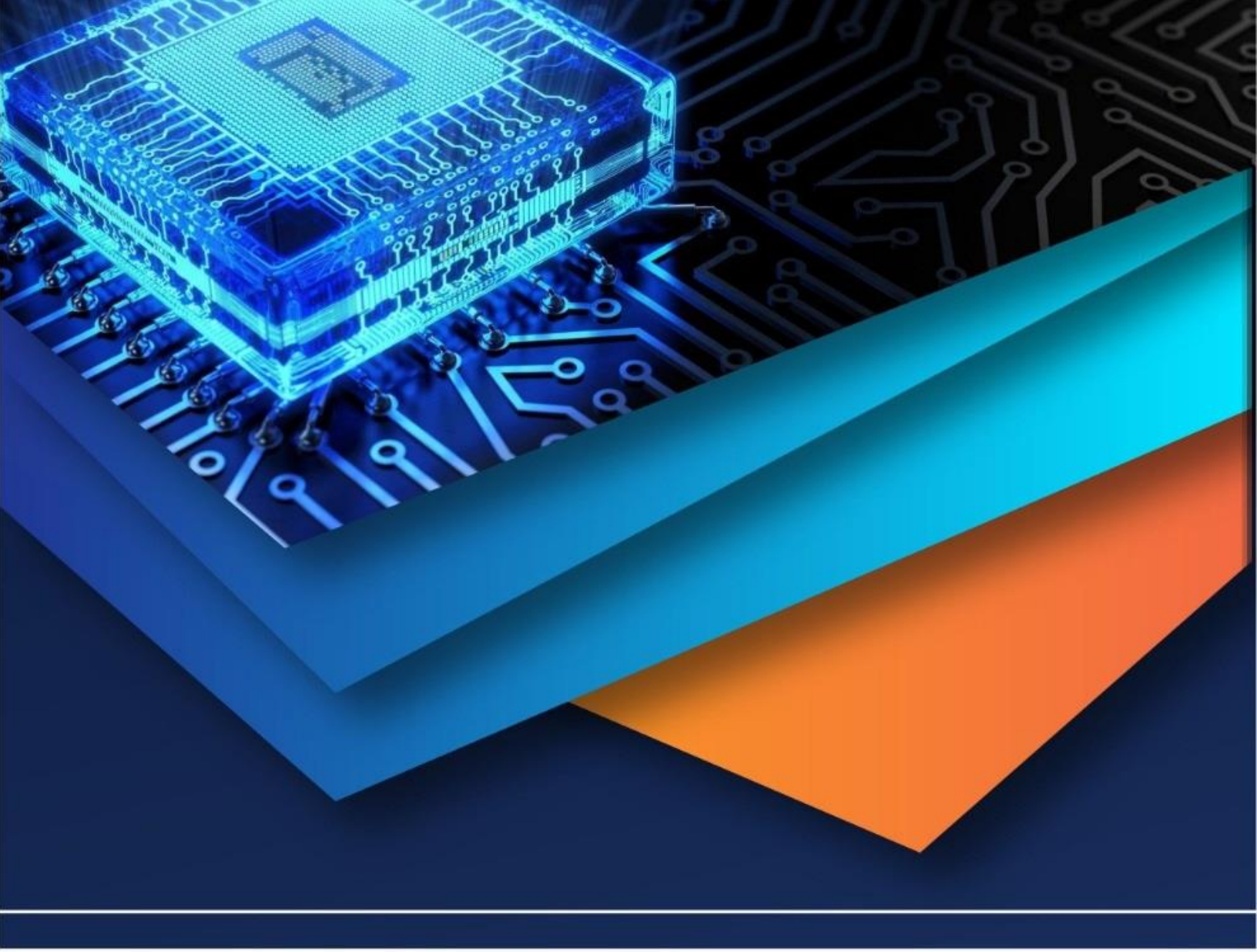
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