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Design of Low Power Double Tail Dynamic Comparator

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Abstract: Dynamic regenerative comparators are being used more and more to enhance power and speed economy in analog-to-digital converters. These converters must be extremely low-power, area-efficient, and high-speed. In this case, the DCs (DC) power is analyzed. A new DC is suggested, modifying the traditional double-tail comparator circuit for quick and low-power functioning even at low supply voltages, in accordance with the analysis that has been provided. Little transistors are added, and the construct is kept simple. Additionally, a new DC in line with on the suggested double-tail topology is provided; this comparator doesn't need a boosted voltage or excessive transistor stacking. Additionally, a latest DC is narrated that it doesn't not require boosted voltage or the stacking of an excessive number of transistors, based on the double-tail structure that has been proposed. Time for Latch delay is greatly decreased by just incorporating a small number of minimum-size transistors into the traditional double-tail DC. Comparing this improvement to the traditional DC and double-tail comparator, significant power reductions are also achieved. The construction of a distinct input and cross-coupled stage is the foundation of the double-tail DC. Fast functioning across a broad common-mode and supply voltage scale is made possible by this separation. This work presents a thorough investigation of DC delays for a variety of topologies. The probe results are validated by the results of simulation in 90 nanometer CMOS technology. It is demonstrated that the DC has a much lower power consumption. At voltage, the comparator's maximal clock frequency is raised to 2.5 Hz, consuming 6.76 μ W in the process. **Index Terms** – Dynamic Comparator, Double tail DC, latch delay, low power operation.

I. INTRODUCTION

The entire dynamic and static power consumption of an integrated circuit can be reduced by employing a range of strategies and procedures together referred to as low power design. Reducing the consumption of power of each individual component is the goal of low power VLSI design, which lowers the overall power consumed. The dynamic power derived from switching and short-circuit power, whereas the static power comes from leakage current flowing along a transistor. Lowering the individual power components as much as feasible will lower the total power consumption, which is the aim of low power design. Both static and dynamic power are included in the power equation. Static power consists of leakage, or the current that passes through the transistor in the absence of activity, whereas dynamic power made up of switching and short-circuit power. A comparators are a building block found in the majority of ADCs. High-speed, low-power comparators with a tiny chip area are necessary for numerous high-speed ADCs, including flash ADCs. Because the devices' threshold voltages supplicant scaled in tandem with the supply voltages of contemporary CMOS processes, high-speed comparators in ultradeep sub micrometer (UDSM) CMOS technologies abide of low voltage supply. Therefore, it becomes more difficult to construct high-speed comparators in low supply voltages. Put another way, in a particular technology, huge transistors are needed to atone for the decrease in supply voltage with focus on achieve high speed. This implies that extra chip space and power are necessary.

Furthermore, a common-mode input range that is restricted by low voltage operation is a significant drawback for several high-speed ADC systems. Comparators typically come in two varieties: voltage comparator and current comparator. While the implementation of circuit are larger and the current comparator requires a voltage converter circuit as an additional circuit, the current comparator uses less power than the voltage comparator. The comparator's drawback is its static power dissipation, which causes the comparator's power consumption to rise.

The suggested comparator has less static power dissipation, which makes static power insignificant and increases comparators' efficiency while using less energy and power. To instigate these constraints of low-voltage design, other strategies have been developed, including supply boosting, body-driven transistors, current-mode design, and dual-oxide processes. These strategies can withstand greater supply voltages.

To solve input-scale and these switching issues, two methods based on increasing the reference, supply or clock voltage are called bootstrapping and boosting. In spite of efficacy of these techniques they have problems with dependability, particularly in UDSM CMOS technology.

Blalock's body-driven approach eliminates the essential for a threshold voltage, allowing body-driven MOSFETs to function as depletion-type devices.

Although the body-driven transistor has advantages over its gate-driven cousin, it has a lower transconductance, and unique fabrication techniques, like deep n-well, are needed to enable both n-channel metal oxide semiconductor and p-channel metal oxide semiconductor transistors to function in the body driven set up. In addition to technology advancements, creating novel circuit topologies that prevent excessive transistor stacking across supply rails is ideal for low-voltage operation—especially if doing so doesn't add to the circuit's complexity. The traditional DC is enhanced with extra circuitry to increase comparator swiftness at lower voltage supply.

The construction of a distinct input and cross-coupled stage is the foundation of the DT-DC. Fast functioning across a broad common- mode and supply voltage scale is made possible by this separation. This work presents a thorough investigation of DCs' delays for a variety of topologies.

Additionally, a new DC is outlined that doesn't need boosted voltage or the stacking of an excessive number of transistors, according to the DT structure that has been proposed. Time due to Latch delay is greatly decreased by just incorporating a small number of minimum-size transistors into the traditional double-tail DC. Comparing this improvement to the traditional DC and double-tail comparator, significant power reductions are also achieved.

II. LITERATURE SURVEY

Here is a detailed summary of some of the existing research studies on this topic:

- 1) S. Babayan-Mashhadi and R. Lotfi (2014) proposed in their research paper titled " Analysis and Design of a Low-Voltage Low-Power DoubleTail Comparator," a thorough investigation of the latency of DCs for different topologies. Additionally, a new DC is outlined that it doesn't demand higher voltage or the stacking of an excessive number of transistors, based on the DT design is proposed. Time due to Latch delay is greatly decreased by just incorporating a small number of minimum-size transistors into the traditional DT DC. Comparing this improvement to the traditional DC and DT comparator, significant power reductions are also achieved.
- 2) S. S. Chiwande and S. P. Akarte (2016), present in their research paper titled " Performance analysis of low voltage, low power dynamic double tail comparator for data convertor application," A novel design for a DC that combines the PMOS bulk-driven input differential stage is displayed in this study. The primary benefit is in the reduced power consumption achieved by linking the input signal to the majority of the transistors in the suggested circuit. The consumption of power of the suggested comparator is situated in the nanowatt range. The circuit that is being shown is simulated and designed using standard 180 nm CMOS technology. Post-layout outcome of simulation indicates that the circuit operates at a frequency of 20 KHz and a voltage supply of 0.5 V, consuming only 8.86 nW of power with a 3.5 ns delay time.
- 3) D. Basak, S. M. I. Huq and S. Nath Biswas (2019) In their survey paper titled " Design and Analysis of High Speed DC for Area Minimization," Comparators are fundamental components found in numerous circuits for mixed signal processing and in ADCs. Because of this, it is imperative to increase its speed and power dissipation while maintaining a small chip size because the market for portable devices is growing. In this study, a modified latching comparator is converter has digital encoding and bubble error correction features. Converter has digital encoding and bubble error correction features. As discussed , and its characteristics are juxtaposed with those of standard models from several literature sources. Cadence, a Spectre Circuit Simulator tool, is used to simulate the circuit. The goal is to minimize the chip area while achieving low consumption of power and a low delay profile. The standard feature size is 90 nm.
- 4) A. Khorami and M. Sharifkhani (2018) in their research paper titled "A Low-Power High-Speed Comparator for Precise Applications". There is a low-power comparator shown. Both the latch stage and the preamplifier of this comparator use pMOS transistors as an input[4]. Two distinct local clock generators operate both stages. To make certain that to attain sufficient preamplification gain and prevent excessive power consumption, latch is actuated with a delay during the assessment phase. In the meantime, tiny cross-coupled transistors diminish the input common mode of the latch and raise the preamplifier gain, which powerfully turns on the pMOS transistors (at latch input) and shortens the delay. The suggested structure, in contrast to the traditional comparator, allows us to select the ideal preamplification delay and prevent overpowering.

When $CLK = 0$ and M_{tail} is turned off, the DC works during the reset phase. To provide the beginning condition and possess a legitimatological level throughout reset, the reset transistors ($M7$ – $M8$) pulls both output nodes, $Outn$ and $Outp$, to VDD . During the comparison phase, M_{tail} is turned on and transistors $M7$ and $M8$ are turned off when CLK is equal to VDD . After being precharged to VDD , output voltages ($Outp$, $Outn$) begin to discharge at varying rates according to the matching input voltage (INN/INP). Considering that $Outp$ discharges faster than $Outn$ in the scenario where $V_{INP} > V_{INN}$, the corresponding pMOS transistor ($M5$) will turn on to initiate the discharge of $Outp$ (discharged by transistor $M2$ drain current) when it falls to $VDD - |V_{thp}|$ before $Outn$ (discharged by transistor $M1$ drain current). Back-to-back inverters causing latch regeneration ($M3$, $M5$ Fig. 2). As a result, $Outp$ releases to the ground and $Outn$ pulls to VDD . The circuits function the opposite way if $V_{INP} < V_{INN}$.

This is because only the latch's transistors $M4$ and $M3$ initially contribute to the positive feedback, which is then amplified by transistors $M6$ or $M5$ to initiate full regeneration when the voltage level of 1 output node drops below a threshold. Only slightly is the gate-source voltage of $M4$ and $M3$ affected by the voltage drop because the gate-source voltages of transistors $M6$ and $M5$ are likewise very small at low supply voltages. Because of the decreased transconductance, this causes the latch 1's delay time to increase. Transistors of DT architecture have two tails. Applications requiring little power use of DT comparator devices. To boost the latch regeneration speed in this technique, raise the voltage differential between the output nodes. During reset phase ($CLK = 0$, M_{tail2} , and M_{tail1} are off), transistors $M3$ – $M4$ pre-charge fp and fn nodes to VDD , which consequently results in transistors $MR2$ and $MR1$ to discharge the nodes of output to ground.

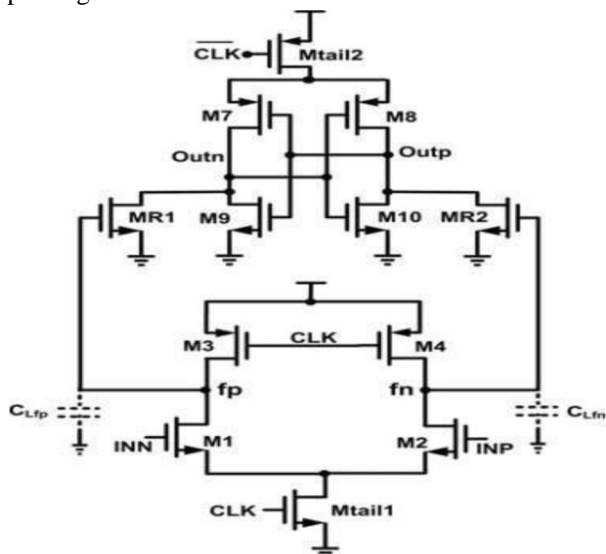


Fig 2: Schematic illustration of the DT-DC

$M3$ – $M4$ switch off, the voltages at nodes fp and fn begin to decline at a rate determined by $I_{Mtail1}/C_{fn(p)}$ during the decision making phase ($CLK = VDD$, M_{tail1} and M_{tail2} turn on), and an input dependent differential voltage $V_{fn(p)}$ will accumulate atop of this. In addition to providing strong shielding between the I/P and O/P, the stage in between made up of $MR1$ and $MR2$ passes $V_{fn(p)}$ to the cross coupled inverters, lowering the amount of kickback noise. Since the fn and fp nodes in this comparator both discharge to ground, both the stage in between transistors have ultimately cut-off, therefore they are of no use in increasing the latch's effective transconductance. While reset phase, these nodes have to be charged from ground to VDD , power consumption.

The pros of the previous architecture included high input impedance, rail-to-rail output swing, no static power consumption, and strong resistance to mismatch and noise [1]. As the output nodes' switching speed is not directly impacted by the parasitic capacitances of the input transistors, huge input transistors could be engineered to minimize the offset. However, the disadvantage is that multiple stacked transistors mean that a respectably large voltage supply is necessary to achieve a suitable delay time. This is because, at first, only the latch's transistors $M4$ and $M3$ participate in to the positive feedback. However, when voltage level of one output node drops below a threshold, transistors $M6$ or $M5$ become active and the full regeneration process begins. The voltage drop has minimal effect on the gate-source voltages of $M3$ and $M4$ because the gate-source voltages of transistors $M5$ and $M6$ are likewise very small at less supply voltages. As a result, the time delay of the latch increases because the transconductances are reduced. To address the shortcomings of the earlier design, the suggested dynamic DT comparator's schematic diagram is displayed in Fig. 3. The suggested comparator is built using a DT architecture because of its superior performance in low-voltage applications.

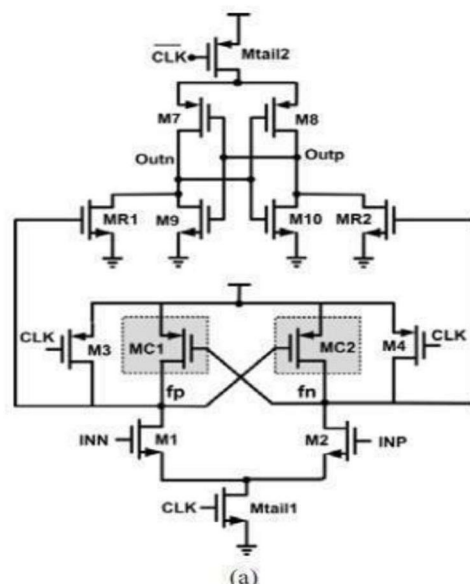


Fig 3: Schematic illustration of the modified DT DC

The 2 control transistors (Mc2 and Mc1) are added to the 1st stage in parallel with the M3/M4 transistors via cross-coupling for the purpose to achieve this. A cross-coupled stage contributes to improved output and input stability. The suggested comparator functions as shown below (Fig. 6). When M4 and M3 pull the fp and fn nodes to VDD 1 during the reset phase (CLK is equal to 0, preventing static power), transistors Mc2 and Mc1 are cut off. The intermediate 29-stage transistors, MR2 and MR1, resets both of the 14 latch outputs to ground. Transistors M4 and M3 turn off during the decision-making phase when CLK is equal to VDD, 1 (Mtail1, and Mtail2 are on). Additionally, since fn and fp are about VDD, the control transistors are still off at the start of this phase. Thus, depending on the input voltages, fn and fp begin to drop at different rates. Assuming $V_{INP} > V_{INN}$, fn drops more quickly than fp because M2 offers a higher current than M1. The related pMOS control transistor (Mc1, in this example) begins to turn on and pulls the fp node back to the VDD so long as fn keeps falling. fn can be fully discharged because the other control transistor (Mc2) is still in the off-state. Considering that initial of the decision-making process, both the fp and fn nodes have been pre-charged to VDD.

V. SIMULATION AND RESULTS

Every circuit has been simulated in a 90nm CMOS technology with $V_{DD} = 1.2$ V to draw a comparison, the suggested comparator with the conventional and DT DC.

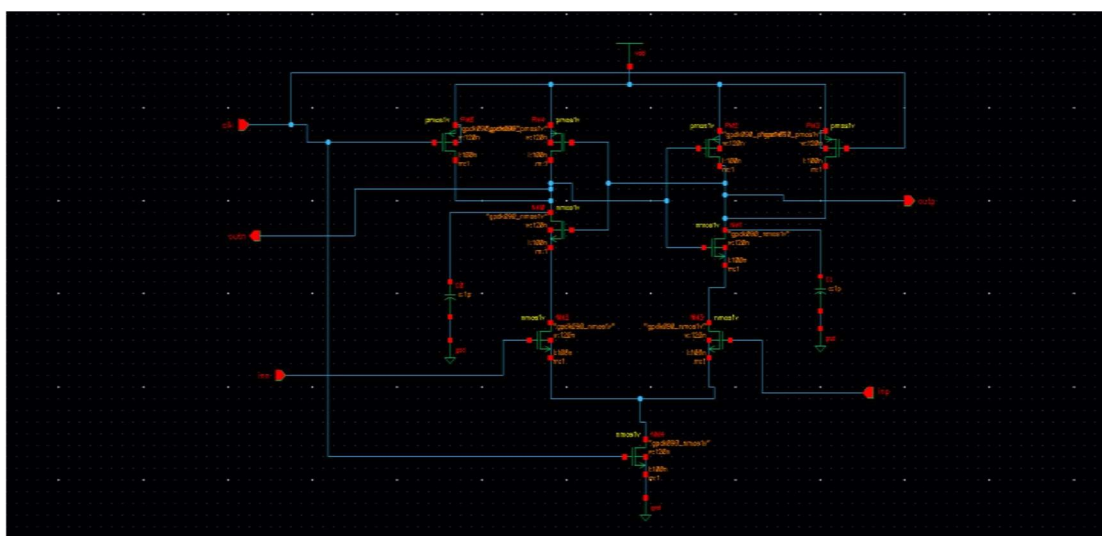


Fig 4: Schematic illustration of the conventional DC.

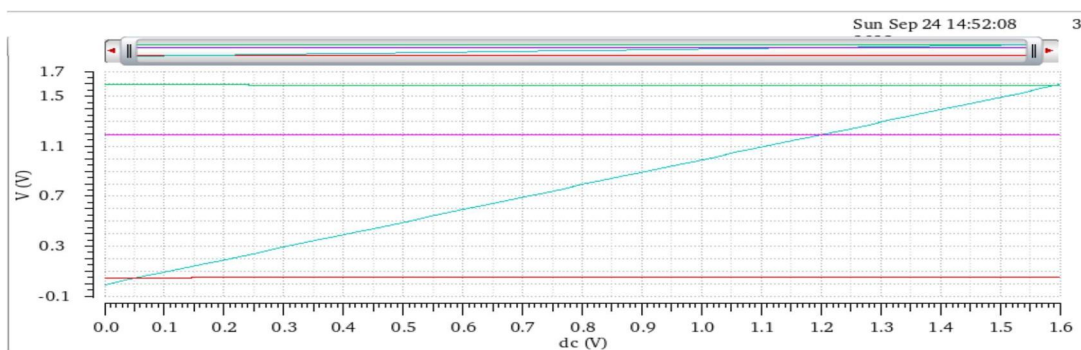


Fig 5: DC analysis for the outn, outp, fn, fp and clock for DC.

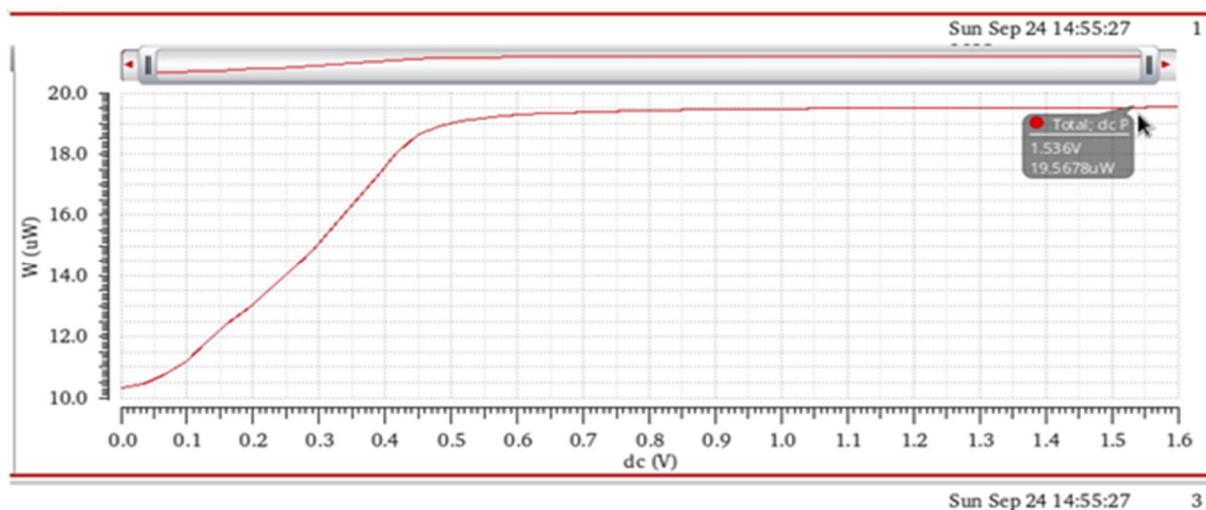


Fig 6: Power consumption for the DC stage .

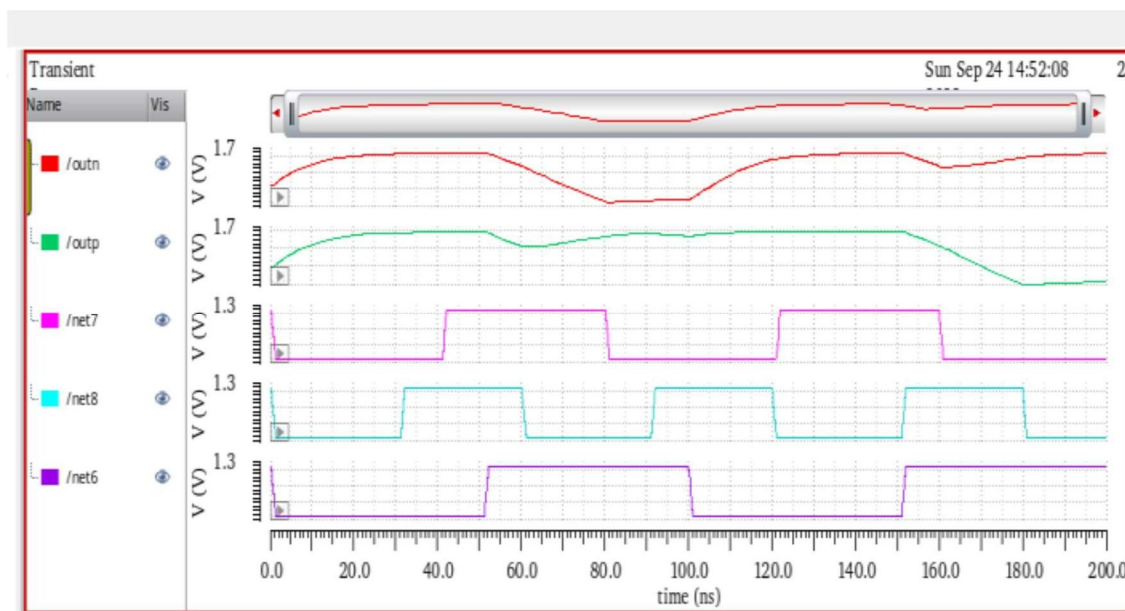


Fig 7: Transient Analysis graph for the outn, outp, fn, fp and clock.

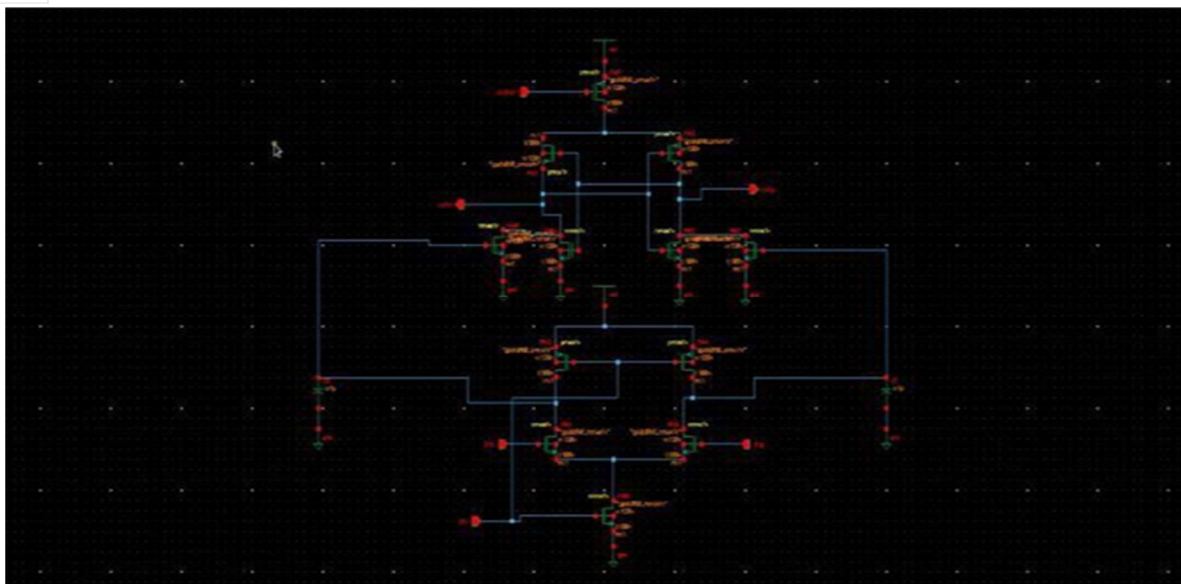


Fig 8 : Schematic illustration of the DT DC.

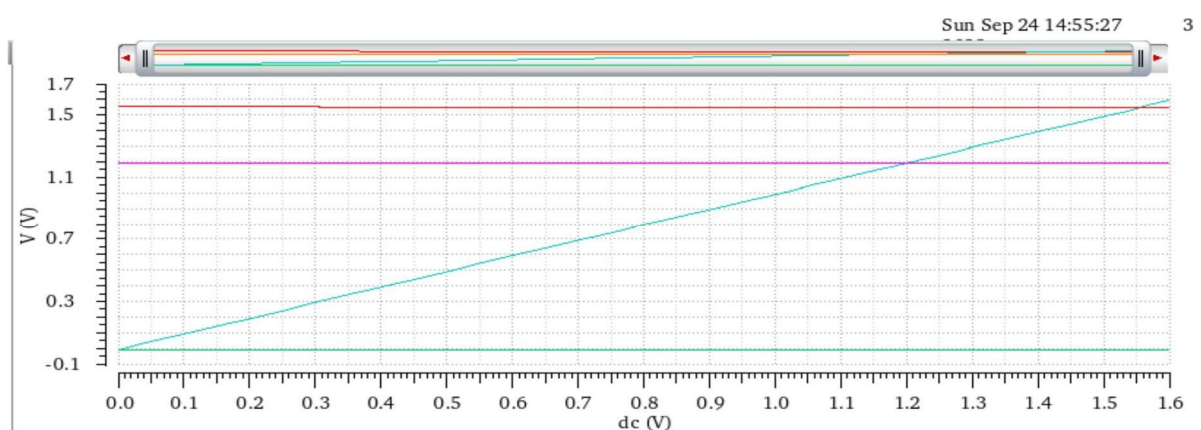


Fig 9: DC analysis for the outn, outp, fn, fp and clock For DT DC.

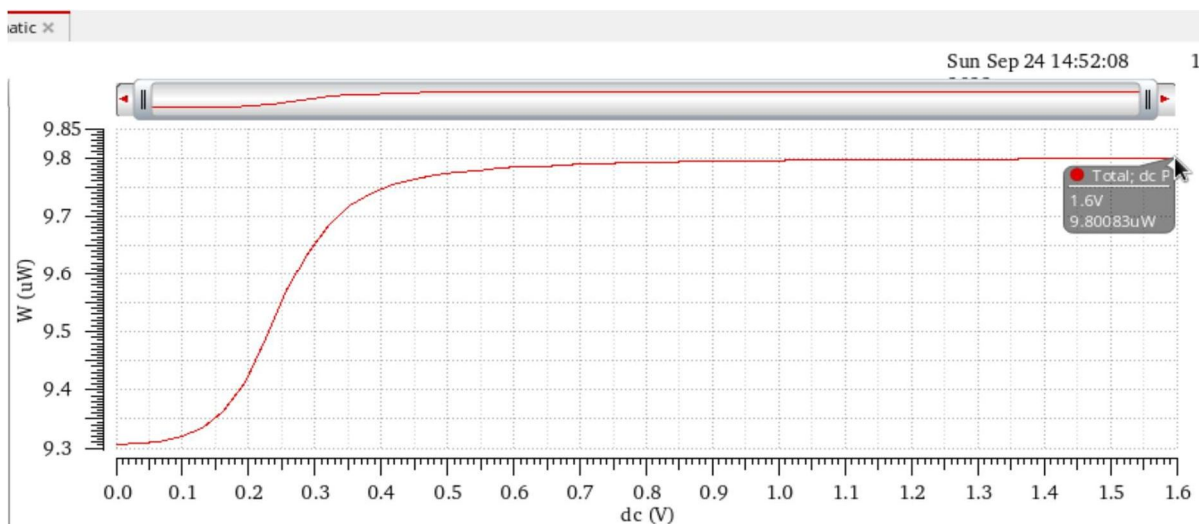


Fig 10: Power consumption for the DT DC stage.

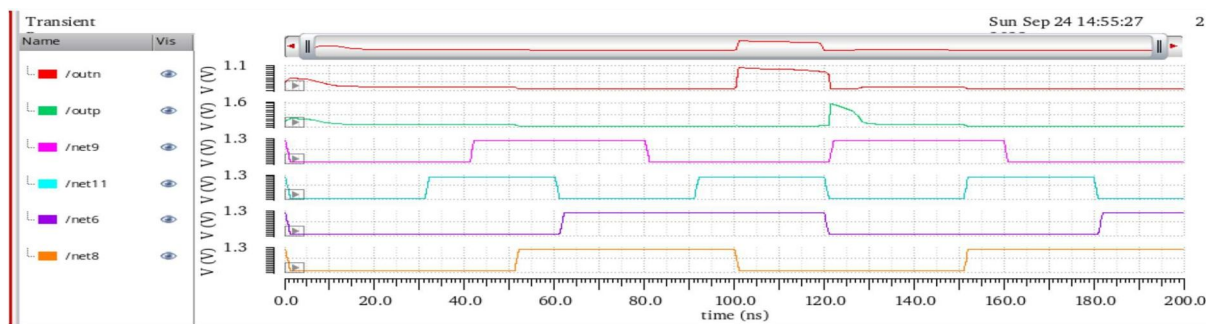


Fig 11: Transient Analysis graph for the outn, outp, fn, fp and clock.

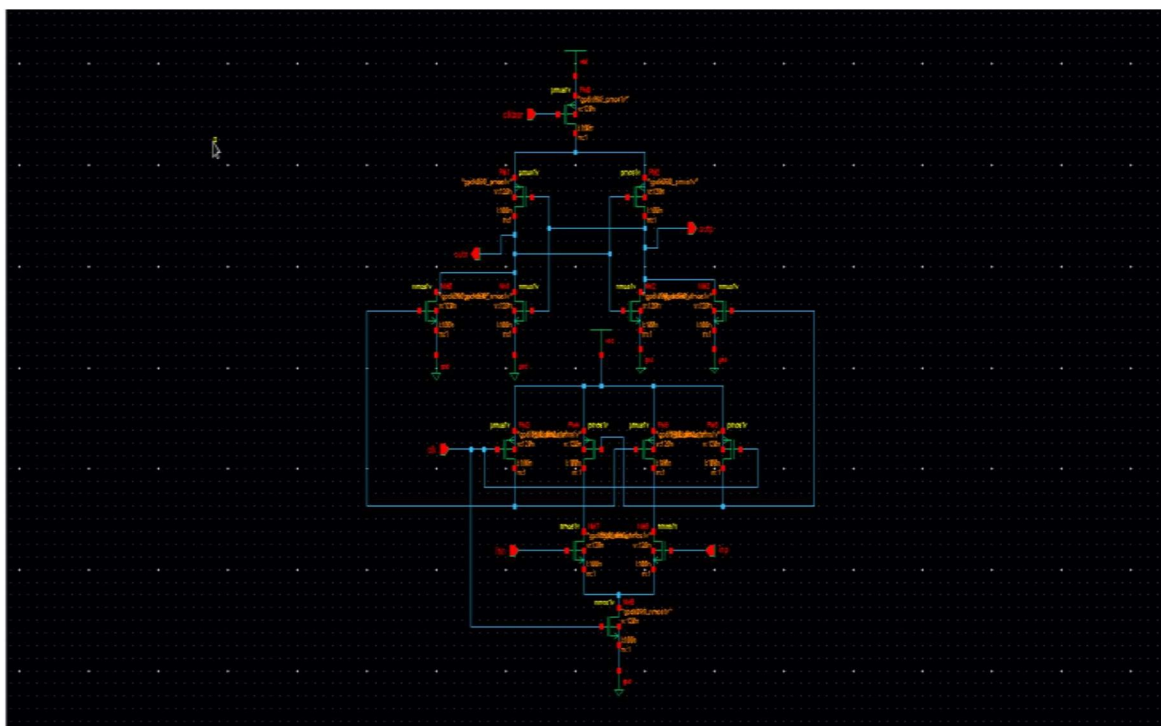


Fig 12: Schematic illustration of the modified DT DC.

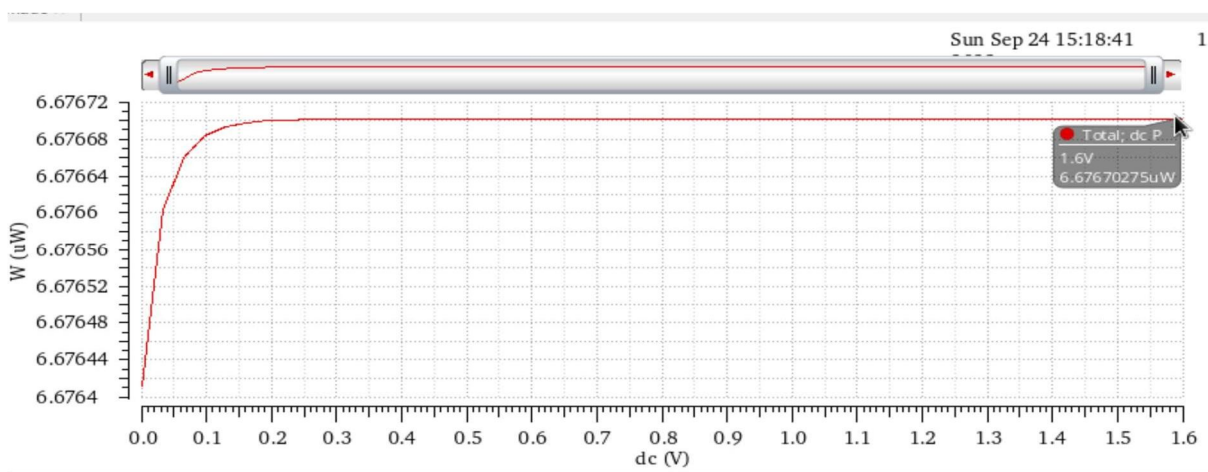


Fig 13: DC analysis for the outn, outp, fn, fp and clock For modified DT DC.

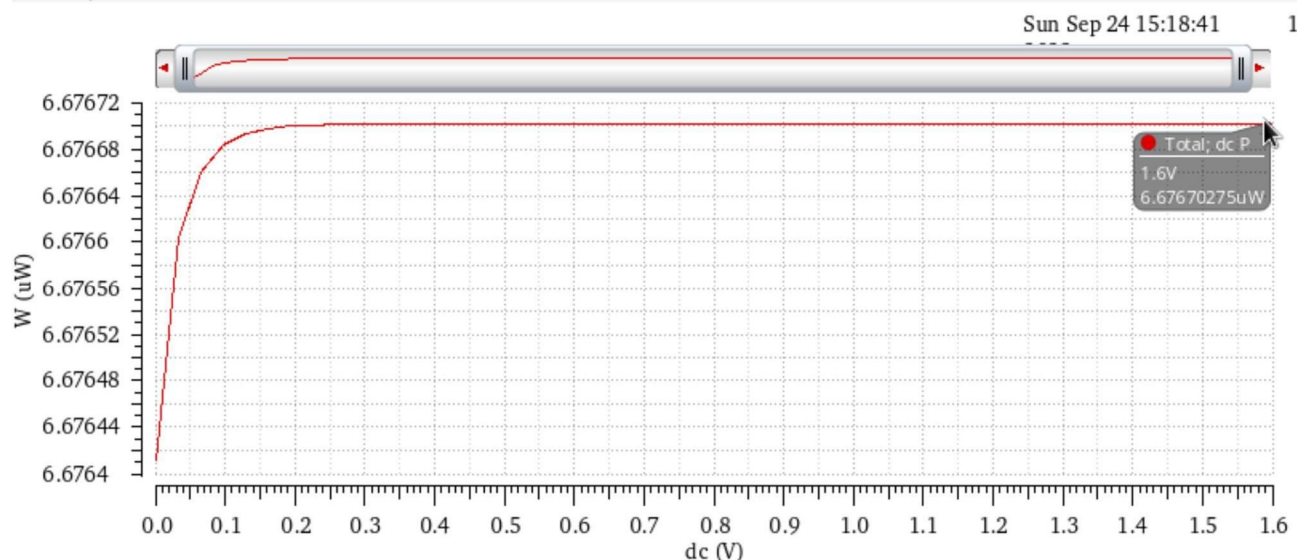


Fig 14: Power consumption for the modified DT DC stage.

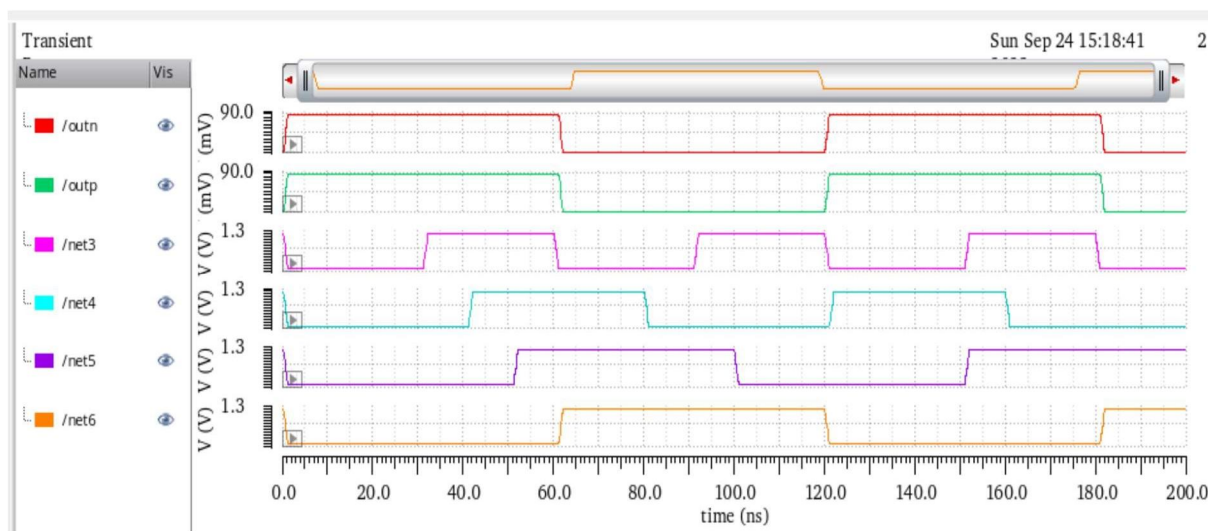


Fig 15: Transient analysis for the outn, outp, fn, fp and clock.

A. Comparator Performance Summary

By analyzing The execution of each stage through the DC and Transient Analysis graph, we have measured power consumption in the 3 stages that has been mentioned in the below table.

DESIGN	Power C Power Consumption at Each Stage
DC Stage	19.56 micro Watt
DT DC Stage	9.80 micro Watt
Modified DT DC Stage	6.76 micro Watt

Table 1: Power consumption in each stage.

VI. CONCLUSION

A thorough power evaluations have been instigated for DCs that are timed. There would be a review of two typical structures: conventional DCs and conventional DT DCs. A single rail in a single tail DC is insufficient owing to the huge power supply. Because DT DC provides big output swing and quick operation with minimal power consumption, single tail DCs have smaller output voltage swing. Power is significantly decreased by just supplementing the traditional DT DC combining a few minimum-sized transistors. Previously, in a DT topology, both the fp and fn nodes should be hauled back up again to the VDD each time they discharge to the ground during the decision-making phase of the reset phase. Among the only one of the aforementioned nodes (fp/fn) must be charged during the reset phase of the redesigned comparator, though. This is because less power was needed because, during the previous decision-making stage, one of the nodes had not been discharged depending regarding the status of the control transistors. Comparing this improvement to the traditional DC and DT comparator will likewise yield significant power savings. Additionally, a significant reduction in consumption of power is required for both of the suggested DCs. To enhance comparator performance, a novel DC with lower power and lower voltage capability is built.

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