iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 9 **Issue:** XI **Month of publication:** November 2021

DOI: https://doi.org/10.22214/ijraset.2021.38727

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 9 Issue XI Nov 2021- Available at www.ijraset.com

Simulation Analysis of Circuit and Designing of PCB Layout of a CMOS based NOR Logic Gate using Open-Source Software eSim

Balakrishna Eppili[1], Probeer Sahw[2], Vanshika Tanwar[3]
[1, 3]*Department of Electronics and Communication Engineering, Dronacharya Group of Institutions, Greater Noida, India*
[2]*Department of Electrical Engineering, Galgotias College of Engineering and Technology, Greater Noida, India*

Abstract: ***There are various basic gates like NAND, NOR gates which are extensively used in the designing of the more complex circuits with use higher number of transistors such as MUXs, ADCs and any other circuits.***
In this paper, we have carried out the modelling of NOR gate at 130 nm technology, yet maintaining comparable performance than conventional CMOS NOR gate logic structure. The modelling includes schematics design and PCB layout design run of the above gates. Also, the simulation results of the gates are obtained at the same node with start time, step time, stop time, rise time, fall time and delay and power dissipation. In this all process have been carried out of a CMOS based NOR Logic Gate using Open-Source Software eSim.
Keywords: Simulation, PCB, NOR, CMOS, eSim

I. INTRODUCTION

We have designed a CMOS (complementary-metal-oxide-semiconductor) NOR gate circuit using a MOSFET p-channel FET (Field effect transistor) and n-channel FET (Field effect transistor). In this CMOS NOR gate circuit uses four MOSFETs, two p-MOSFET which are connected in series and other two n-MOSFET are connected in parallel. The two p-MOSFET taken as Q1 and Q2 and another two n-MOSFET taken as Q3 and Q4, and Vdd1 and GND (ground) are also connected. In this esim circuit designed we are going to do the analysis of 2 input NOR gate using 180nm technology. First input A and second input B which is passing into p-MOSFET and n-MOSFET and output are obtained at Y.

A. NOR Gate Working

1) When input A=low (0) and B=low (0) value is given in p-MOSFET and n-MOSFET: p-MOSFET Q1 and Q2 comes in ON state and also, at a same time Both n-MOSFET Q3 and Q4 comes in OFF state. As Vdd1 connected to p-MOSFET and p-MOSFET comes in ON state and it is also connected in series with P-MOSFET Q2 Hence, Y output get charged to Vdd1 level. Since no path form Y output to GND (ground). So therefore, no discharging and hence Y output will be high (1).

2) When input A=low (0) and B=high (1) value is given in p-MOSFET and n-MOSFET: p-MOSFET Q1 gives a low (0) value so, Q1 comes in ON state and Q2 gives a high (1) value so, Q2 comes in OFF state and at a time n-MOSFET Q3 gives a low (0) value so, Q3 comes in OFF state and Q4 gives a high (1) value so, Q4 comes in ON state. So, in this case Y connected output to GND (ground) through Q4, but no path to Vdd1. So, Vdd1 at Y output gets discharged and output comes as GND (ground) at level low (0).

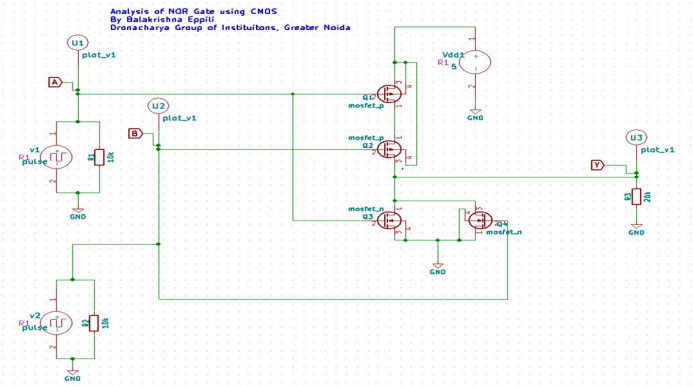


Fig.1. Analysis of NOR gate using CMOS

©IJRASET: All Rights are Reserved

3) When input A=high (1) and B=low (0) value is given in p-MOSFET and n-MOSFET: p-MOSFET Q1 gives a high (1) value so, Q1 comes in OFF state and Q2 gives a low (0) value so, Q2 comes in ON state and at a time n-MOSFET Q3 gives a high (1) value so, Q3 gives a ON state and Q4 gives a low (0) value so, Q4 comes in OFF state. So, in this case Y output connected to GND (ground) through Q4, but no path to Vdd1. So, Vdd1 at Y output gets discharged and output comes as GND (ground) at low (0) level.

4) When input A=high (1) and B=low (1) value is given in p-MOSFET and n-MOSFET: p-MOSFET Q1 gives a high (1) value so, Q1 comes in OFF state and Q2 gives a high (1) value so, Q2 comes in OFF state and at a time n-MOSFET Q3 gives a high (1) value so, Q3 gives a ON state and Q4 gives a high (1) value so, Q4 comes in ON state. So, no path to Vdd1 from Y output to GND (ground). So, Y output will be low (0) level.

A	B	Q1	Q2	Q3	Q4	Y	Logic
0	0	ON	ON	OFF	OFF	Vdd1	HIGH
0	1	ON	OFF	OFF	ON	GND	LOW
1	0	OFF	ON	ON	OFF	GND	LOW
1	1	OFF	OFF	ON	ON	GND	LOW

Analysis of NOR gate using CMOS Truth table

B. NOR Gate Waveform

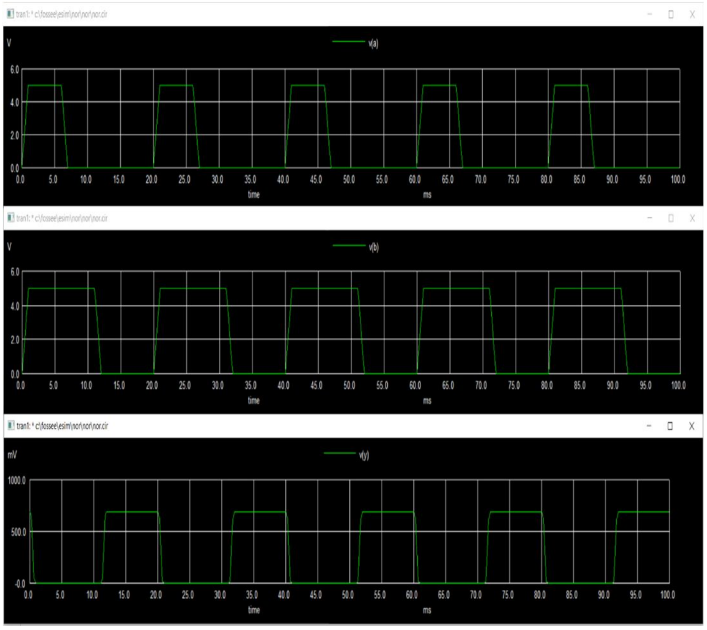


Fig.2. NOR gate NGSPICE waveform

II. SYSTEM DESCRIPTION

Analog signals consist of different infinite value and digital signals consist of different finite values, and it takes only two values low (0) or high (1). Although we have shown low (0) and high (1) as constant levels. Any value in the low (high) band will be interpreted as 0(1) by digital circuits. A digital circuit that accepts and processes binary data (ON/OFF) according to the rules of Boolean logic (AND, OR, NOT, NAND, NOR, XOR, and XNOR).

A group of compatible ICs with same logic levels and supply voltages fabricated for performing various logical functions referred as a logic family. Example TTL, CMOS, ECL logic and etc. Digital circuits are made using a variety of devices. And most of the VLSI circuits today employ the MOSFET technology because of the high density, high speed, and low power consumption. It is used in digital circuits to efficiently design technology and electronics devices. Digital circuits allow for data transmission, communication, in converter like serial to parallel converter and vice versa, thermal counter which measures the temperature of people, etc.

©IJRASET: All Rights are Reserved

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 9 Issue XI Nov 2021- Available at www.ijraset.com

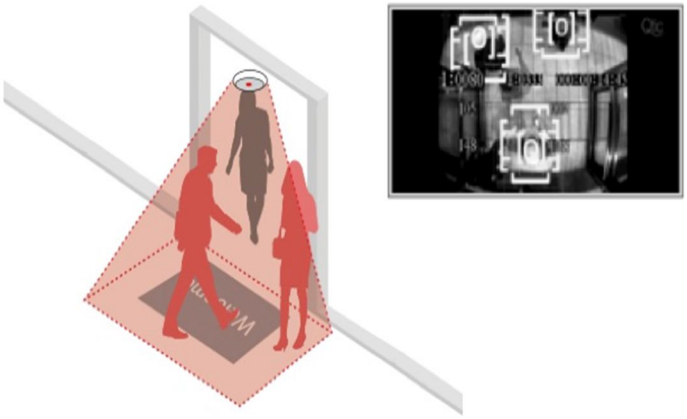


Fig.3. (i). Thermal counter

Fig.3. (ii). digital ICs

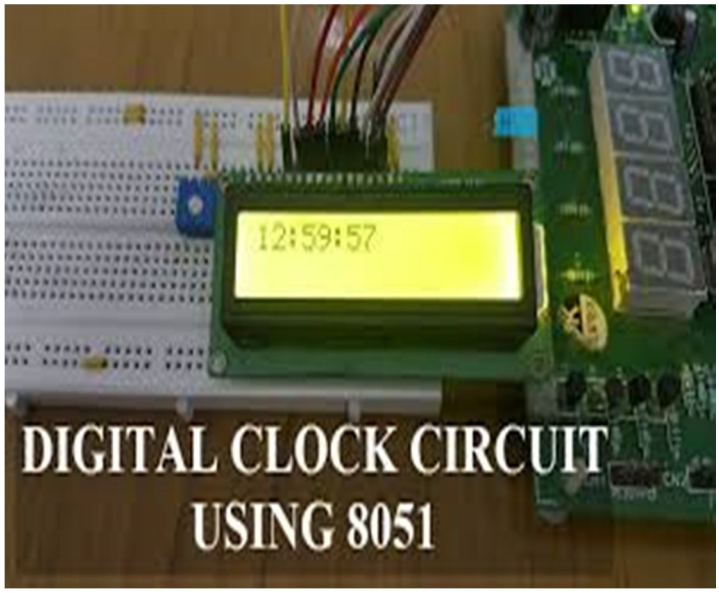


Fig.3. (iii). Digital clock circuit

©IJRASET: All Rights are Reserved

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 9 Issue XI Nov 2021- Available at www.ijraset.com

III. NOR GATE

A NOR gate has two or more input signals but only one output signal. All input has to be low (0) to get a high (1) output. It is combination of OR gate allowed by NOT gate.

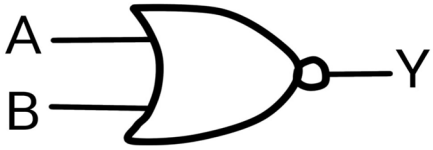


Fig.4. NOR GATE

NOR gate the one of the universal gates.

It is combining NOT gate and OR gate and the output of NOR gate is reversal of OR gate. NOR gate outputs logic high value (1) if both the inputs are at low logic level (0). Mathematical expression for NOR gate operation is given as

Y= (A+B)'

Input A	Input B	Output (A NOR B)
0	0	1
0	1	0
1	0	0
1	1	0

NOR gate Truth table

IV. CMOS TECHNOLOGY

CMOS (complementary metal oxide semiconductor) is a type of MOSFET fabrication process that uses complementary and symmetrical pairs of p-type and n-type MOSFETs for logic functions. CMOS is used as internal implementation for most of the logic gates. The CMOS refers to the typical digital design with combination of p-MOS and n-MOS. CMOS is widely used in electronics industry nowadays. In CMOS technology, both kinds of transistors are used in a complementary way to form a current gate that form an effective means of electrical device.

In this, all the p-MOS device will be together is known as pull-up network and the substrates are connected to the VDD. And all the N-MOS devices will be together is known as pull down network and its substrates are a connected to VSS. The output will be taken at the center as a function of inputs.

A transistor can be thought of as a switch controlled by its gates signal. A p-MOS transistor acts as an inverse switch that is ON condition when the controlling signal is low and OFF condition when the controlling signal is high. An n-MOS switch is ON condition when the controlling signal is high and is OFF condition when the controlling signal is low.

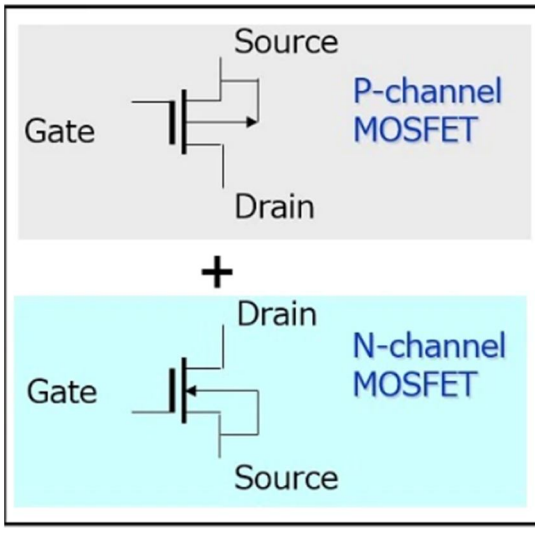


Fig.5. p-channel MOSFET and n-channel MOSFET

©IJRASET: All Rights are Reserved

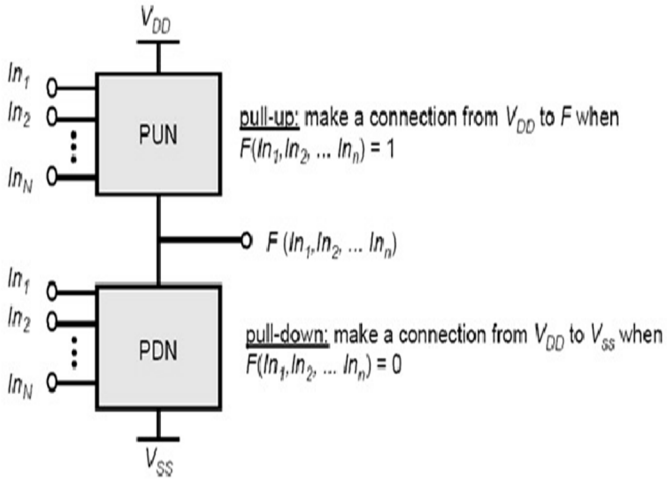


Fig.6. PUN AND PDN network in CMOS

V. REALIZATION OF CMOS BASED NOR GATE

When you open the eSim software then , create new project and take name of the project, then a new schematic window is opened in eSim now as we know that the components which we are using for the realization of NOR Gate are plot, ground, dc voltage(vdd1), PMOS, N-MOS pulse voltage and resistors and also need the global variable then we will select all these elements using place component tool and then connected all these component with each other such that both P-MOS is connected in series and both N-MOS is connected in parallel with other also resistor is connected in parallel with pulse voltage and dc voltage(vdd1) is connected at top and all labels are connected in the circuit now the circuit is completed we have to do the annotation of the circuit then ,check for Erc and Netlist is generated in the schematic then we have to go to eSim environment and click on kicad to Ng spice and enter value of start time ,step time, stop time and then also enter the rise time, fall time, delay time in the source details after that in device modelling add the library of the respective MOSFETs and convert it then do simulation by clicking on simulation tool then waveform is displayed .

Printed Circuit Board (PCB) design is an important step in electronic system design. In every component of the circuit, it needs to be placed and connections routed to minimize delay and area. Each component has an associated footprint. PCB design involves associating footprints to all components, placing them appropriately to minimize wire length and area, connecting the footprints using finally extracting the required files needed for printing the PCB.

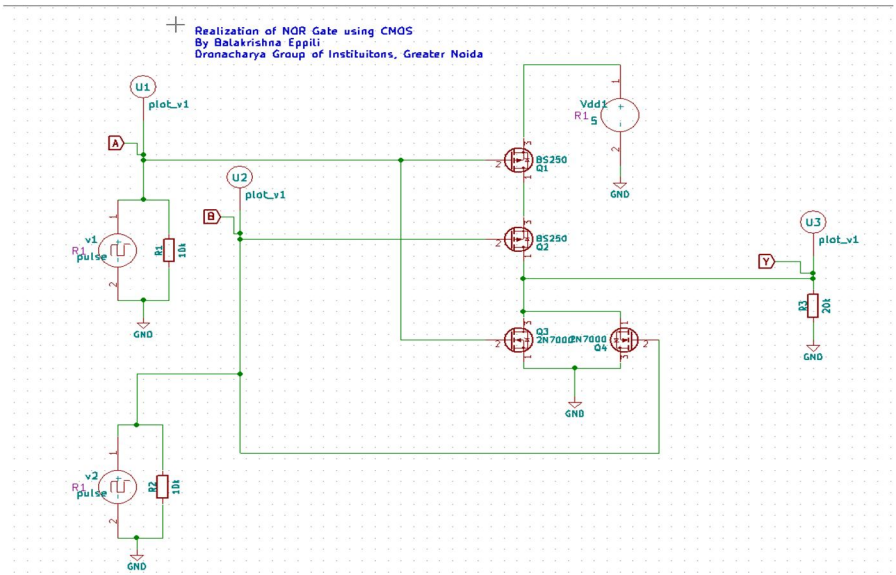


Fig.7.Realization of NOR gate using CMOS

©IJRASET: All Rights are Reserved

VI. SIMULATION RESULT AND PCB LAYOUT

The PCB for a realization of NOR gate using CMOS. A 2N7000(n-MOSFET), BS250 (p- MOSFET), resistor, ground, power and a connector are required. Connectors are used to take signals in and out of the PCB.

The netlist for PCB is different from that for simulation. To generate netlist for PCB, click on the Generate netlist tool from the top toolbar in Schematic. And we have saved it in the same directory in esim folder, do not change the directory or the name of the netlist file. Save the schematic and close the schematic editor.

Once the netlist for PCB is created, then click the run CvPcb to associate components and footprints tool from the top toolbar in mapping. In the tool footprints editors is used for this in this software used CvPcb as its footprint's editor. Then once all footprints are selected in all libraries. Then open layout printed circuit board tool, then after making the border line of the PCB and arranged of all components in a proper orientation without any intersection of wire.

Before doing next step first check that all components' wires have not intersection. Then we have made a track layer in help to B.cu layer. B.cu layer is a back copper layer which is using as track layer. Then the last step which have to follow is we have to add the dimensions in whole PCB so, for adding it select margin in the layer option and then, go to place option then, after that click on dimension now, we have to make a proper line at the border of PCB for measuring its dimension of both length and breadth side of it. Once completed all processes then generate a Gerber file of this PCB.

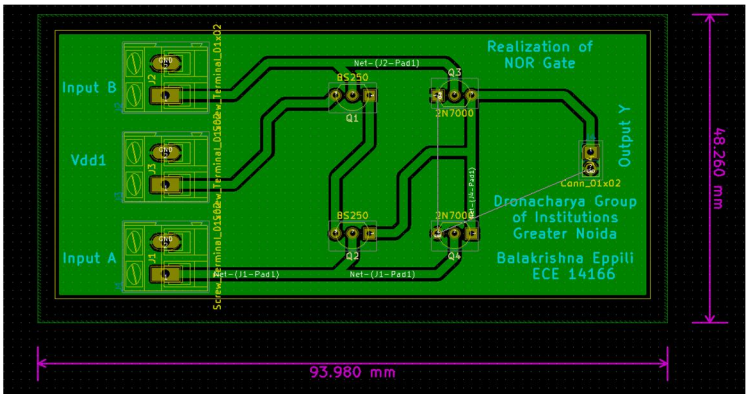


Fig.8. PCB layout of NOR gate

Then we have to generate Gerber files, click on File then Click on Plot. Then open a plotting window option, then we have clicked a plot option then after click on generate drill file once we click generate dill file then the save an esim directory.

Then after all process are completed and save drill fie in this PCB. Then we go to search bar in your window and open command prompt then write a gerbview once gerbview file is open then go to file tool from the top toolbar then select an option there of load Gerber file click on it once and then it opens it in the c drive of your window then open that same path directory where you just saved the drill file and then one by one select a load file in a Gerber file. Then after all process are completed in load file.

Then after that our PCB is ready for the manufacturing purpose in this Gerber file. Then we can take print of this PCB board and finally your PCB is ready.

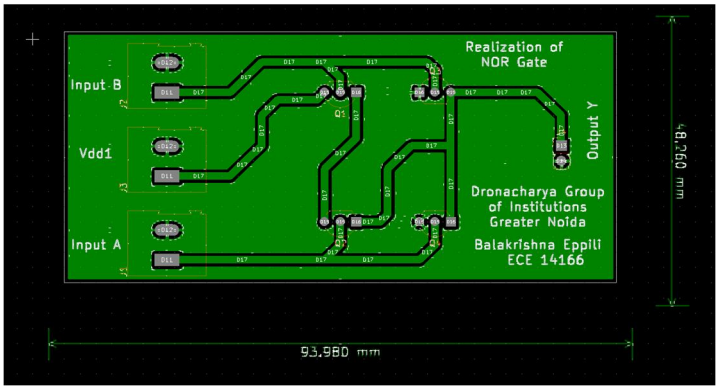


Fig.9.Gerbview of PCB layout NOR gate

This is the whole process of working of NOR Gate in eSim software.

©IJRASET: All Rights are Reserved

VII. CONCLUSION

The paper presents a fully custom hardware implementation of schematics, its simulation and PCB layout design of NOR gate using CMOS in 180nm technology and also, the terms of power, delay and power dissipation. Layout of NOR gate has been designed and simulated using above mentioned techniques for area and power comparison both the layout of NOR Gate have been simulated using 180nm technology. The area and power performance are improved in semicustom design.

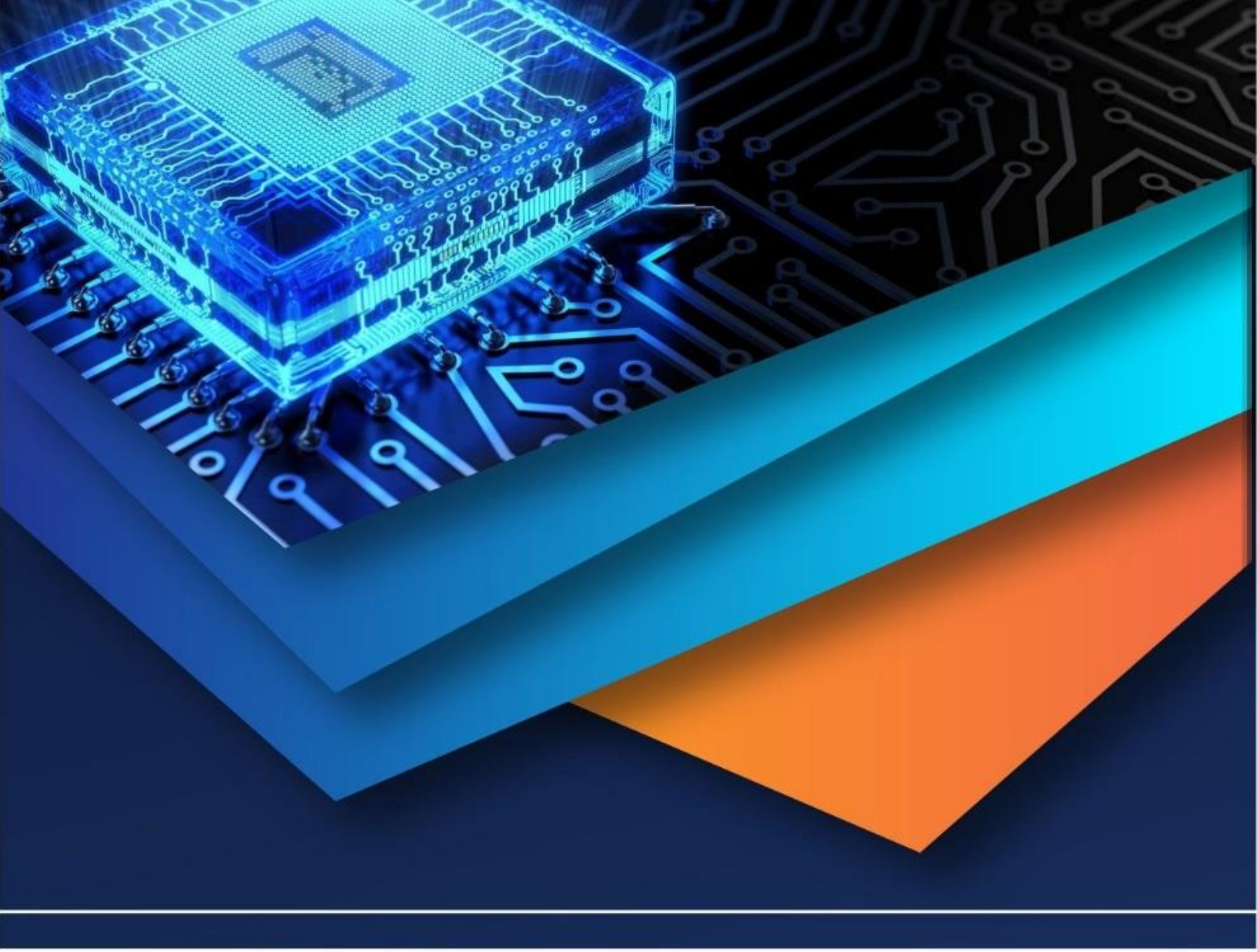
REFERENCES

[1] S. A. Sivakumar. Design of low power alu architecture based on srgdi primitives. http://www.ijaceeonline.com/VOL3ISS4/IJACEE_FPV3I4P1.pdf V. soni and nitin naiyar. Evaluation of logic families using NOR and NAND logic gates. https://studylib.net/doc/18649909/evaluation-of-logic-families-using-nor-and-nand-logic-gates

[2] Balraj Singh, Mukesh Kumar and J. S. Ubhi Analysis of CMOS based NAND and NOR Gates at 45 nm Technology https://www.researchgate.net/publication/316548029_Analysis_of_CMOS_based_NAND_and_NOR_Gates_at_45_nm_Technology

[3] Vibha Soni, Nitin Naiyar Evaluation of Logic Families using NOR and NAND Logic Gates https://studylib.net/doc/18649909/evaluation-of-logic-families-using-nor-and-nand-logic-gates

©IJRASET: All Rights are Reserved



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)