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Development of a CMOS Based on OTA for Bluetooth or WiFi Applications in 65nm Technology

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Abstract: ***In the modern digital economy, the internet is the unifying strand for billions of people, which provides communication and access to information globally. The vast connectivity is largely made possible by wireless communication technologies, which are one of the main driving forces behind the advantages gained in our interconnected world. Harmonized guidelines for mobile devices allow people to use their devices almost everywhere on the planet. Bluetooth and Wi-Fi technologies are the cornerstones of wireless communication, guaranteeing uninterrupted device connections. Operational Transconductance Amplifiers (OTAs) are crucial in circuit design for Bluetooth and Wi-Fi usage as key elements in signal processing. Based on CMOS technology, OTAs offer versatile solutions that are particularly notable for their capability to transform voltage signals into current signals.***

This article provides a high-level design of a cascade current mirror Operational Transconductance Amplifier (OTA) for Bluetooth and Wi-Fi systems, based on a 65nm CMOS technology node. The design works towards improving the overall system performance by emphasizing crucial parameters like gain, power dissipation, area, and group delay. The suggested design lowers power consumption considerably and reduces the chip area occupied, along with lowering the group delay to enhance the responsiveness of the system. A significant gain increase is also obtained, providing enhanced signal amplification and overall performance for Bluetooth and Wi-Fi communication systems. This book showcases the significance of OTAs for maximizing the efficiency and performance of contemporary wireless telecommunication systems and emphasizes their significant role in establishing the next phase of Bluetooth and Wi-Fi development.

Keywords—OTA, CMOS, Current Mirror, Cascade, WiFi, Bluetooth

I. INTRODUCTION

In the mid-1990s, bipolar and GaAs technologies are dominated the control of RF integrated circuits**,**whereas CMOS developments were used chiefly for baseband signal purposes. Nevertheless, when CMOS devices' network lengths were brought down to one micron in the 1990s, the prospect of CMOS RFICs to work over GHz frequencies turned out to be real. Since then, the ongoing shrinking of CMOS device sizes to the current submicron technologies has ushered in a new era for CMOS RFIC designs, such as OTA circuits. The technology has evolved over the last decades from passive devices employed in wireless telecommunication to a broad variety of active filters and VLSI circuits, utilized in applications ranging from high-frequency space engineering to very low-frequency systems. From massive vacuum tubes, the circuits have progressed to micro silicon chips, which are now miniaturizing into the world of nanotechnology. Accompanying this, the need for lower power consumption and supply voltages has increased immensely. Downscaling the circuits has rendered it essential for devices to draw little voltage and power.

Over the past twenty years, handheld devices like laptops and mobile phones have found a place in every day to day life. The speedy technology advancement has led to a greater need for low-power, low-voltage circuits. Since the majority of devices operate on batteries, designing circuits that reduce both supply voltage and current usage has become a necessity.Even a reduction of a slight margin in one or both these factors can highly increase battery duration, enhancing the value of the product and feasibility, particularly for applications that are critical in nature like biomedical systems. Such applications tend to include wireless connectivity across networks such as Bluetooth and WiFi, which involves the use of transceivers. This, therefore, gives rise to the urgent need for transceiver components that can use lower voltages, in synchronization with the ongoing technological needs. With the progress of VLSI technology and microelectronics, the dimensions of semiconductors have reduced, and the requirements of power supply have also decreased in a similar fashion.

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Operational Transconductance Amplifiers (OTAs) are important in implementing these circuits because they possess various useful features, including electronic transconductance gain adjustment, high bandwidth, rapid response speed, minimal power consumption, compact chip size, and minimal supply voltage. In the modern era of wireless communication, technologies like Bluetooth and WiFi are pivotal in the facilitation of seamless connectivity. OTAs play a vital role in enhancing the performance of wireless systems. This research touches on the design and use of OTAs, with their application in adapting to Bluetooth and WiFi environments. With innovative strategies, the research seeks to provide insights into maximizing the efficiency and connectivity of such widespread technologies.

OTAs provide many benefits in WiFi and Bluetooth designs, such as high linearity for precise signal processing, large bandwidth to handle different frequency ranges, low power for prolonged battery life, small size to integrate into circuits, and versatility to handle multiple functions like amplification and filtering. In this paper, we introduce an OTA design based on 65nm CMOS technology in LTSPICE software for Bluetooth and WiFi applications. The OTA is designed to run in the 2.4 GHz range, which Bluetooth and WiFi share.

II. RELATED WORKS

Current research has been aimed at optimizing OTA design for Bluetooth-specific applications, where there has been considerable improvement based on 65nm technology relative to 90nm technology. Kim et al. (2023) analyzed advanced OTA design methods, laying emphasis on power consumption being minimal and linearity being high enough to meet Bluetooth-enabled device needs. Their results provide useful information regarding the optimization of performance parameters of Bluetooth systems, noting that 65nm technology provides improved integration and efficiency over 90nm technology, which results in improved system performance.

Kulej et al. (2022) presented a novel ultra-low-voltage linear OTA structure with a non-tailed differential class AB stage integrated with an additional linear resistor for third-order harmonic component suppression. The proposed structure, implemented in 65nm CMOS, provides high linearity without added power consumption. The OTA has a rail-to-rail input range, with a nominal transconductance of 2.93µS, which can be adjusted from 1.41µS to 5.72µS. 65nm technology is more efficient compared to 90nm technology, with reduced power dissipation and linearity, and hence is more preferable for low-voltage applications.

Shankar et al. (2022) described OTA design with 90nm CMOS for 2.4GHz and 5GHz WiFi applications. They had presented their findings in terms of principal results under the present, group delay, frequency response, phase margin, and power consumption with a 43.26GHz power consumption for both the WiFi bands. By comparison, 65nm technology offers minimized power consumption as well as greater performance because its smaller feature dimension allows for finer optimization in WiFi communication systems, as shown by Li et al. (2022), when they proposed an OTA architecture of WiFi transceivers. The study pointed out enhanced signal integrity and energy efficiency in 65nm designs that surpass 90nm technologies in energy usage and integration for WiFi systems.

Song et al. (2021) presented a 2.4GHz low-power BLE receiver implemented by means of 65nm CMOS technology. The receiver showed good performance with 8.16dB noise figure, 54.5dB conversion gain, and 32.1dB image rejection ratio. It runs on a 2.5mA bias current from a 0.8V supply and has a small die area of 1.65 square millimeters. The design has better performance than comparable designs from 90nm technology in terms of lower power consumption, reduced footprint, and improved efficiency—factors essential for IoT usage.

Hu et al. (2021) introduced a 28nm CMOS Bluetooth Low Energy receiver architecture with 1mW power consumption. They used an inverter-based, inductorless low-noise transconductance amplifier, which improved the performance of the receiver by 1.5/2.5dB at 2/3MHz offset. Their 183.2dB figure of merit and −93.2dBm sensitivity design makes it best-in-class. In comparison with 90nm technology, 65nm brings much-improved power efficiency, noise performance, and overall receiver sensitivity, which is perfect for BLE applications in current low-power devices.

Prasad et al. (2021) suggested a GmC complex filter for Bluetooth wireless receivers with high Image Rejection Ratio (IRR) using fewer stages, increasing the quality factor (Q) of the filter and decreasing power consumption. The design using 90nm technology has an IRR of 55.4 dB. Compared to this, 65nm technology has more power-efficient usage, reduced noise, and greater performance due to its finer geometry, making it more suitable for current applications of Bluetooth where minimizing power loss is important.

In summary, 65nm technology has several benefits over 90nm technology in power efficiency, area reduction, and performance improvement for WiFi and Bluetooth applications. The smaller feature size is beneficial for greater integration, reduced power consumption, and increased linearity, thus making it the best option for modern communication systems, particularly for portable and IoT devices.

III. PROPOSED METHODOLOGY

An Operational Transconductance Amplifier (OTA) is a specialized amplifier that converts voltage signals into current signals. OTAs are used extensively in analog circuit design and are indispensable for applications including filtering, oscillation, and amplification. Their primary features are high gain, broad bandwidth, and minimal power consumption, making them perfectly suited for incorporation into integrated circuits. OTAs have an important role in signal processing applications, especially in communication systems, audio amplifiers, and sensor interfaces. The OTA with the suggested configuration has been designed and implemented in 65nm CMOS technology via LTSpice XVII software. The flow of design methodology

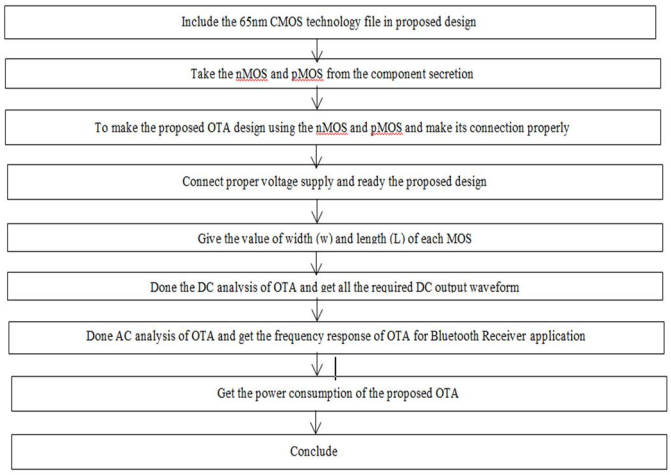

Fig::Design Flow of Proposed OTA Design

For design proposed OTA first include the CMOS 65nm technology file in the LTSpice XVII software after that take the nMOS and pMOS from the component section and make the proper connection of the proposed OTA. Now give the value of W and L to each nMOS and pMOS and done the dc analysis of the proposed design using the DC analysis section. After done the dc analysis done the AC analysis from the ac analysis section and check the power consumption of the proposed OTA design in the ac analysis.

A. Proposed Ota Design And Results For 65nm Technology

Fig. 2 shows the suggested OTA structure, which is organized in terms of the cascade current mirror configuration. This configuration is widely used in Operational Transconductance Amplifiers (OTAs) to provide high gain and superior linearity. In this configuration, several stages of transistors are cascaded in series, with each stage mirroring the current of the preceding one. This facilitates signal amplification with little distortion.

By cascading multiple stages, the overall gain of the OTA can be substantially amplified with high linearity. Moreover, this configuration enhances output impedance matching and stability and is applicable to a wide range of analog signal processing functions, such as filters, oscillators, and amplifiers.

The CMOS OTA design is simulated and verified with LTSpice software and is run within a 65nm CMOS technology environment. The supply voltage is 2.6V for simulation.

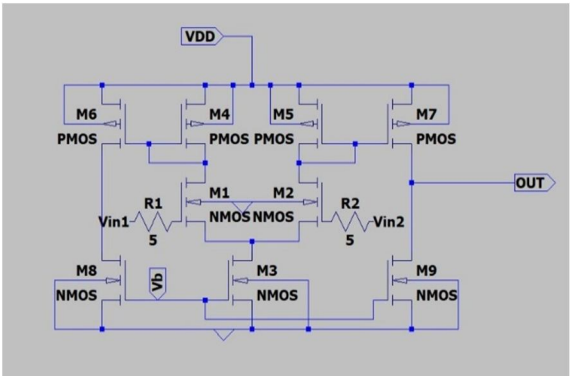

Fig:2 Proposed OTA Design

The width (W) and length (L) of the proposed OTA is displayed in the table 1 and used input parameters for the presented OTA design using the LTSpice software is shown in the table 2.

Table i. Dimension of each transistor for the proposed ota design in 65nm

Transister	Width (W um)	Length(L um)
M6,M7	15.2	0.065
M4,M5	3.6	0.065
M1,M2	16	0.075
M8,M9	13	0.07
M3	26.7	0.07

TABLE 2:Used input parameters for simutation of presented OTA for Bluetooth /wifi application

Parameter	Value
CMOS technology Used	65nm
Power Supply(Vdd)	2.6V
Biasing Voltage(Vb)	0.3V

A. DC Response of a Proposed OTA

In the DC simulation analysis, a resistor was integrated at the output terminal of the OTA in 65nm. The configuration designed for the DC analysis of proposed CMOS OTA is presented in Fig 3.

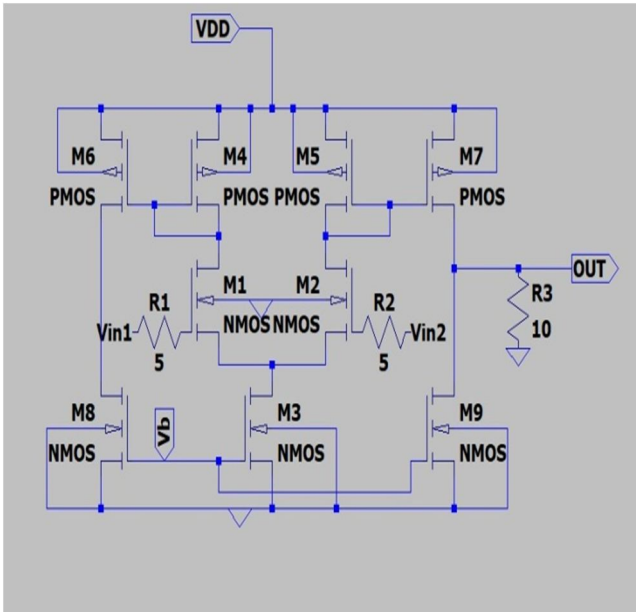

Fig. 3. Proposed OTA Configuration for DC Analysis

The total current range for the proposed OTA varies from 9.58mA to 9.61mA, resulting in an overall current of 0.03mA. The waveform for output current of the proposed OTA in 65nm is depicted in Fig 4.

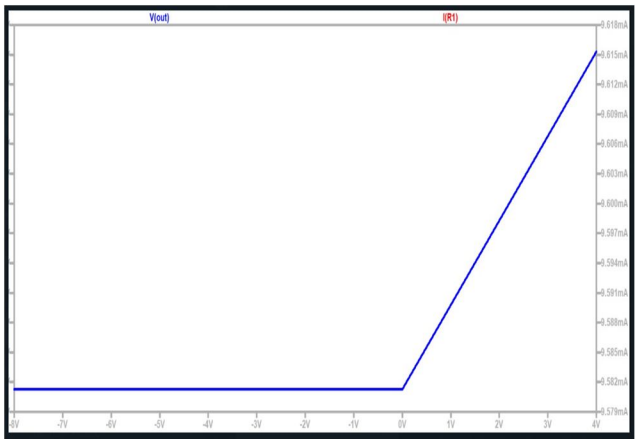

Fig. 4. Overall Output Current of Proposed OTA

B. AC Response of Proposed OTA

To analyze the AC response of the suggested CMOS OTA, a capacitor with a value of 1pF was introduced at the output terminal of the configured OTA. Fig 5 illustrates the configuration devised for the AC response of the OTA.

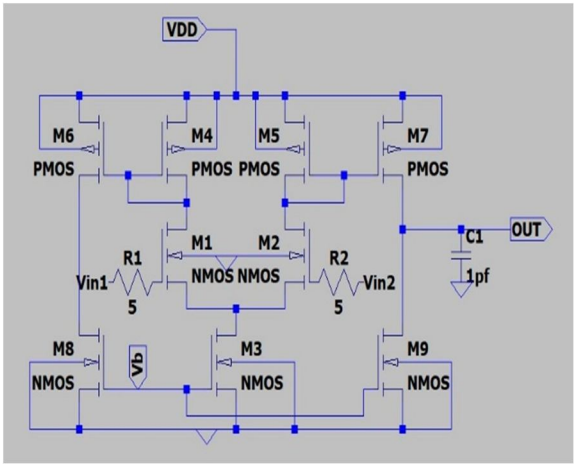

Fig. 5. Configuration of Proposed OTA for 65nm AC Response

The -3dB frequency response of the presented OTA is depicted in Fig 6, illustrating a frequency response at 2.4GHz with a magnitude of -20.09dB, a phase of 111.50°, and a Group Delay of 62.27ps. Table 3 displays the frequency response of the proposed OTA alongside the acquired responses for various parameters.

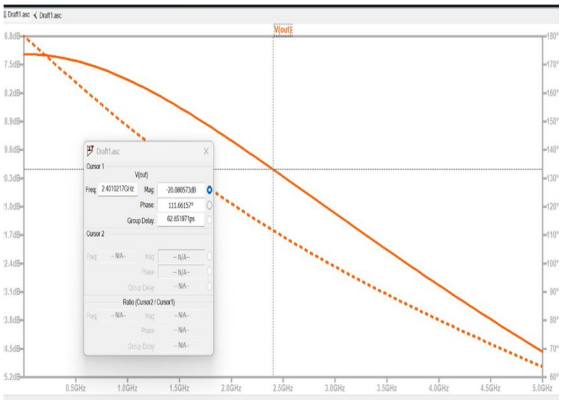

Fig .6. Obtained Response of the Different Parameters and the Frequency Response of the Proposed OTA for Bluetooth/WiFi Application for 65nm

TABLE III. Results Obtained from the AC Response of the Proposed Operational Transconductance Amplifier IN 65nm

Parameter	Value
-3db Frequency Response	2.4GHz
Magnitude	-20.09dB
Phase	111.50
Group Delay	62.27Ps
Power Dissipation	27.09mW

IV. CONCLUSION

The project deals with the important aspect in electronic circuit design: the OTA, and its uses in the applications of Bluetooth and WiFi. The project
studies the integration of CMOS technology with a view to optimizing the performance of an amplifier to sustain efficient wireless communication system operation. Bluetooth and WiFi technologies are commonly employed to link devices, and this paper presents a cascade current mirror CMOS operational transconductance amplifier (OTA) tailored for wireless communication systems operates in the 2.4GHz frequency band.

The new OTA design is realized in 65nm CMOS technology and simulated with LTSpice software under a 2.6V supply voltage. The resulting performance specs for the OTA are a magnitude of -20.09dB, a phase of 111.50°, a Group Delay of 62.27ps, and a power dissipation of 27.09mW. This paper is proof of the feasibility of using the cascade current mirror configuration for improving the OTA's performance as an application to high-speed wireless communication systems, highlighting the relevance of accurate design and simulation as requirements for cutting-edge technology implementations.

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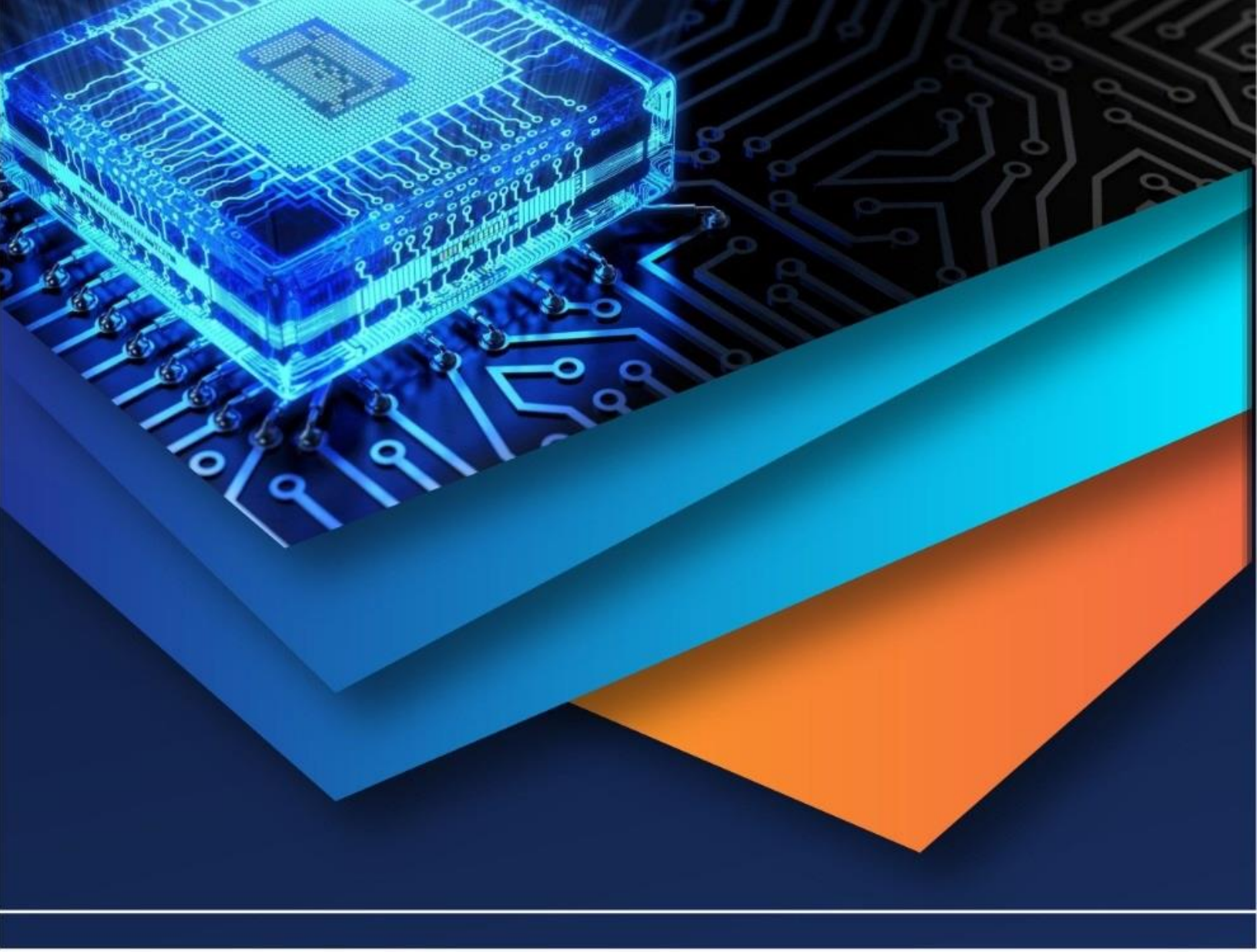

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