iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 10 **Issue:** X **Month of publication:** October 2022

DOI: https://doi.org/10.22214/ijraset.2022.46977

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 10 Issue X Oct 2022- Available at www.ijraset.com

A Comparative Study in Different Topology to Design Push Pull Amplifier for Wide Band Application for Radio and Wireless Communications Systems

Arunendra Nath Tripathi[1], Rajkumar Tiwari[2], Monika Tiwari[3]
[1]*Research scholar, Department of physics and electronics, Dr ram Manohar Lohiya Avadh University Ayodhya Uttar Pradesh*
[2]*Prof.& Ex dean faculty of science, Department of physics and electronics, Dr ram Manohar Lohiya Avadh University Ayodhya Uttar Pradesh*
[3]*Lecturer Rajkiya Polytechnique college Gonda Uttar Pradesh*

Abstract: ***In this paper we present a comparative study of three topology to design push pull amplifier for wide band amplification, and also analysis among these and verify who is best for wide band application is use of radio & wireless communications, we examine topology at different parameters like frequency band width, transients' analysis, power consumption's, noise figure temperature stability etc and their uses.***
Keywords: Push pull amplifier, wild band frequency, temperature stability, RKTG pair, NMOS and NPN transistor Pair, Compound pair of NMOS and PMOS pair.

I. INTRODUCTION

In any radio frequency communication system, power amplifier plays very important role, the main function of power amplifier is provided larger output power at the load to derive all output power devices.[1] For this work push pull amplifier is very popular between researcher and designer and in electronic field because it provided high efficiency without any distortion and larger band width. Push pull amplifier work on the principle of class B amplifier[2]. Last few decades CMOS technology play very effective role in designing R F communications electronics devices because

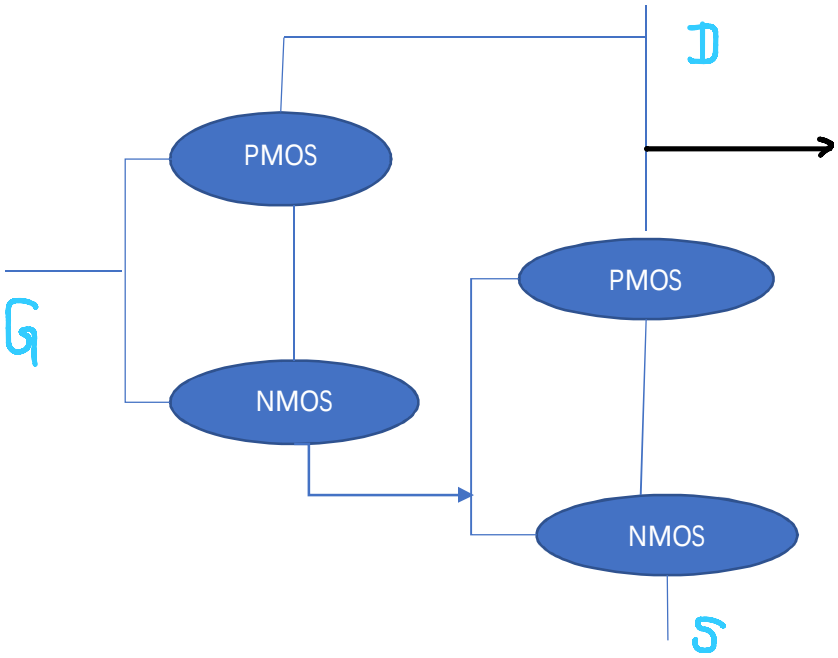
1) Low power consumptions
2) High efficiency
3) Cost Effective
4) Minimum feature size
5) Number of gates on a chip
6) High noise immunity[3]

In modern time latest demand in electronic field amplification at very minimum power consumptions provided better output without any detorsion with high frequency band. To achieve this goal researcher, use many topologies like Darlington pair, Szikali pair, RKTG pair, NMOS and NPN transistor pair, NMOS and PMOS compounds pair and so many other pair which are possible[4].
Among all these possible pair here, we have presented a comparative study among RKTG pair, NMOS and NPN transistor pair and NMOS& PMOS compounds pair, these pair are simulated in 180 nm meter cadence virtuoso software and parameters are same[2].

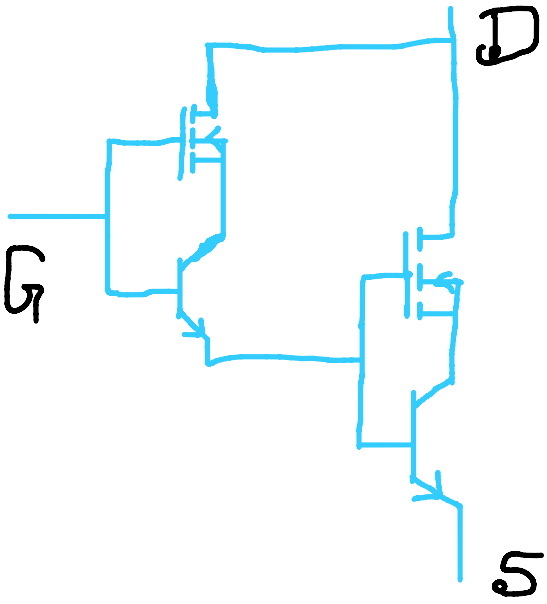
II. COMPARISONS AMONG THEIR PAIR

1) *RKTG Pair:* This pair worked on the principle of complementary compound pair using CMOS technology, RKTG pair is designed with the help of two PMOS and TWO NMOS. It worked on principle that if a complimentary pair consist OF PMOS deriver and NMOS output devices, then the driver act as simple NMOs transistor. And its vice-versa[1].

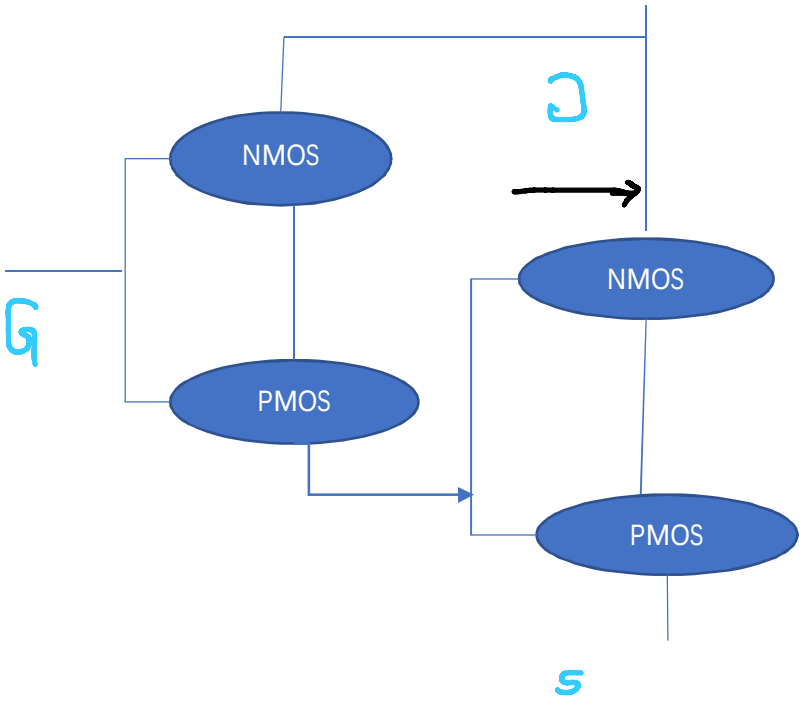
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 10 Issue X Oct 2022- Available at www.ijraset.com



2) *NMOS and NPN Pair:* This pair is designed with the help of NMOS and NPN transistors pair, in this pair NMOS transistor is in driver position and NPN transistor is in it fallower position this combination provided high speed at low power consumptions, their connection model is given below.



3) *NMOS and PMOS Combinations Or MRKTAN Pair:* This pair designed just opposite of RKTG pair and designing principle is same as like RKTG pair, in this pair we change the place of both MOS transistor i.e., where in RKTG pair place PMOS tis is replace with NMOS and vice versa. Is can being easily under stood by below ray diagram.



4) *Comparisons Among Their Circuits& Simulations Results:* Since all these above-mentioned topologies simulated on cadence virtuoso 180 nm technology. If we put all values like input voltage biased resistance input capacitance inductor value at output load resistance output capacitance are same and then we draw a comparison table among their simulation result as shown in below[6-8]

Parameter	RKTG pair	NMOS and NPN transistor	MRKTAN pair
Input frequency	50Hz	50Hz	1000Hz
Input amplitude	1mV	1mV	1mV
Bandwidth	100KHz-6.25ZHz	75Hz-127 PHz	177Hz-77 YHz
Voltage gain	14.8db	36.8db	Less than 1
Power gain	-	-	36.8db
Current gain	-	-	-
Power consumptions	69 mW	36mW	63pW

III. DISCUSSION AND RESULT

By the examine the above result it is found that in radio frequency communication system if want larger voltage gain with bandwidth, we prefer to use design amplifier with the combination of NMOS and NPN transistor but if we focus extra bandwidth with slightly less voltage gain, we use to design amplifier BY RKTG pair but again we find without voltage gain double extra bandwidth we chose MRKTAN pair.

IV. FUTURE WORK

we focus to modify the MRKTAN pair to increase the voltage gain without disturbing the bandwidth and minimize the power loss and tends to zero.

V. ACKNOWLEDGMENT

This work is supported by the grant from the Major Research Project of University Grant Commission (UGC) New Delhi (Project ID.MRP-MAJOR-ELEC-2013-31956). Authors are thankful to University Grant Commission to provide financial support.[10]

REFERENCES

[1] Tiwari, Raj Kumar, Shiksha Jain, and Gaya Prasad. "Complementary Compound Push Pull Power Amplifier for Wide Frequency Band Applications Using CMOS Nanotechnology." In 2020 International Conference on Electrical and Electronics Engineering (ICE3), pp. 402-405. IEEE, 2020.

[2] Arunendra Nath Tripathi, Abhinav Tripathi, Raj Kumar Tiwari, Monika Tiwari, Ganga Ram Mishra, Gaya prasad, "Compound Push Pull Power Amplifier for Wide Frequency Band Applications Using pair of NMOS and NPN Nanotechnology", International Journal of Scientific Research in Science and Technology (IJSRST), Online ISSN : 2395-602X, Print ISSN : 2395-6011, Volume 9 Issue 14, pp. 36-43, May-June 2022.

[3] Tiwari Raj Kumar, Prasad Gaya, Jain Shiksha, Ganga Ram Mishra, Monika Tiwari, Trivedi Parul, "RKTG Pair Amplifier with Gain Boosting Stage", AIJRSTEM 19-106; ISSN-2328-3491@2019.

[4] Tiwari Raj Kumar, Monika Tiwari& Gaya Prasad , "Low Input Voltage High Gain Wideband CMOS Push Pull Amplifier for Tuned High Pass Filter," International Journal of Research in Electronics & Communication Technology, Volume-2, Issue-3, MayJune, pp. 27-31, 2014, © IASTER 2014

[5] Raj Kumar Tiwari, Gaya Prasad, "A New Circuit Model Of Low Voltage High Current Gain CMOS Compound Pair Amplifier" volume 5,issue 4,April 2014,pp.65-71@ IJECET-2014

[6] Raj Kumar Tiwari and Gaya Prasad, "A High-Quality Factor Tuned Amplifier Circuit at High Frequency", Published in Acta Ciencia Indica, Vol. XXXIX, pp.no.01-05, 2013.

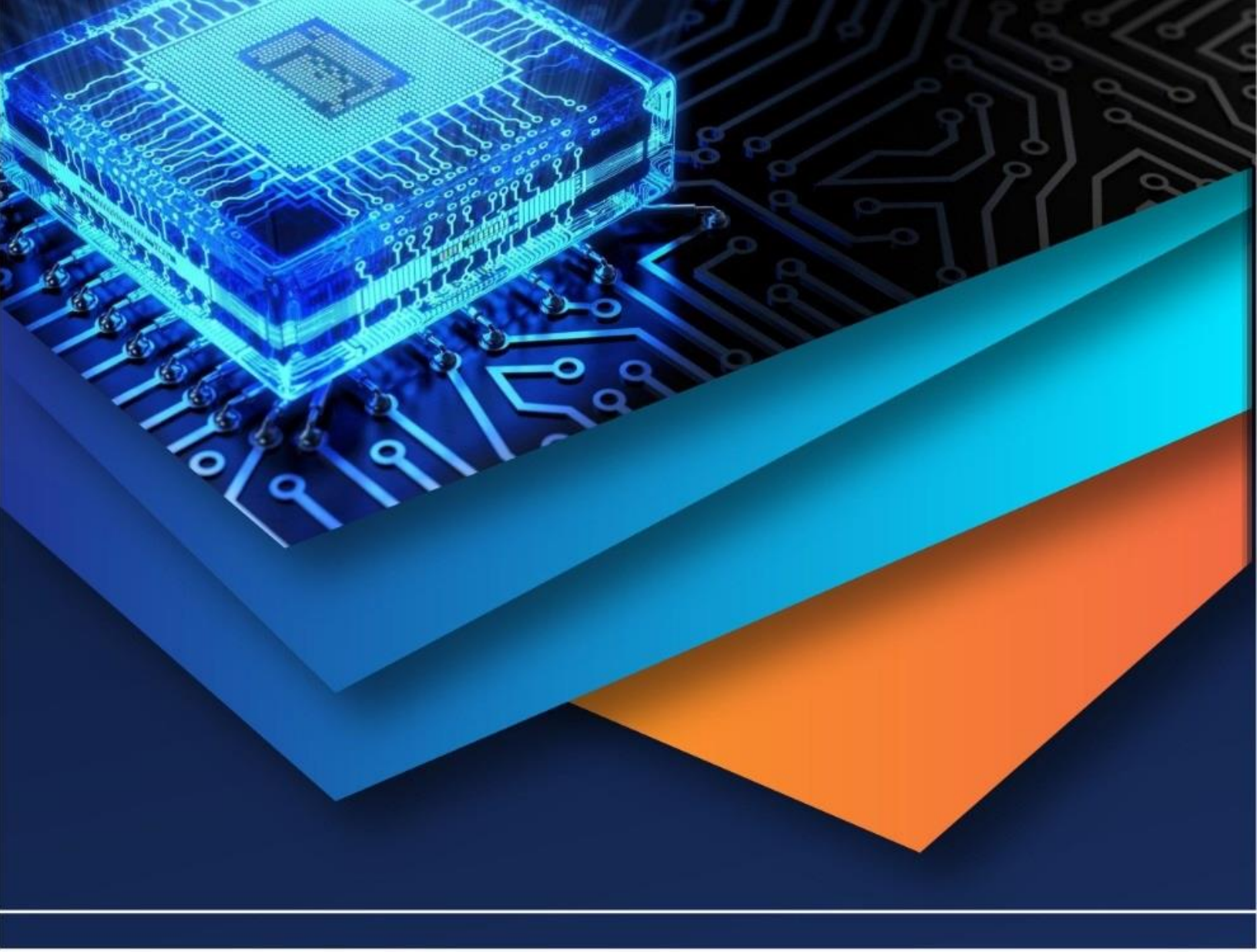
[7] Raj Kumar Tiwari, Gaya Prasad,&Vineet Tiwari, "A Comparative Study of Multilevel Darligton Pair FET amplifier", published in Invertis Journal of science and Technology, vol.6, No.4, pp. 205-210, 2013.

[8] P . Borkhade Gauri , Dr. D. S. Chaudhari, "Ultra -Wideband Low Noise Power Amplifier" International Journal of Advanced Research in Computer Engineering & Technology, ISSN: 2278 – 1323 Volume 1, Issue 4, June 2012

[9] Raj Kumar Tiwari & Jyotsna Mishra, "A New Circuit Model for Distortion less Push-Pull Amplifier" in Bulletin of pure and applied sciences, An International Journal of Physics, Vol.29D(No.1) January-June 2010.

[10] — Shamik Das, Member, IEEE, Alexander J. Gates, Hassen A. Abdu, Student Member, IEEE, Garrett S. Rose, Member, IEEE, Carl A. Picconatto, and James C. Ellenbogen, Member, IEEE _Designs for Ultra-Tiny, Special-Purpose Nanoelectronics Circuits

[11] . Rashmi k. Patil, M.A. Gaikwad, V. G. Nasre, "Area Effect wide sequer range CMOS VCO for PLL in 0.18µm CMOS process", I.T. of Engg. Research and applications (IJERA), vol.2, Jul- Aug-2012 Page1696-1699, ISSN- 2248-9622 -2012



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY