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An effective GDI (Gate Diffusion Input) Based 16- bit Shift Register Design for Power and Area Optimization

Akhila Rayini[1], Rajesh Gogineni[2]
[1, 2]*Department of Electronics & Communication Engineering, Dhanekula Institute of Engineering &Technology, Ganguru, India*

Abstract: ***Sequential circuit design is heavily influenced by power consumption and area reduction. Mainly consisted is shown here. Rather than using flip flops, pulsed latches are used to limit the amount of space these utilize. The shift register uses a minimal number of pulsed clock signals by combining the latches into numerous sub shifter registers and using Multiplexer and additional temporary storage latches. Multiple non-overlap delayed pulsed clock signal schemes are presented for data synchronization in a multi bit shift register to decrease power consumption. In order to maintain the current system, Tanner S-EDIT will be used with Taiwan Semiconductor (TSMC) 0.18mm technology. Designing low-power digital combinational circuits using Gate Diffusion Input(GDI) is a common practice nowadays. When used in particular operating conditions, the GDI approach restores the in-cell swing by implementing sophisticated logic functions on two transistors. This method reduces power consumption, propagation latency, and digital circuit size while maintaining low complexity of logic design. Dual Edge Triggered Flip Flop(DETFF) implementation using GDI technology is introduced as an improvement to the shift register design. This idea also takes into account time restrictions, which can be reduced with the least amount of management.***
Keywords: ***Shift Register, Thermometer Code, Gate Diffusion Input, Dual Edge Triggered Flip-Flop, Propagation latency.***

I. INTRODUCTION

Digital circuits employ a wide range of flip-flops and latches, which have a significant impact on the recycled elemental particles. Today's digital designs incorporate advanced pipelining techniques as well as multiple flip-flops and shift register files that are simple to multiply. A reduction in chip power can be achieved by reducing the clock power used by latches and flip-flops. Other than the D-Flip flop and its variations, such as T-flip flops and JK-flip flops, there are a variety of other, there are slew of new and innovative flip-flop structures to consider. Each of the clock periods two powerful falling edges or rising edges can be triggered by a Single Edge Triggered flip-flop. Due to battery-operated systems' need for low power consumption, high-performance designs with better reliability, custom-sized and low-power configurations have been developed over the past several years. This necessitates designs that use a less amount of electricity while keeping the same level of performance VLSI designers must therefore take into account both space usage and power dissipation while developing their designs. Flip-flops and latches are fundamental storage features in digital design. When utilised in digital circuits, they can have a significant impact on their speed and power consumption. Considerations for lowering power consumption have become increasingly essential in VLSI chip design. Sequential circuits, such as the shift register, are frequently employed for storing and transferring digital data. Shift register is the fundamental building component of VLSI circuits. In a wide variety of contexts, it is frequently employed. Using a shift register has a very basic design. There are M data flip-flops that can make up the M bit shift register. When building a shift register, the smallest flip-flops can be used to save space and power. Information is stored in latches and flip-flops, the most fundamental of electronic components. One latch or flip-flop can hold a single piece of data. “Flip-flops, on the other hand, are only impacted by their inputs for as long as the enable signal is present. This is the major distinction between latches and flip-flops. To put it another way, when they're enabled, the data they're displaying updates instantaneously. Flip-flops alter their contents when the enable signal rises or falls. They are a simple electronic device. The enable signal is frequently the clock signal. Flip-flop content is unaffected by changes in input, whether rising or dropping, because it is a function of the clock edge. When it comes to memory design, shift registers are frequently employed. To design the shift registers, flip flops with edge triggers are used. Clock signals keep all of the flip flops in sync. Adding flip flips to a shift register as its word length grows is a natural consequence. Edge-triggered flip flops have two or more latches in their design. Master-slave latches provide the basis of the flip flop's overall structure. Flip flops in series are used to construct a shift register's internal circuitry. It is possible to create the latches by employing transmission gates in conjunction with combination multiplexer logic cells. There are a succession of synchronised, N-bit flip flops that make up the N-bit shift register's construction, It is not necessary to connect the flip flops in a shift register because there are no interconnected circuits between the flip flops, which means that speed is not a key constraint on shift register design.

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Shift register design is largely void of latches because of their inability to maintain precise timing. In terms of shift register design, the non-overlapping pulse latches are the best choice. It reduces the number of transistors needed for design, which in turn reduces the amount of space and energy used. This research uses pulsed latches to create a low-power and compact shift register. Instead of a single pulsed clock signal, the shift register uses several non-overlapping delayed pulsed clock impulses. Sub shifters and temporary storage assist reduce the number of the clock cycles required by shift register.

II. LITERATURE REVIEW

Jiren Yuan and Christer Svensson - To build Latches and Flipflops with the least delay and power consumption, the TSPC approach was proposed in 1996. A non-transparent input state of the unlatched slave can be safely allowed to reach the "latched" master output without causing any problems. It is sufficient for the "latched" master to have a single isolated output state that is identical to the slave's opaque input state. The biggest disadvantage of this approach is the increased amount of leakage current. Manjit Borah, Robert Michael Owens, and Mary Jane Irwin In 1996, CMOS circuits with alternative transistor scaling approaches were used with power, time, and area optimizations.. Increasing the width of the transistor closest to the power/ground node in long series chains may result in a speed increase and a reduction in power consumption. A typical high fan-out gate does not benefit from tapering since The gate's overall source/drain capacitance is less than or equal to the capacitance of the entire load. The complexity of the hardware, the lack of interoperability, and the increased cost of implementation are the methods' bottlenecks.

Z. Luo, A. Steegen, M. Eller, R. Mann, C. Baiocco, P. Nguyen, L. Kim, M. Hoinkis, V. Ku, V. Klee in 2004 developed Transistors using cutting-edge 65nm Low-power, long-life CMOS technology. NMOSFET and PMOSFET performance increased significantly when plasma nitrided gate oxide and off-set spacers were used in conjunction with low temperature MOL processes. This method's primary flaw is the higher level of complexity that results in tolerable output. Andrea Bevilacqua, Christoph Sandner, Andrea Gerosa, and Andrea Neviani, A low-power, low-noise amplifier was developed in 2006 The ladder input network has two sections, each with a lower voltage and lower current. Digital 0.13-millimeter complementary metal oxide semiconductor technology was used to achieve a 1-dB compression point of 6 dBm, a peak power gain of 9.5 percent, a minimum noise figure of 3.5 percent, and an input-referred gain of 0.8 percent. In this design, the key downside is the high hardware cost with a modest fan output. Emmanuel Bouhana, PatrickScheer, Samuel Boret, Daniel Gloria, Gilles Dambrine Utilizing MOS transistors technologies from 130nm to 65nm, a substrate impedance network was devised in 2006 that could be scaled up or down depending on power requirements. In this notion, compatibility and throughput are two of the main bottlenecks. Chun-Cheng, LiuandSoon-JyhChang, The Monotonic Capacitor Switching Procedure (MCSP) was used in 2010 to create the SAR analog-to-digital converter (ADC) with active low area and figure of merit. The common-mode voltage progressively drops to zero during the switching process. Signal-dependent offset induced by common-mode voltage volatility can be reduced with a better comparator. Among the system's shortcomings are its complication and lack of precision. Xin Zhang, Po-Hung Chen and Koichi Ishida DMBB zero-crossing detector (ZCD) zero-crossing Detector (ZCD) was introduced in 2014 to improve load current efficiency and stability of the Digital Buck converter (DBC). To regulate voltage, a digital PWM controller is used, and an automatic DCM/CCM controller is proposed to switch between CCM and DCM modes at will.

III. EXISTING METHOD

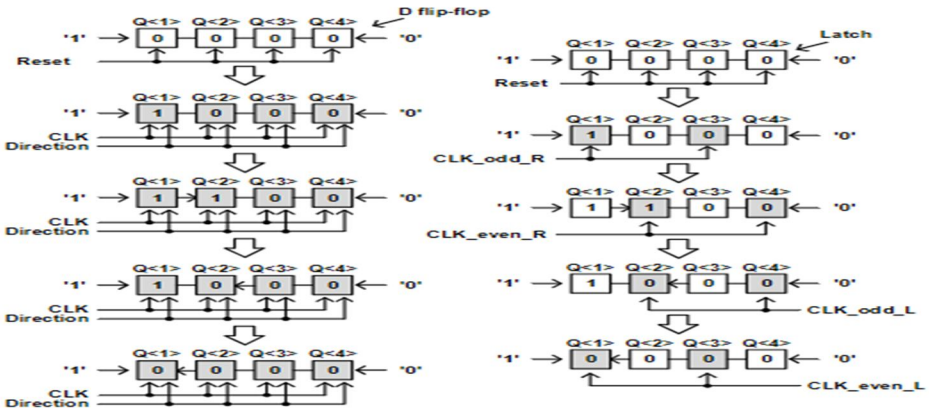


Fig.1.(a) Conventional bidirectional 4-bit D-FF based thermometer-code shift-register (b) Proposed bidirectional 4-bit latch-based thermometer-code shift-register.

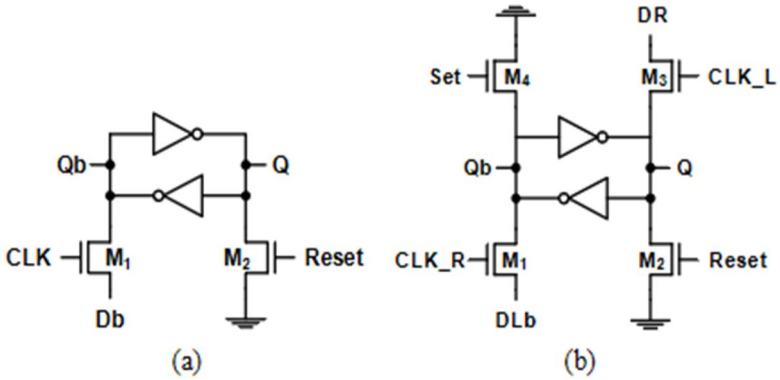


Fig.2 Proposed thermometer-code latches (a) unidirectional (b) bidirectional.

When it is birectional the clock is high (CLK='1') and the inverted data input from the left latch is ground (Db='0'). It resets the latch (Q and Qb) by discharging Q to ground via M2, when the Reset signal is high. The bidirectional latch receives the data '1' from the left latch and the data '0' from the right latch. It updates the data Q to the data '1' by discharging Qb to ground via M1, when the inverted data input from the left latch (DLb='0') is ground and the clock for right-shifting (CLK_R) is high. It updates the data Q to the data '0' by discharging Q to ground via M3, when the data input from the right latch (DR='0') is ground and the clock for left-shifting (CLK_L) is high. It resets the latch (Q and Qb) by discharging Q to ground via M2, when the Reset signal is high. It sets the latch (Q and Qb) by discharging Qb to ground via M4, when the Set signal is high.

Fig.4(a) shows the proposed unidirectional 64-bit thermometer-code shift-register. It consists of a clock signal generator and N unidirectional (UD) thermometer-code latches. The UD latch receives the inverted data output (Qb) of the left latch. The clock signal generator in Fig. 3(a) makes two clock signals (CLK_odd and CLK_even), which enable odd and even UD latches, alternately, as shown in Fig. 1(b). Fig.4(b) shows the proposed bidirectional 64-bit thermometer-code shift-register. It consists of a bidirectional clock signal generator and N bidirectional (BD) thermometer-code latches. The bidirectional latch receives the inverted data output (Qb) from the left latch and the data output (Q) from the right latch. The bidirectional clock signal generator in Fig. 3(b) makes four clock signals according to the direction signal. It shifts the data '1' right or the data '0' left according to two clock signals for right-shifting (CLK_odd_R and CLK_even_R) or two clock signals for left-shifting (CLK_odd_L and CLK_even_L), respectively, as shown in Fig. 2(b).

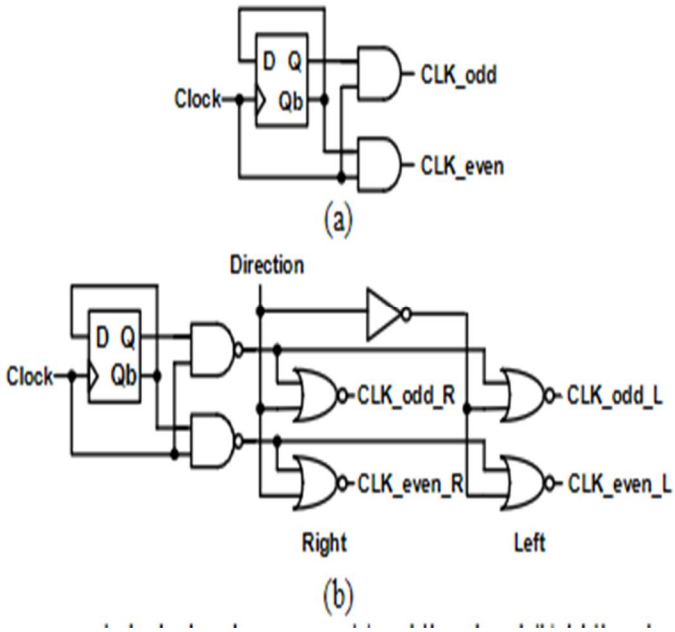


Fig. 3 Proposed clock signal generator (a) unidirectional (b) bidirectional

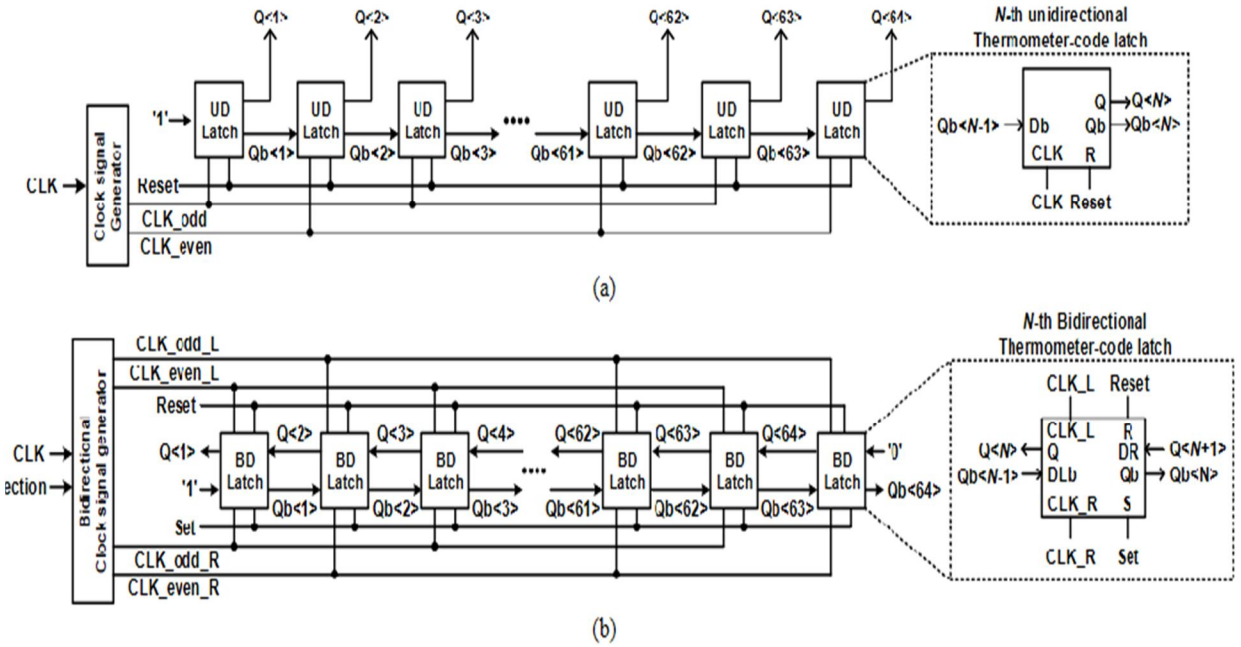


Fig.4 proposed 64-bit thermometer-code shift-registers (a) unidirectional (b) bidirectional.

The bidirectional thermometer-code shift-register shifts the data '1' right with CLK_odd_R and CLK_even_R or the data '0' left with CLK_odd_L and CLK_even_L, according to the direction signal. They shift one bit data per clock cycle by enabling alternately the odd and even latches with CLK_odd and CLK_even, respectively. Therefore, they have the hold time as much as a half clock period. This removes the timing problem among latches.

IV. PROPOSED METHOD

It is possible to reduce the power consumption of a thermometer code shift register utilising the pulsed latch approach, which is an existing way for reducing the power consumption of the thermometer code shift register. In this we can proposed the technique named as GDI based DETFF by using this methodology also can reduce the performance of area and power consumption.

A. GDI Based DETFF

To build low-power digital circuits, Gate Diffusion Input(GDI)employs this method. When used under specific operating conditions, For sophisticated logic operations, GDI's two transistor implementation allows for in-cell swing restoration. A low degree of logic complexity is maintained while reducing digital circuit power consumption, propagation latency and area.
Dual Edge Triggered Flip Flop (DETFF) is introduced as an upgrade to the design of shift registers using the GDI approach. Timing constraints also considered in this concept to reduce with at most management.

B. DETFF Using GDI Based Mux

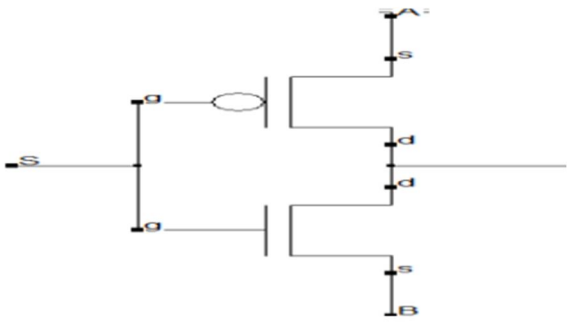


Fig.5 Multiplexer Using GDI

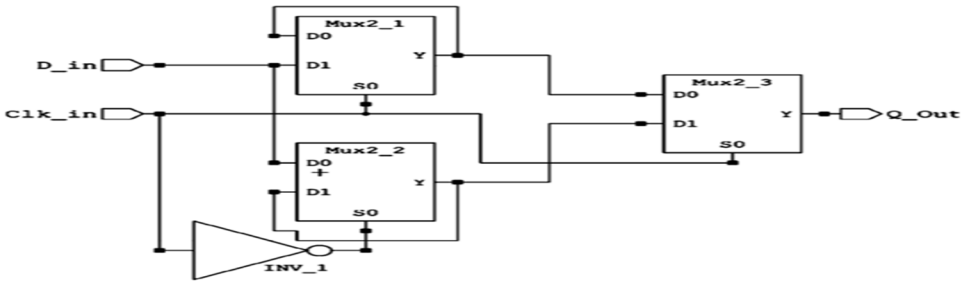
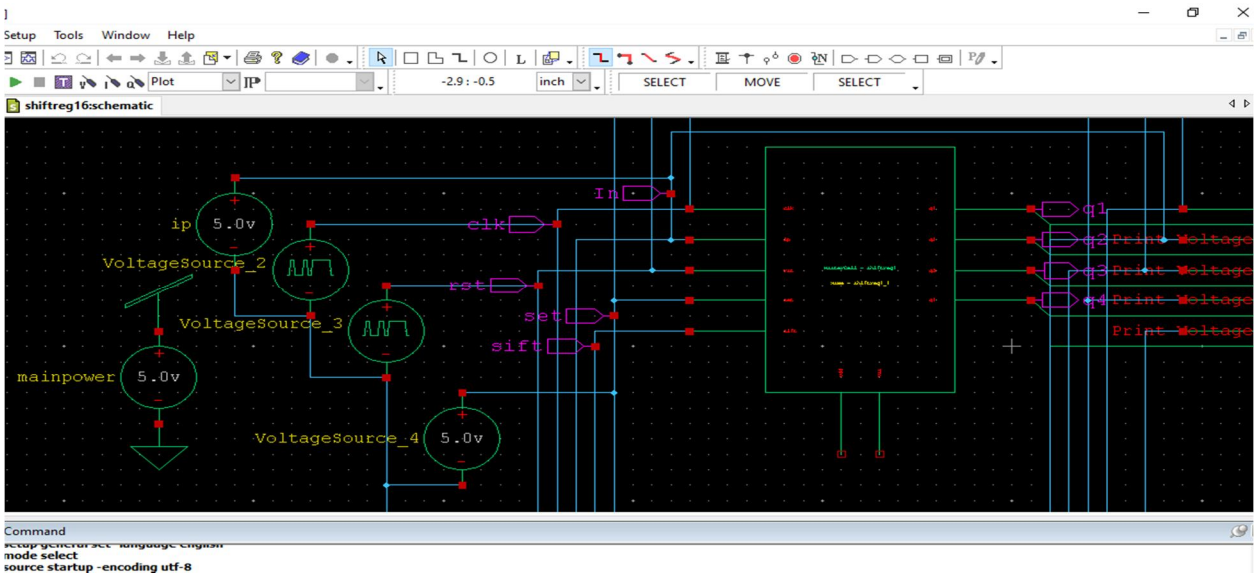


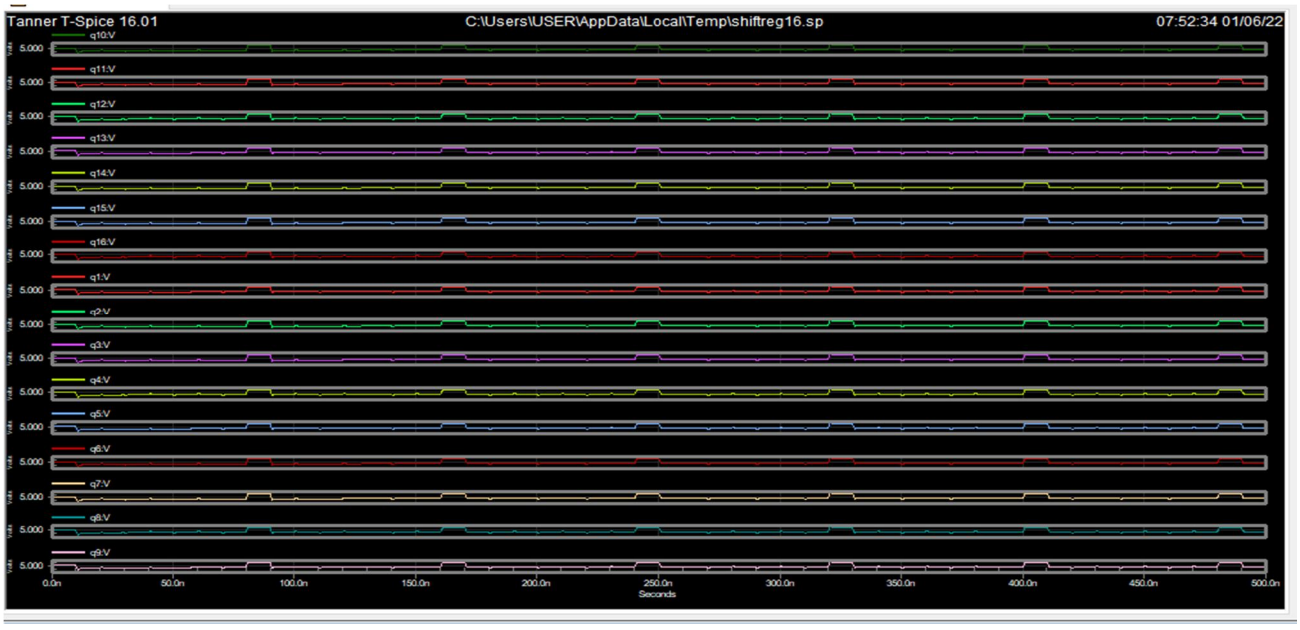
Fig.6 DETFF Using GDI Multiplexers

V. RESULTS

A. *Existing Design*



1) *Output*



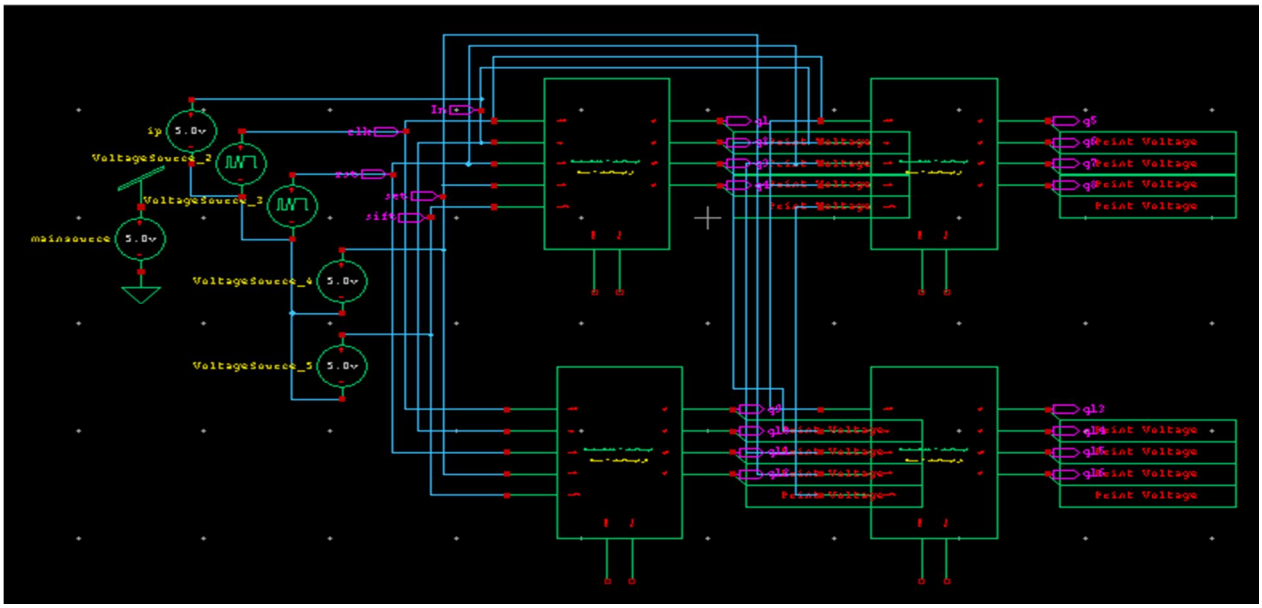
2) Calculation of Power

Vmain power from the time 0 to 50
Average power consumed -> 1.170426e-010 watts
Max power 1.661541e-002 at time 1.0825e-008
Min power 7.920511e-003 at time 8.0425e-008
Total power consumed is: 108Mw

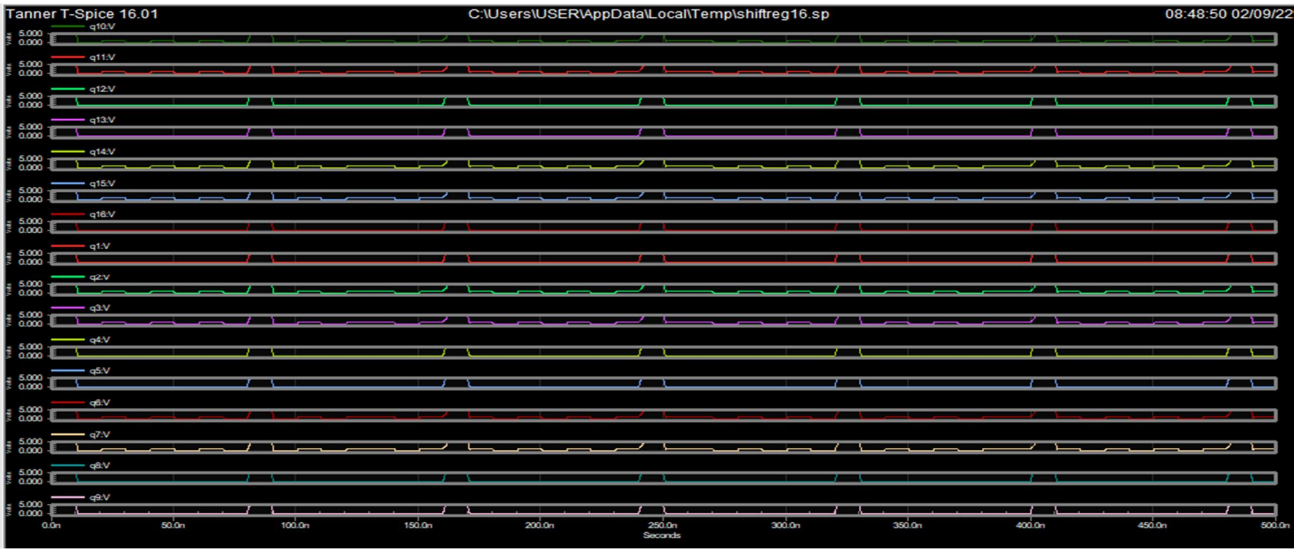
3) Calculation Of Area

Total Nodes = 474*technology (Here we are using Tsmc 0.18)
= 474*18
= 8532/100 = 85.32% in mm

B. Proposed Design



1) Output



2) Calculation Of Power

Vmainsource from the time 0 to 50
Average power consumed -> 9.865176e-010 watts
Max power 2.760266e-001 at time 4.803e-007
Min power 3.276772e-002 at time 1.70325e-007
Total power consumed is: 48Mw.

3) Calculation Of Area

Total nodes = 422
= 422*18
=7596%100 = 75.96% in mm

By using GDI Technique we can reduce the VLSI design parameters like power consumption as well as area Performance. Hence this proves that by using GDI technique can reduce both power consumption and Area performance.

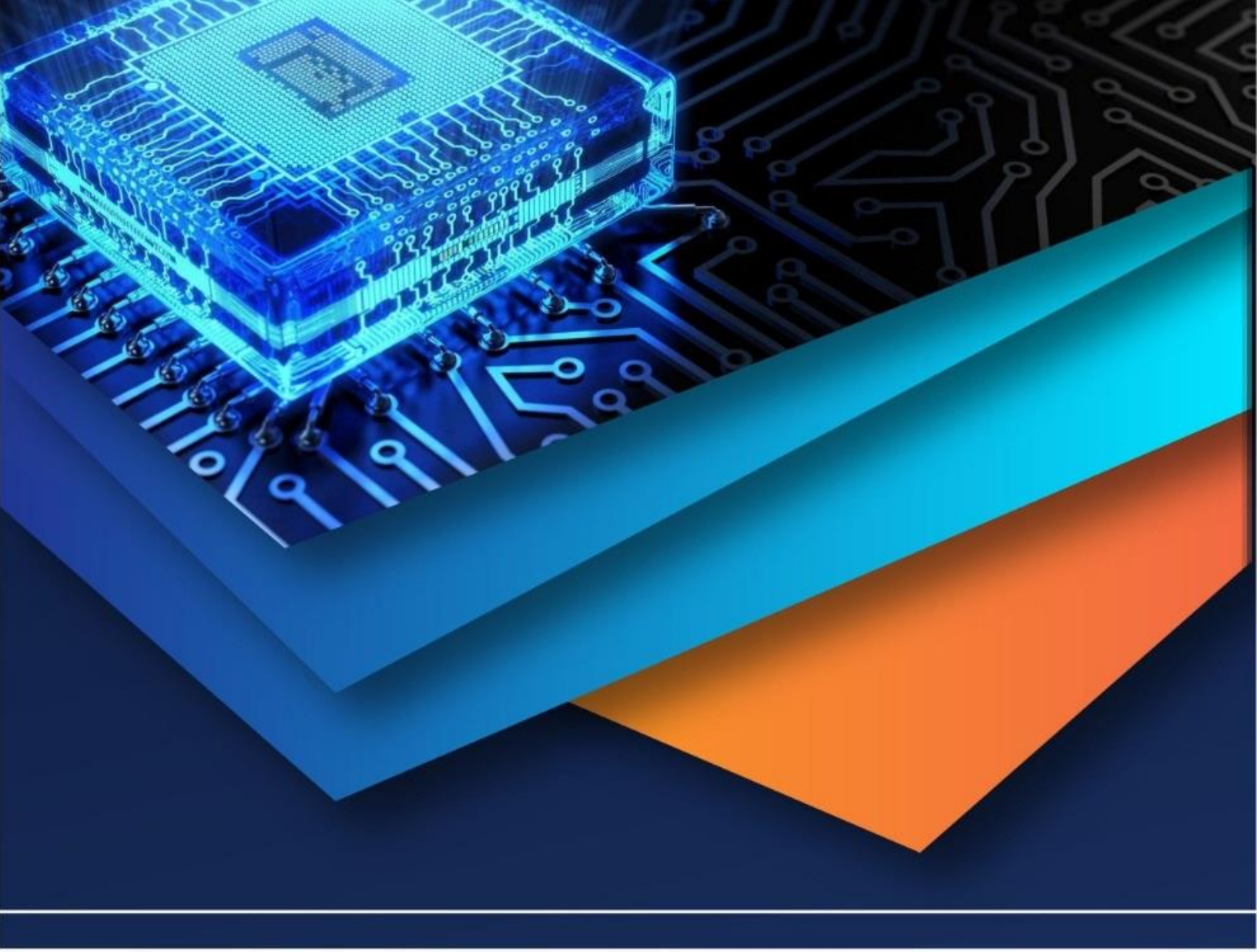
VI. CONCLUSION AND FUTURE WORK

S-EDIT in tanner software is used to provide a GDI- based thermometer-code shift-register that may be used in both directions. The proposed technique utilizes the power consumption by 48Mw and Area by 75.24% in mm by using 16-bit shift-registers on TSMC 0.18mm were simulated using a tanner W edit. However, the static differential sensing amp shared pulse latch has an undesirable switching that may lead to excessive dynamic power consumption and area occupancy. Modifying a shift register's transistor-level latch will further minimise its footprint and power usage.

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