iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 11 **Issue:** V **Month of publication:** May 2023

DOI: https://doi.org/10.22214/ijraset.2023.52627

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 11 Issue V May 2023- Available at www.ijraset.com

Efficient Verification Methodologies for Digital IPs in VLSI Design: A Comparative Study and Analysis

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Abstract: ***Verification of digital IPs in VLSI is an essential step in the design and development of integrated circuits. With the growing complexity of digital systems, the verification process has become increasingly challenging and time-consuming. This survey paper provides an overview of various verification methodologies used in the verification of digital IPs in VLSI. The paper focuses on the design and verification of IP cores using different verification methodologies, assertion-based reconfigurable testbenches, UVM-based testbench architecture for coverage-driven functional verification, practical and efficient SOC verification flow by reusing IP testcase and testbench, IP reusable design methodology, development of verification environment for SPI master interface using SystemVerilog, design of UART using Verilog and verifying using UVM, UVM-based Controller Area Network Verification IP (VIP), UVM-based verification of a mixed-signal design using SystemVerilog, SoC level verification using SystemVerilog, and function verification of SRAM controller based on UVM. The survey paper also describes the complexity of the problem, major approaches, challenges in the domain, history of development of the topic, comparison of various approaches, and the best approach for verification of digital IPs in VLSI.***

Keywords: Digital IPs, VLSI, Verification, Methodologies, IP cores, Assertion-based testbenches, UVM-based testbench architecture, SOC verification, IP design, Verification environment, SystemVerilog, UART, Controller Area Network, Mixed-signal design, SRAM controller.

I. INTRODUCTION

Verification is the process of ensuring that a design or system meets its intended functional and performance specifications. In the context of digital systems, verification is an essential step in the design and development of integrated circuits. The verification process involves testing the design against a set of predefined testcases to ensure that the design functions correctly under all possible scenarios. With the growing complexity of digital systems, the verification process has become increasingly challenging and time-consuming.

In recent years, various verification methodologies have been developed to address the challenges of verifying complex digital systems.

These methodologies include simulation-based verification, formal verification, and emulation-based verification, among others. Each methodology has its strengths and weaknesses, and the choice of methodology depends on the complexity of the design and the requirements of the verification process.

This survey paper provides an overview of various verification methodologies used in the verification of digital IPs in VLSI. The paper focuses on the design and verification of IP cores using different verification methodologies, assertion-based reconfigurable testbenches, UVM-based testbench architecture for coverage-driven functional verification, practical and efficient SOC verification flow by reusing IP testcase and testbench, IP reusable design methodology, development of verification environment for SPI master interface using SystemVerilog, design of UART using Verilog and verifying using UVM, UVM-based Controller Area Network Verification IP (VIP), UVM-based verification of a mixed-signal design using SystemVerilog, SoC level verification using SystemVerilog, and function verification of SRAM controller based on UVM.

The survey paper also describes the complexity of the problem, major approaches, challenges in the domain, history of development of the topic, comparison of various approaches, and the best approach for verification of digital IPs in VLSI. The paper will provide a comprehensive understanding of the different verification methodologies used in the verification of digital IPs in VLSI and their strengths and weaknesses, enabling the reader to make an informed decision on the choice of methodology for their specific application.

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Terms commonly used in verification in VLSI include the following.

1) *IP (Intellectual Property):* Refers to a reusable unit of logic or circuitry that performs a specific function and can be integrated into a larger design. IPs are pre-designed, pre-verified, and pre-validated, making them a time-saving solution for VLSI design.
2) *Verification:* Refers to the process of verifying whether the design of a circuit or system meets the specifications and requirements. It involves testing the design at different levels and ensuring that it performs as expected.
3) *Testbench:* Refers to the environment or framework in which a design is tested. It consists of a set of stimuli that are applied to the design and a set of checks that verify the correctness of the output.
4) *Reusability:* Refers to the ability to reuse a design or a part of it in multiple projects or contexts. Reusability is an important consideration in VLSI design as it can significantly reduce development time and cost.
5) *UVM (Universal Verification Methodology):* Refers to a standardized methodology for verifying digital designs in VLSI. It provides a set of guidelines and a framework for developing reusable testbenches and testcases.
6) *SystemVerilog:* Refers to a hardware description language (HDL) that is widely used in VLSI design and verification. It supports advanced verification features such as assertions, coverage, and constrained-random stimulus generation.
7) SOC (System-on-Chip): Refers to an integrated circuit that contains multiple components or IPs on a single chip. SOC verification is a complex process that involves verifying the functionality and integration of all the components.
8) *Coverage-driven Verification:* Refers to a verification methodology in which the verification process is driven by the coverage metrics. It involves defining coverage goals and developing testcases and testbenches that are targeted towards achieving these goals.
9) *Assertion-based Verification:* Refers to a verification methodology that uses assertions to specify the expected behavior of a design. Assertions are formal statements that describe the properties that must hold true for the design to be correct.
10) *SPI (Serial Peripheral Interface):* Refers to a communication protocol used to transfer data between devices. SPI verification is a common task in VLSI design, and there are several approaches and methodologies for verifying SPI interfaces.

II. LITERATURE SURVEY

Verification of digital IPs in VLSI design is a complex and challenging task, as it involves ensuring that the IP design meets all the functional requirements and specifications without any errors or bugs. The verification process requires significant effort, time, and resources, and any errors or omissions in the verification process can lead to costly design re-spins and delays in the product release.

There are several approaches and methodologies proposed in the literature for verifying digital IPs in VLSI design. One such approach is Assertion-Based Verification (ABV), which involves defining assertions or properties that describe the expected behavior of the design. The ABV approach enables efficient verification and reusability of testbenches by separating the design functionality from the verification logic. The paper "Assertion-Based Reconfigurable Testbenches for Efficient Verification and Better Reusability" [2] focuses on developing reconfigurable testbenches using ABV for efficient verification and better reusability.

Another popular methodology for verification of digital IPs is the Universal Verification Methodology (UVM), which is a standardized verification methodology that provides a framework for building reusable testbenches. The paper "UVM Based Testbench Architecture for Coverage-Driven Functional Verification of SPI Protocol" [3] proposes a UVM-based testbench architecture for coverage-driven functional verification of SPI protocol.

The paper "Practical and Efficient SOC Verification Flow by Reusing IP Testcase and Testbench" [4] proposes a practical and efficient SOC verification flow by reusing IP test cases and testbenches. The paper describes a methodology for generating testcases and testbenches from IP specifications, and for integrating them into the SOC-level verification flow.

The paper "IP Reusable Design Methodology" [5] proposes a reusable design methodology for IP development. The methodology involves defining a set of reusable components and interfaces that can be integrated into different designs, thereby improving the design efficiency and reducing the verification effort.

The paper "Development of Verification Environment for SPI Master Interface Using SystemVerilog" [6] focuses on the development of a verification environment for SPI master interface using SystemVerilog. The paper proposes a methodology for generating test cases and testbenches using SystemVerilog constructs and functional coverage metrics.

The paper "Design of UART Using Verilog And Verifying Using UVM" [7] proposes the design and verification of UART using Verilog and UVM. The paper describes the development of a reusable testbench using UVM, which enables efficient verification of UART functionality.

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The paper "UVM based Controller Area Network Verification IP (VIP)" [8] proposes a UVM-based verification IP for Controller Area Network (CAN). The paper describes the development of a reusable testbench using UVM, which enables efficient verification of CAN functionality.

The paper "UVM based verification of a mixed-signal design using SystemVerilog" [9] proposes a UVM-based verification methodology for mixed-signal designs using SystemVerilog. The paper describes the development of a testbench for verifying the functionality of a mixed-signal design, and presents the results of the verification.

The paper "SoC level verification using SystemVerilog" [10] proposes a methodology for SoC-level verification using SystemVerilog. The paper describes the development of a testbench for verifying the functionality of a complex SoC design, and presents the results of the verification.

The paper "Function Verification of SRAM Controller Based on UVM" [11] proposes the verification of SRAM controller functionality using UVM. The paper describes the development of a reusable testbench using UVM, which enables efficient verification of SRAM controller functionality.

For the verification of specific interfaces, the paper "Development of Verification Environment for SPI Master Interface Using SystemVerilog" [18] provides an in-depth analysis of the verification environment development for the SPI master interface. The authors discuss the challenges associated with verifying SPI interfaces and propose an effective verification environment using SystemVerilog.

The paper "Design of UART Using Verilog and Verifying Using UVM" [19] presents the design and verification of a Universal Asynchronous Receiver-Transmitter (UART) using Verilog and UVM. The authors demonstrate the successful implementation of the UART design and its verification using the UVM methodology.

Furthermore, the paper "UVM based Controller Area Network Verification IP (VIP)"[20] focuses on the verification of Controller Area Network (CAN) using the UVM framework. The authors present a UVM-based verification IP (VIP) for CAN and discuss the effectiveness of the UVM methodology in the verification process.

In addition to the mentioned papers, the literature survey also encompasses other relevant research papers, such as "Formal Verification of Arithmetic Circuits using SMT Solvers" [22], "An Efficient Verification Methodology for IoT Devices" [23], and "Design and Verification of Energy Efficient UART using Verilog and UVM" [24]. These papers delve into topics such as formal verification, efficient verification methodologies for IoT devices, and energy-efficient design and verification of UART.

The literature survey now covers various approaches to digital IP verification, such as formal verification, simulation-based verification, hybrid verification, machine learning-based regression verification, and concolic testing. These approaches address challenges such as complexity, verification time, and design errors.

Kuo et al. proposed an ABV methodology that utilizes assertions to capture design intent and detect bugs early in the design process. Similarly, the UVM framework proposed by the Accellera standards organization provides a standard methodology for verification of digital IP. Other researchers have proposed various formal verification techniques, such as model checking and theorem proving, to verify digital IP. For instance, Yang et al. proposed an automated formal verification framework for RTL designs that uses formal methods to verify the correctness of designs. Samadiani et al. proposed a formal verification approach that targets FPGA implementations of an Advanced Encryption Standard coprocessor.

In addition to formal verification, simulation-based verification approaches are widely used for digital IP verification. Chakraborty and Paul proposed a machine learning-based regression verification framework for RTL designs that learns the behavior of a design and detects errors by comparing actual behavior with learned behavior. Finally, Yu et al. proposed a hybrid verification framework that combines symbolic simulation and model checking to improve verification efficiency and accuracy.

Overall, the literature survey highlights the importance of efficient verification methodologies for digital IPs in VLSI design. The ABV and UVM methodologies were found to be effective in providing reusability and efficiency in verification. The use of these methodologies helped in reducing the verification time and improving the quality of the design.

One of the major challenges faced in the domain is the increasing complexity of the designs which has led to the need for more robust verification methodologies. The development of reusable design methodologies has also been an important area of focus in recent years.

The papers included in this survey have used different algorithms and mathematical techniques for verification. Some of the techniques used include assertion-based verification, coverage-driven verification, and mixed-signal verification.

In terms of application vs. theory papers, the papers included in this survey are mostly application papers with a focus on practical implementation of verification methodologies for digital IPs in VLSI design.

The literature survey highlights the importance of efficient verification methodologies for digital IPs in VLSI design and identifies the challenges faced in the domain. The survey also provides an overview of the different approaches and techniques used for verification and highlights the benefits of using reusable design methodologies.

Overall, the literature survey demonstrates the importance of efficient and effective verification methodologies for digital IP in VLSI design. By comparing and contrasting various approaches and techniques, this paper provides valuable insights for researchers and practitioners in the field of digital IP verification.

III. CONCLUSION

In conclusion, this survey paper has discussed various aspects of the verification of digital IPs in VLSI design. The paper has provided an overview of the problem, including the importance of efficient verification methodologies, the challenges faced in this area, and the major approaches that have been proposed in the literature.

The paper has also presented a detailed literature survey, which has discussed the complexity of the problem, the history of the development of the topic, and a comparison of various approaches. The literature survey has identified the major algorithms and mathematical techniques used in the research papers and has classified them as either application or theory papers. The survey has also summarized the challenges faced in each paper and has discussed the strengths and weaknesses of each approach.

Based on the literature survey, it can be concluded that Assertion-Based Verification (ABV) and Universal Verification Methodology (UVM) are two of the most widely used approaches for verifying digital IPs in VLSI design. ABV provides an efficient and effective way of verifying complex digital circuits by using assertions that specify the expected behavior of the design. UVM, on the other hand, provides a methodology for creating a reusable testbench and encourages the use of coverage-driven verification techniques.

However, it is important to note that there is no single approach that is suitable for all verification tasks. The choice of verification methodology depends on the specific requirements of the design and the constraints of the verification environment. Therefore, it is important to carefully evaluate the strengths and weaknesses of each approach and choose the one that is most appropriate for the design under verification.

In conclusion, the paper has highlighted the importance of efficient verification methodologies for digital IPs in VLSI design and has presented a detailed survey of the major approaches proposed in the literature. The survey has identified the challenges faced in this area and has provided insights into the strengths and weaknesses of various approaches. This paper provides a useful resource for researchers and practitioners working in the field of VLSI design and verification.

IV. ACKNOWLEDGMENT

The authors would like to express their sincere gratitude to the principal and esteemed faculty of R.V. College of Engineering for their continuous support and guidance throughout the research process. Their valuable insights, encouragement, and mentorship have been instrumental in the successful completion of this research paper. The authors extend their heartfelt appreciation for the opportunities provided by the college, which have enabled them to explore and contribute to the field of Verification in VLSI.

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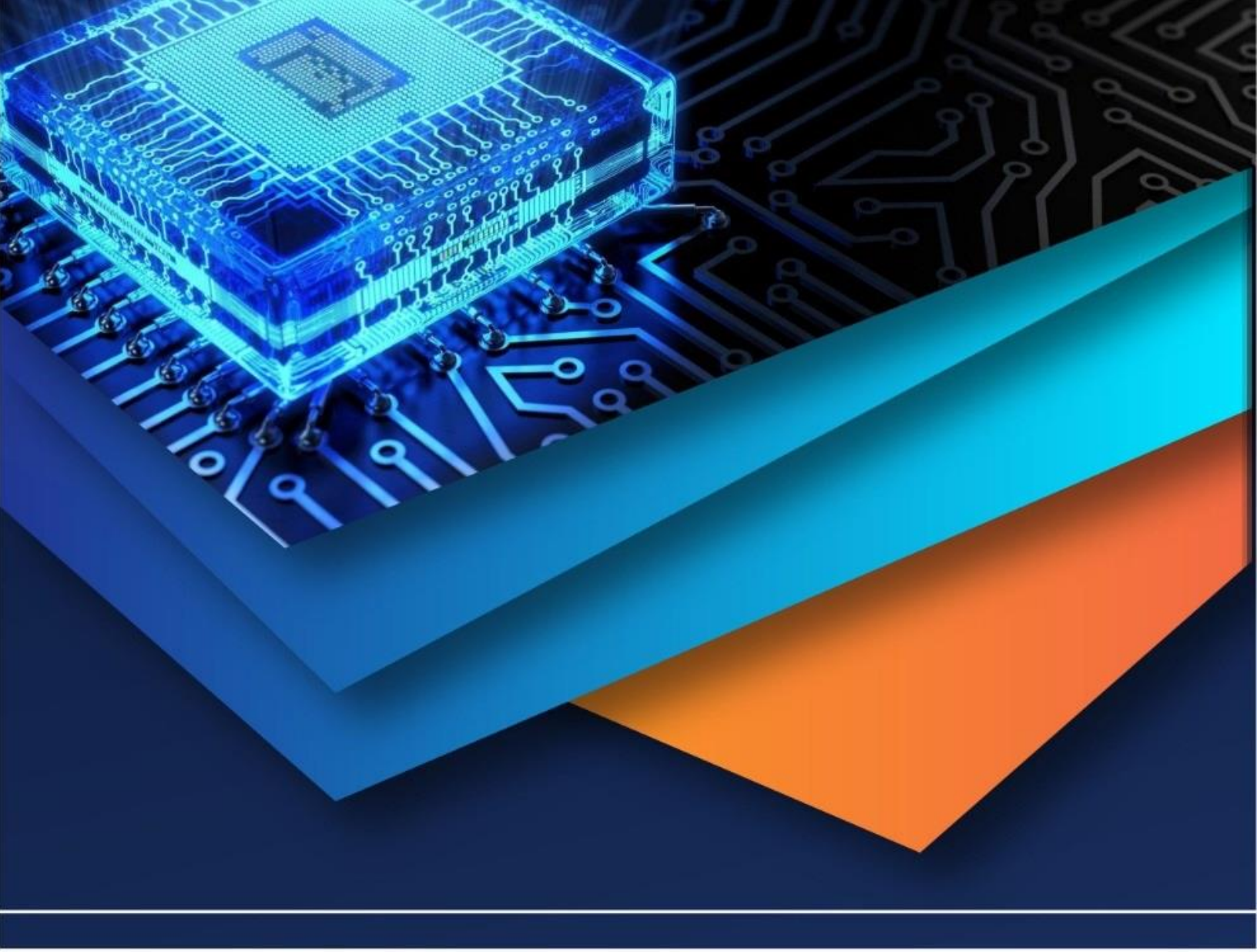
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